

A 19-GHz Broadband Amplifier Using a g_m -Boosted Cascode in 0.18- μm CMOS

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Abstract—This paper describes a broadband CMOS amplifier for differential receiver front-ends. A capacitive cross-coupling network provides passive g_m -boosting in the input cascode stage. This results in a greater than 30% increase in bandwidth. Combined with several other established bandwidth-enhancement techniques, the prototype achieves a measured 3-dB bandwidth of 19 GHz with no peaking in a 0.18- μm CMOS process. The dc gain is 11 dB differential, and the power consumption is 113 mW. Eye diagrams up to 24 Gb/s are shown.

I. INTRODUCTION

Differential broadband communication receiver front-ends require amplifiers with flat magnitude response, linear phase response, and an input impedance matched to 50 Ω per side. This paper describes a multi-stage amplifier that combines several bandwidth-enhancement techniques to meet these requirements over a 19-GHz bandwidth in a 0.18- μm CMOS process.

Distributed amplifiers can be used as differential broadband low noise amplifiers in CMOS [1]. However, they require accurate passive device modeling to avoid ripple in the gain and group delay [2]. They can also consume considerable area.

CMOS cascodes are popular broadband amplifiers. Using inductive peaking and other techniques to distribute parasitic capacitances, the bandwidth of amplifiers based on cascode stages has been extended to 10 GHz in 0.18- μm CMOS [3], [4]. In [5] and [6], a cross-coupling capacitance was used to boost the transconductance of a differential common-gate amplifier in order to improve its noise figure. In this work, applying the same technique to the common-gate devices in a differential MOS cascode results in a greater than 30% improvement in bandwidth.

The g_m -boosted cascode is analyzed in Section II. In Section III, an input pre-amplifier employing the g_m -boosted cascode is described, including measurement results. Section IV describes a multi-stage amplifier that includes additional differential stages to increase the overall amplifier gain to 11 dB.

II. BANDWIDTH-ENHANCEMENT TECHNIQUES FOR THE MOS CASCODE

A standard MOS cascode is shown in Fig. 1(a). Its bandwidth is determined by the time constants associated with the three nodes' parasitic capacitances: C_{IN} , C_X , and C_{OUT} .

The input time constant is the product of the total input capacitance, C_{IN} , and source resistance. Its effect can be reduced by inserting an inductance in series with the gate, L_1 in Fig. 1(b). This splits C_{IN} by separating the gate capacitance of M_1 from the output capacitance of the previous stage (or, as in this design, from the pad capacitance) [7].

The output time constant is the product of C_{OUT} and the amplifier's output resistance. Shunt and series peaking inductors, L_3 and L_4 in Fig. 1(b), can be used to improve the bandwidth at this node [8].

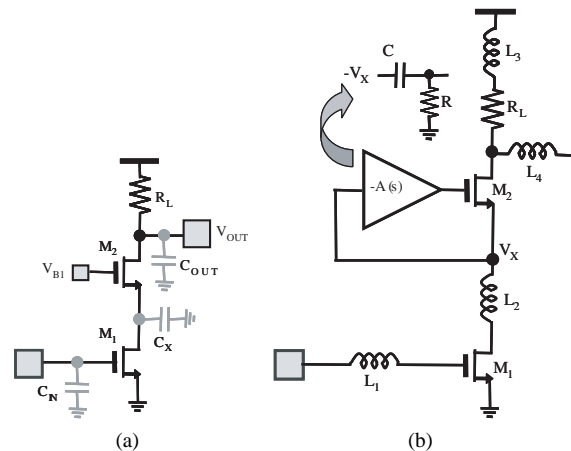


Fig. 1. (a) A conventional MOS cascode. (b) A g_m -boosted MOS cascode with enhanced bandwidth.

This leaves the time constant at the source of M_2 , approximately C_X/g_{m2} . Inserting inductor L_2 in Fig. 1(b) separates the drain capacitance of M_1 from the source capacitance of M_2 and, hence, improves the bandwidth at this node [3]. In this work, a feedback network, $A(s)$, is introduced to increase the effective transconductance of M_2 providing a further bandwidth improvement.

Gain-boosting is a well-established technique that uses an amplifier in place of $A(s)$ to increase the dc gain of a cascode stage. With negative feedback as shown in Fig. 1(b), the effective transconductance of M_2 is increased by a factor of $[1 + A(s)]$,

$$g_{m,\text{eff}} = [1 + A(s)]g_{m2}. \quad (1)$$

In a fully-differential circuit, a cross-connection can be used to provide the negative polarity of the feedback. Using a simple CR-section for the cross-connection provides a first-order high-pass response,

$$A(s) = \frac{RCs}{1 + RCs}. \quad (2)$$

Substituting (2) into (1) gives a frequency dependent transconductance,

$$g_{m,\text{eff}} = \frac{1 + 2RCs}{1 + RCs}g_{m2}. \quad (3)$$

Hence, at low frequencies $f \ll 1/4\pi RC$, $g_{m,\text{eff}} \approx g_{m2}$. Whereas, at high frequencies $f \gg 1/2\pi RC$, $g_{m,\text{eff}} \approx 2g_{m2}$. The result is a 6-dB g_m -boost at high frequencies, which reduces the effect of the time constant at the source of M_2 and, hence, extends the amplifier bandwidth.

Capacitive cross-coupling has previously been used to reduce the noise factor of a CMOS common-gate stage [5], [6]. Here, it is being

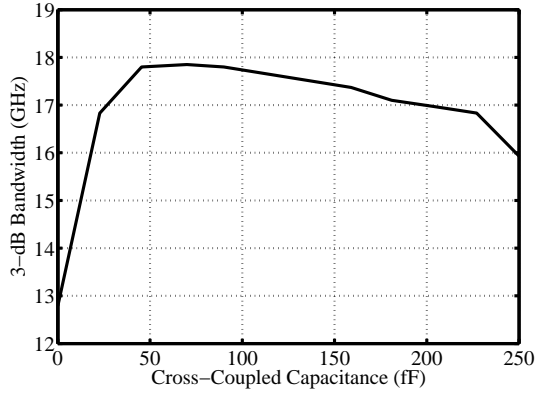


Fig. 2. Simulated bandwidth of the single-ended cascode in Fig. 1(b) showing the effect of cross-coupling capacitance, C .

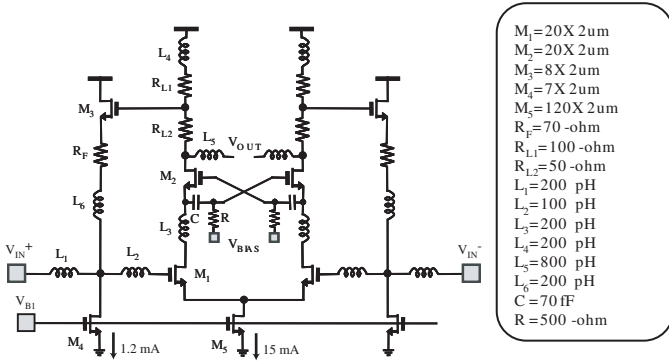


Fig. 3. A broadband differential cascode pre-amplifier with shunt-shunt feedback. All gate lengths are $0.18 \mu\text{m}$.

used for bandwidth improvement. However, if the value of the cross-coupling capacitor, C , is too large, its loading effect at the source of M_2 reduces the bandwidth. Fig. 2 shows simulation results for the single-ended cascode in Fig. 1(b). The component values and bias currents are the same as in the fully-differential pre-amplifier presented in Section III, except that the value of C is swept. They show that by choosing the capacitance correctly (50 – 100 fF, in this case), bandwidth is improved by 5 GHz, greater than 30%, over the case $C = 0$ (no g_m -boosting).

III. CASCODE PRE-AMPLIFIER

This section describes the design of a differential pre-amplifier that employs a g_m -boosted cascode in a $0.18\text{-}\mu\text{m}$ CMOS process. A schematic is shown in Fig. 3.

It employs all of the bandwidth enhancement techniques described in Section II in a differential amplifier with shunt-shunt feedback. The cross-coupling capacitance is 70 fF. To accommodate source-follower M_2 in the feedback path, a relatively high supply voltage of 2.5 V was used. Splitting the load resistance into two parts, R_{L1} and R_{L2} reduces the loading effect of the gate of M_3 [9]. Inductors L_1 and L_2 form a passive ladder network to distribute the parasitic capacitances at each node [3]. Finally, the inclusion of L_6 in the feedback path is known to improve bandwidth [10]. The pre-amplifier circuit consumes 44 mW.

The pre-amplifier was fabricated and tested on-wafer. A die photo is shown in Fig. 4(a). The area is $1.4 \text{ mm} \times 0.7 \text{ mm}$. The simulated and measured S_{21} of the circuit are plotted on Fig. 5. The measured

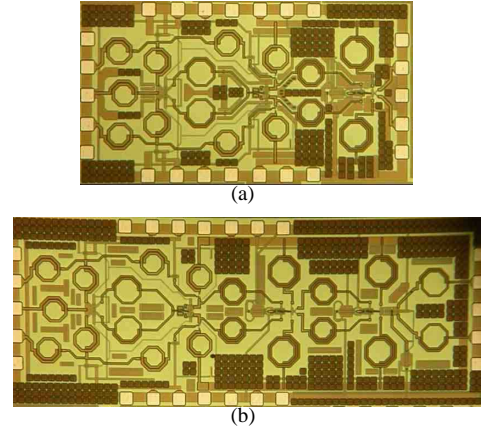


Fig. 4. Die photo of the two fabricated amplifiers: (a) pre-amplifier, (b) complete amplifier.

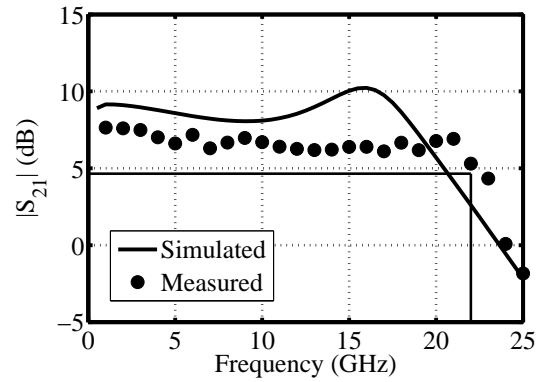


Fig. 5. Measured and simulated $|S_{21}|$ of the differential cascode pre-amplifier. (Single-ended S_{21} was measured and 6 dB added.)

dc gain is 1.5 dB less than simulated. The measured 3-dB bandwidth is 22 GHz with no peaking (20 GHz simulated).

IV. COMPLETE AMPLIFIER

The complete amplifier comprises the input pre-amplifier described in Section III plus two additional gain stages, as shown in Fig. 6. A schematic of the two post-amplifier gain stages is shown in Fig. 7.

The post-amplifier gain cells employ peaking inductors L_1 and L_2 to increase their bandwidth. In [11], these inductor were chosen so that $L_2/L_1 = 2$ resulting in 22-GHz bandwidth and a peaked magnitude response. Here, the inductors values were chosen to maintain a flat response and constant group delay, resulting in L_2/L_1 ratios between 0.4 and 0.9, similar to the design in [12]. In addition,

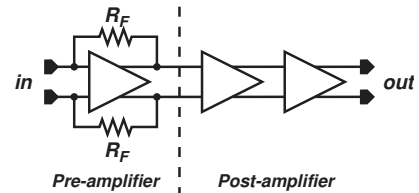


Fig. 6. Block diagram of the complete prototype amplifier.

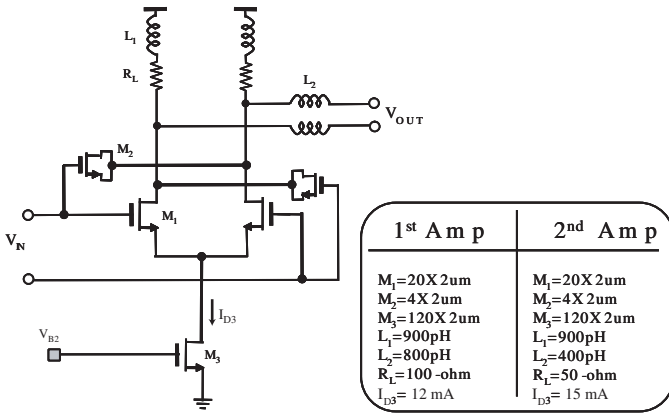


Fig. 7. The post-amplifier gain stages. All gate lengths are $0.18\ \mu\text{m}$.

cross-coupled MOS capacitors M_2 serve to partially cancel the gate-drain capacitances of the differential pair devices M_1 .

A die photo of the complete amplifier is shown in Fig. 4(b). The total area is $2\ \text{mm} \times 0.7\ \text{mm}$ and the total power consumption is $111\ \text{mW}$ from a 2.5-V supply. All measurements were performed on-wafer.

Fig. 8(a) shows the magnitude of S_{21} for the complete amplifier, both simulated and measured. The measurements were made with a 2-port network analyzer, so $6\ \text{dB}$ was added to show the differential gain. The measured 3-dB bandwidth is $19\ \text{GHz}$ with a gain of $11\ \text{dB}$. No peaking is observed in the measured response. The phase response, simulated and measured, is plotted in Fig. 8(b). The phase response is linear, implying constant group delay, within band. Fig. 9 plots the input and output return losses, S_{11} and S_{22} . Since a 2-port network analyzer was used, the results are single-ended. An input return loss better than $9\ \text{dB}$ is observed up to $18\ \text{GHz}$, and the output return loss is better than $10\ \text{dB}$ from 6 to $16\ \text{GHz}$. If used as the front-end of an integrated receiver, the amplifier will only drive on-chip loads and the output return loss is not critical. The measured transimpedance gain is $52\ \text{dB}\Omega$.

To demonstrate the suitability of the amplifier for broadband receiver front-ends, the circuit was tested with NRZ binary data inputs. The inputs are formed by multiplexing together four independent PRBS patterns. In Fig. 10, four $(2^{31} - 1)$ PRBS patterns are multiplexed resulting in a length- $4(2^{31} - 1)$ pattern. The data rates are 20 and $24\ \text{Gb/s}$ and the input swing is $270\ \text{mVpp}$. Only one side of the differential output is shown. The eye patterns are very symmetric with no obvious overshoot. The output eye amplitudes are $400\ \text{mVpp}$ per side and the RMS jitter is less than $3\ \text{ps}$.

As a sensitivity test, a 20-dB attenuator was used to provide a nominal $27\ \text{mVpp}$ input swing. The data rate was decreased to $14\ \text{Gb/s}$ to stay within the bandwidth of the attenuator and the pattern length was reduced to $4(2^7 - 1)$ to accommodate the oscilloscope's pattern locking capability. Fig. 11 shows the eye diagram at the amplifier output and the corresponding bathtub curve, indicating plenty of margin.

V. CONCLUSION

A g_m -boosting technique using capacitive cross-coupling was used to increase the bandwidth of a CMOS cascode stage. The technique was used in the design of a pre-amplifier with a measured 3-dB bandwidth of $22\ \text{GHz}$ in a $0.18\text{-}\mu\text{m}$ CMOS process. The pre-amplifier is the first stage of a broadband receiver front end with 11-dB

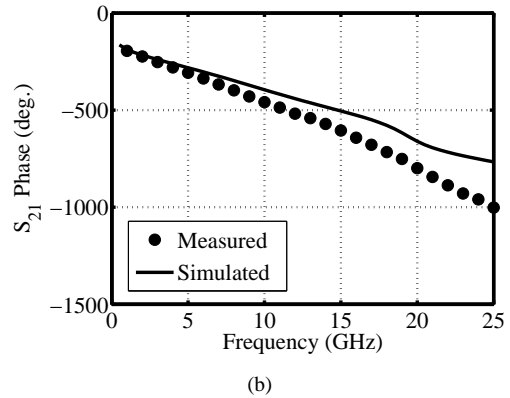
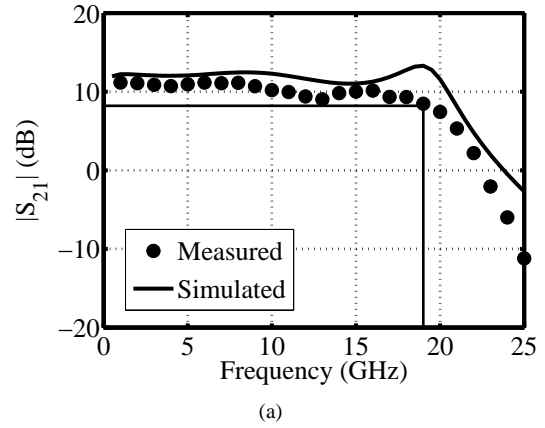


Fig. 8. Simulated and measured S_{21} of the complete amplifier: (a) magnitude and (b) phase. (Single-ended S_{21} was measured and $6\ \text{dB}$ added.)

gain, 19-GHz bandwidth, no peaking and linear phase response. These results are summarized in Table I and compared with other recently reported broadband amplifiers based on CMOS cascodes, demonstrating a significant bandwidth improvement. Eye diagrams up to $24\ \text{Gb/s}$ show little or no overshoot and excellent symmetry.

ACKNOWLEDGMENTS

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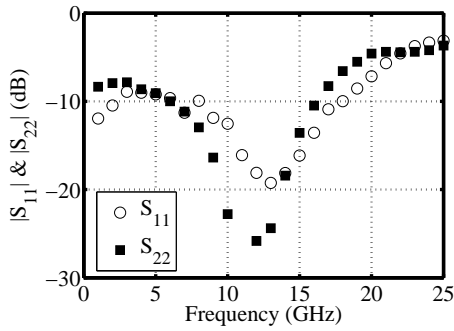
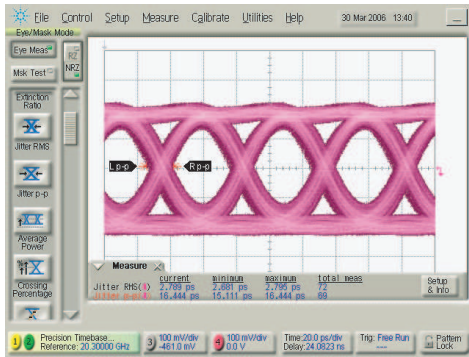
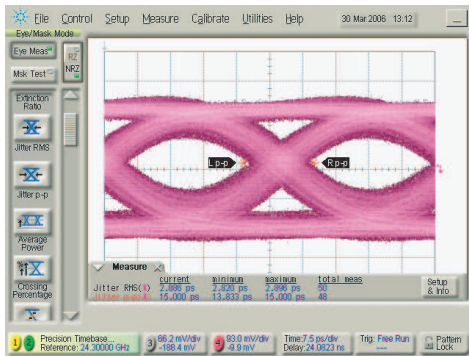


Fig. 9. Measured single-ended input and output return loss of the complete amplifier.



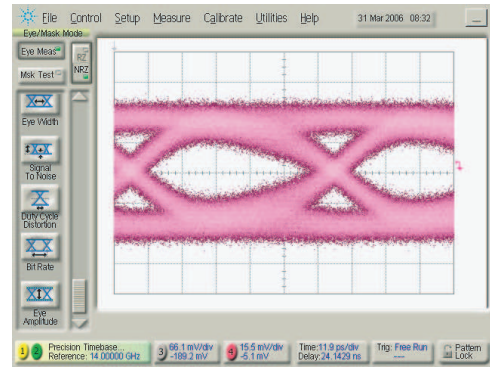
(a)



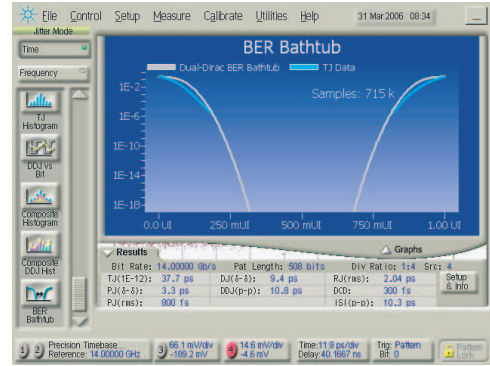
(b)

Fig. 10. Single-ended 400-mVpp output eye diagrams using a length-4($2^{31} - 1$) 270-mVpp NRZ input data pattern at: (a) 20 Gb/s (b) 24 Gb/s.

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(a)



(b)

Fig. 11. (a) Single-ended 60-mVpp output eye diagram for a 27-mVpp input length-4($2^7 - 1$) NRZ pattern at 14 Gb/s. (b) The corresponding BER measurement.

	This work	[3]	[4]
CMOS Technology	0.18 μm	0.18 μm	0.18 μm
Single-ended (SE) or Differential (Diff.)	Diff.	SE	SE
3-dB Bandwidth (GHz)	19	9.2	7.5
In-band $ S_{21} $ (dB)	11	—	9.3
In-band $ Z_{21} $ (dB Ω)	52	54	—
Sensitivity (μW)	3.6 @ 14 Gb/s	15.8 @ 10 Gb/s	—
Power (mW)	111	137.5	9
Supply voltage (V)	2.5	2.5	1.8
Area (mm^2)	1.4	0.64	1.1

TABLE I

PROTOTYPE SUMMARY AND COMPARISON WITH OTHER RECENTLY REPORTED BROADBAND CMOS AMPLIFIERS BASED ON CASCODE STAGES.

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