A 30-GS/sec Track and Hold Amplifier in 0.13-µm CMOS Technology

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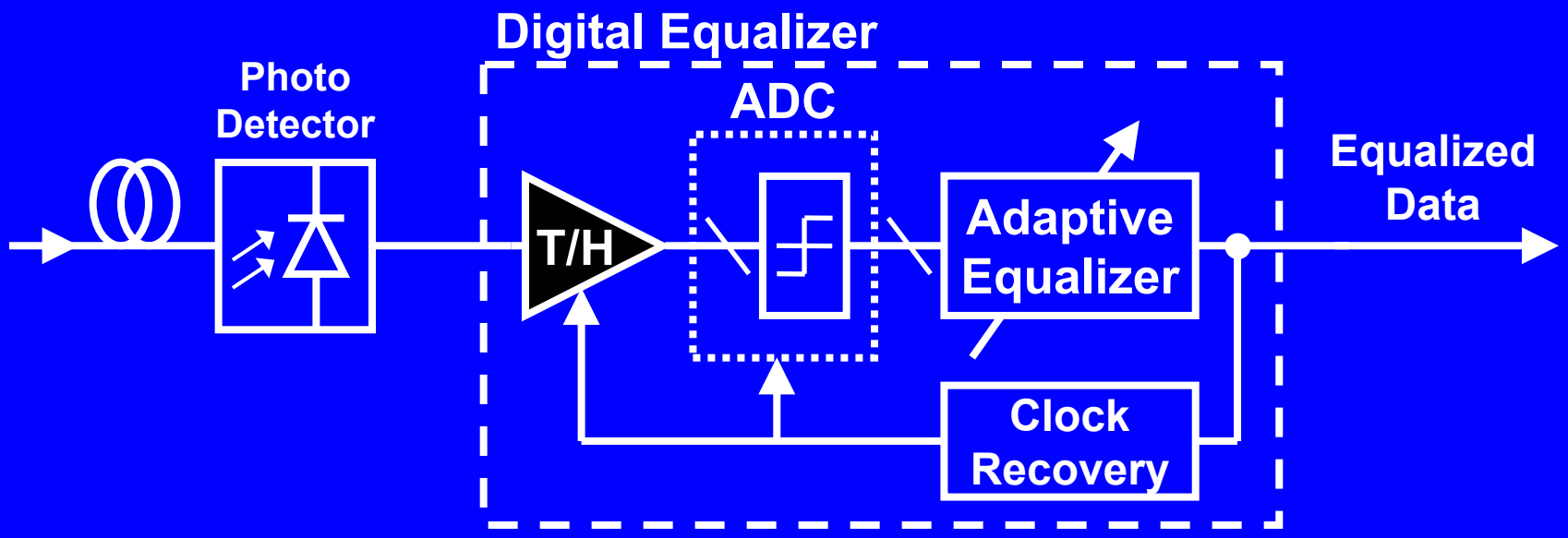
Introduction & Motivation I

- Equalization required at high bit rates
- Analog equalization up to 40 Gb/s
- Digital equalization is more robust and flexible



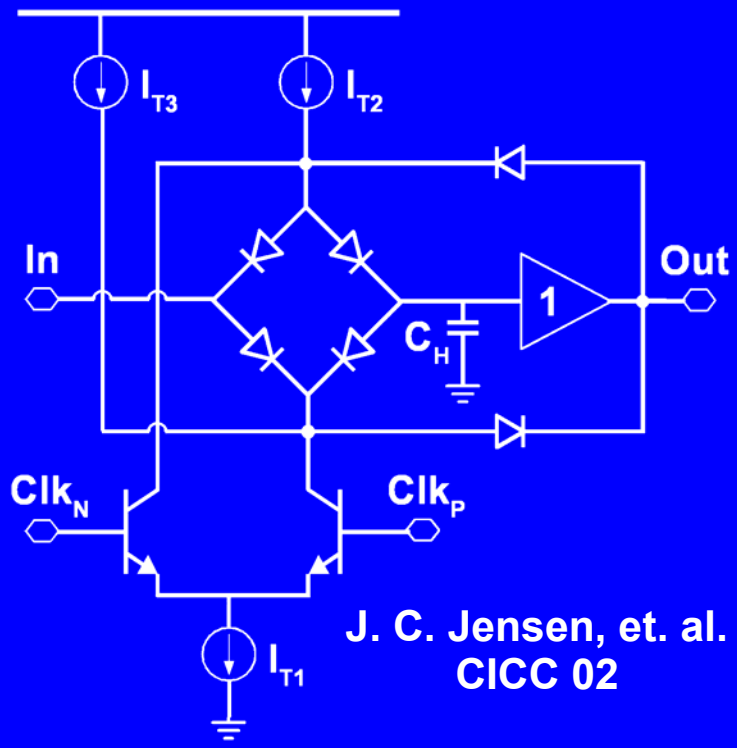
- Require full rate Track & Hold Amplifiers

Introduction & Motivation II

- Demonstrated 40-GS/sec THA in SiGe BiCMOS
  - f_T and f_{MAX} of 160 GHz
- CMOS technologies scaling to nanometre
  - f_T and f_{MAX} exceed 200 GHz for in production CMOS
- CMOS is a serious contender for implementing DSP based equalizers above 10 Gb/s

Introduction & Motivation III

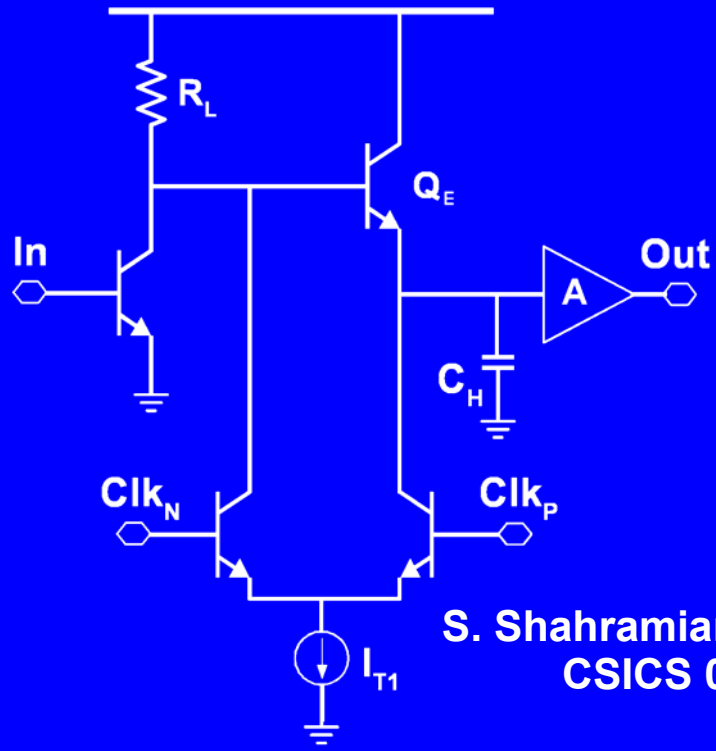
Diode Sampling Bridge



J. C. Jensen, et. al.
CICC 02

- High speed
- Low dynamic range
- Requires diodes

Switched Emitter Follower

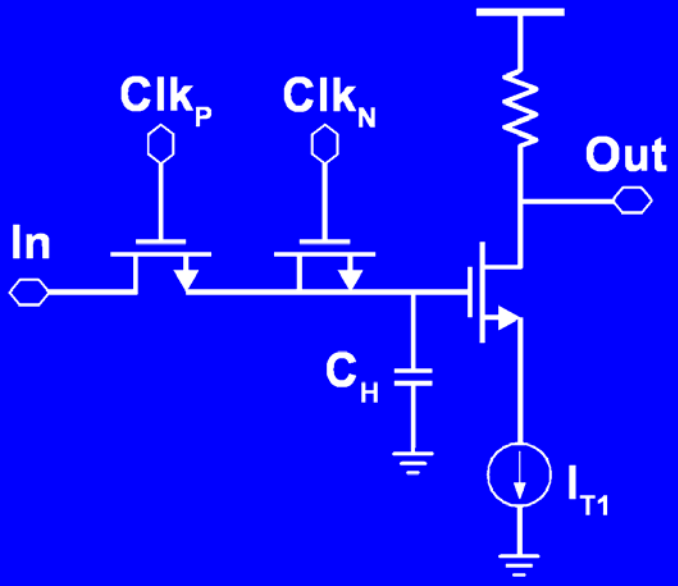


S. Shahramian, et. al.
CSICS 05

- High speed
- Lower supply
- Isolation in hold mode

Introduction & Motivation IV

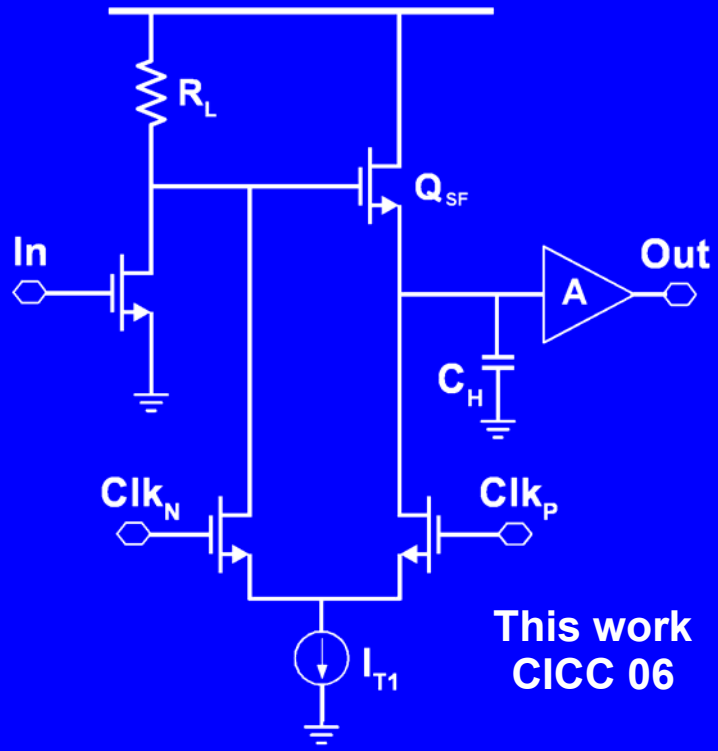
Series CMOS Sampler



I. H. Wang, et. al.
Electronic Letters 06

- Low supply
- Low speed due to series CMOS R_{ON}

Switched Source Follower

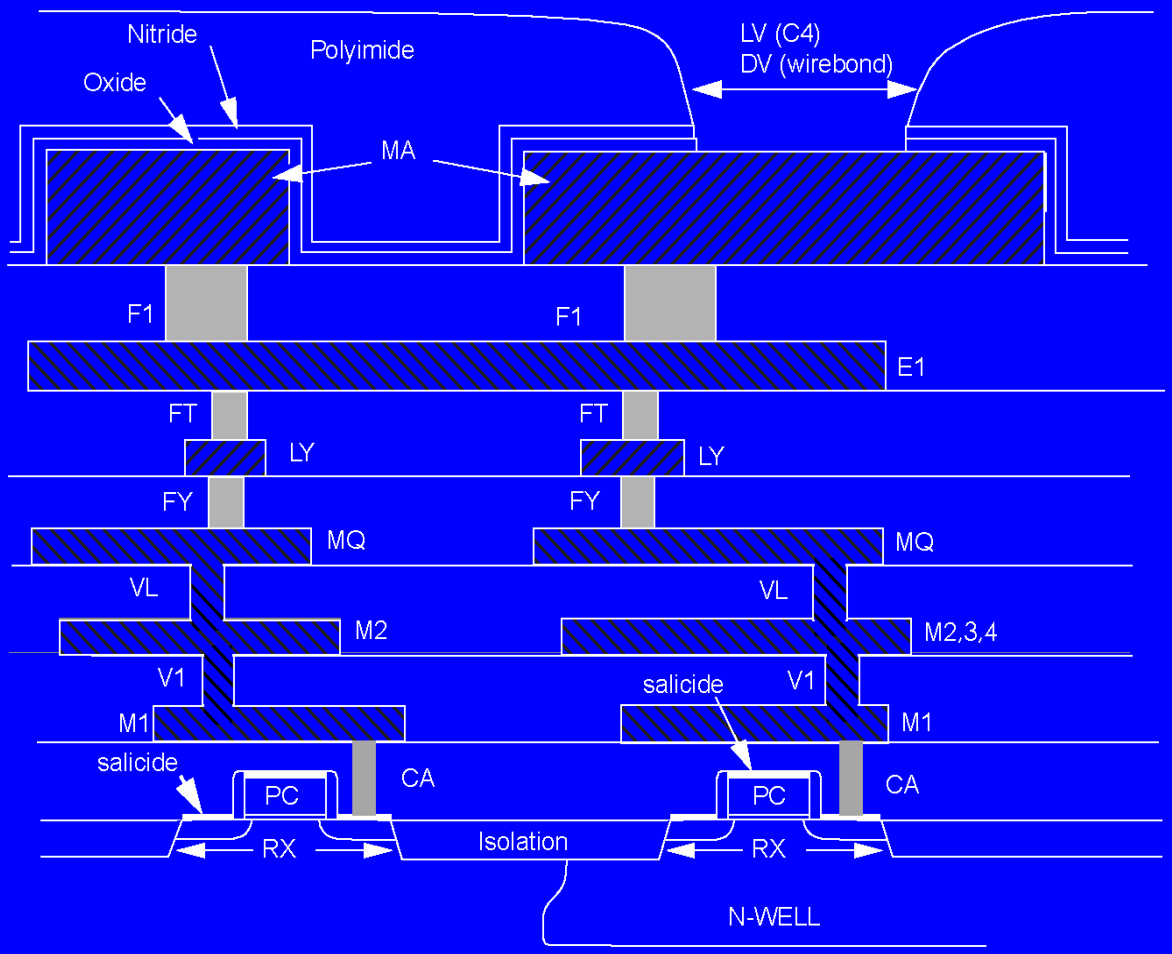


This work
CICC 06

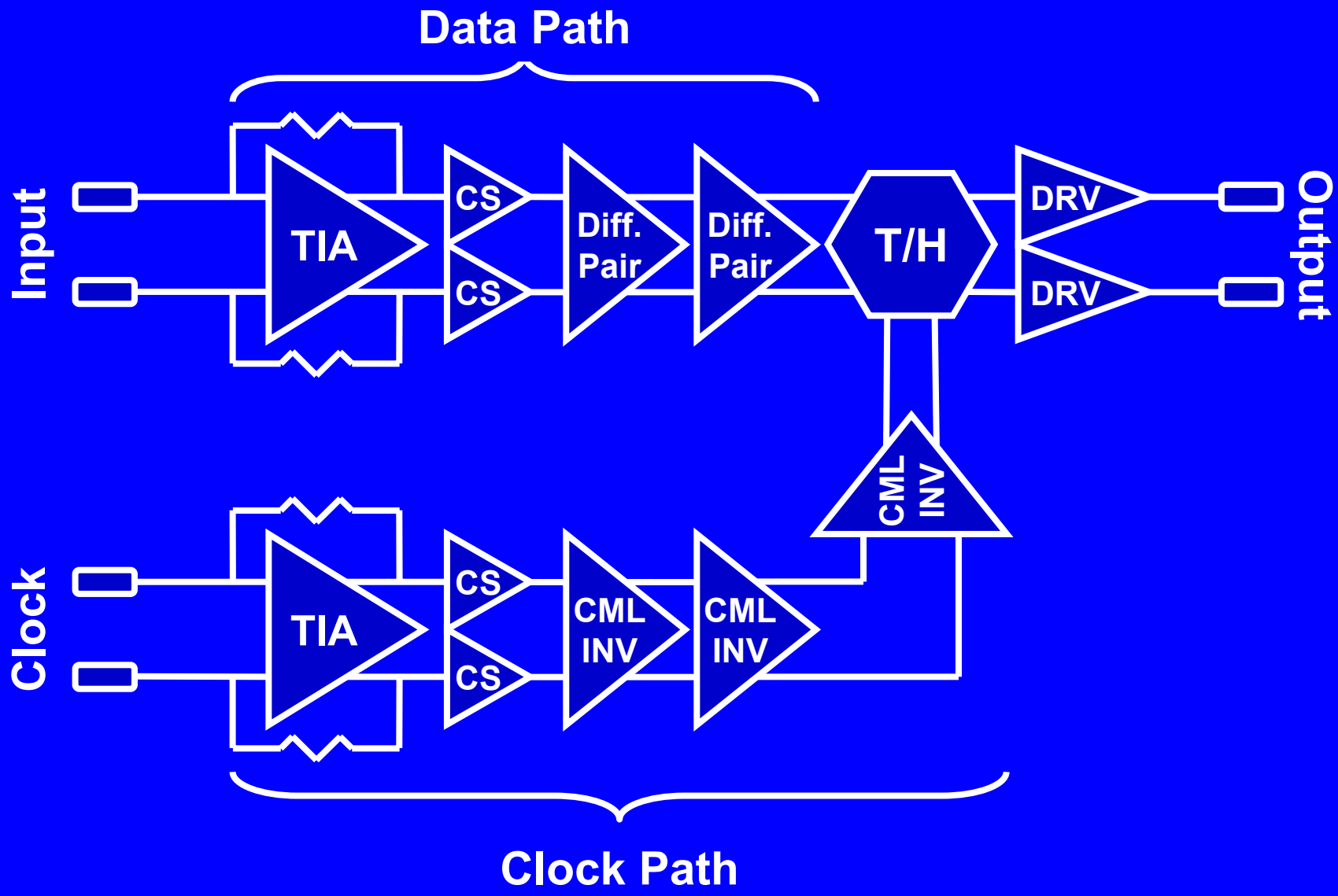
- Take advantage of high speed CMOS source follower

0.13-µm CMOS Technology

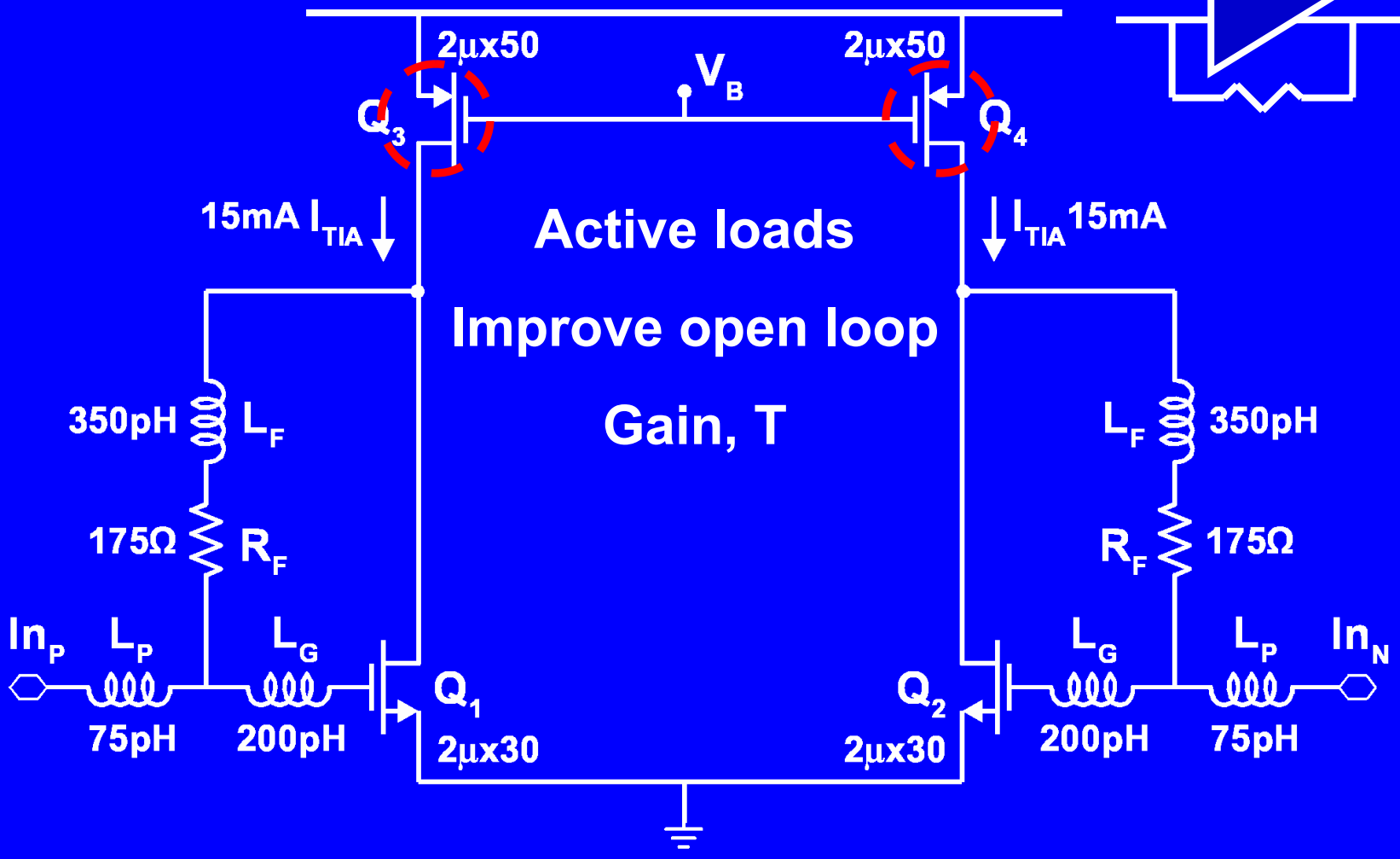
- Simulated f_T and f_{MAX} of 80 GHz
- 8 layer metallization back end with thick RF top metal layers
- Available triple-well CMOS transistors
- Available low power (high V_{TH}) transistors



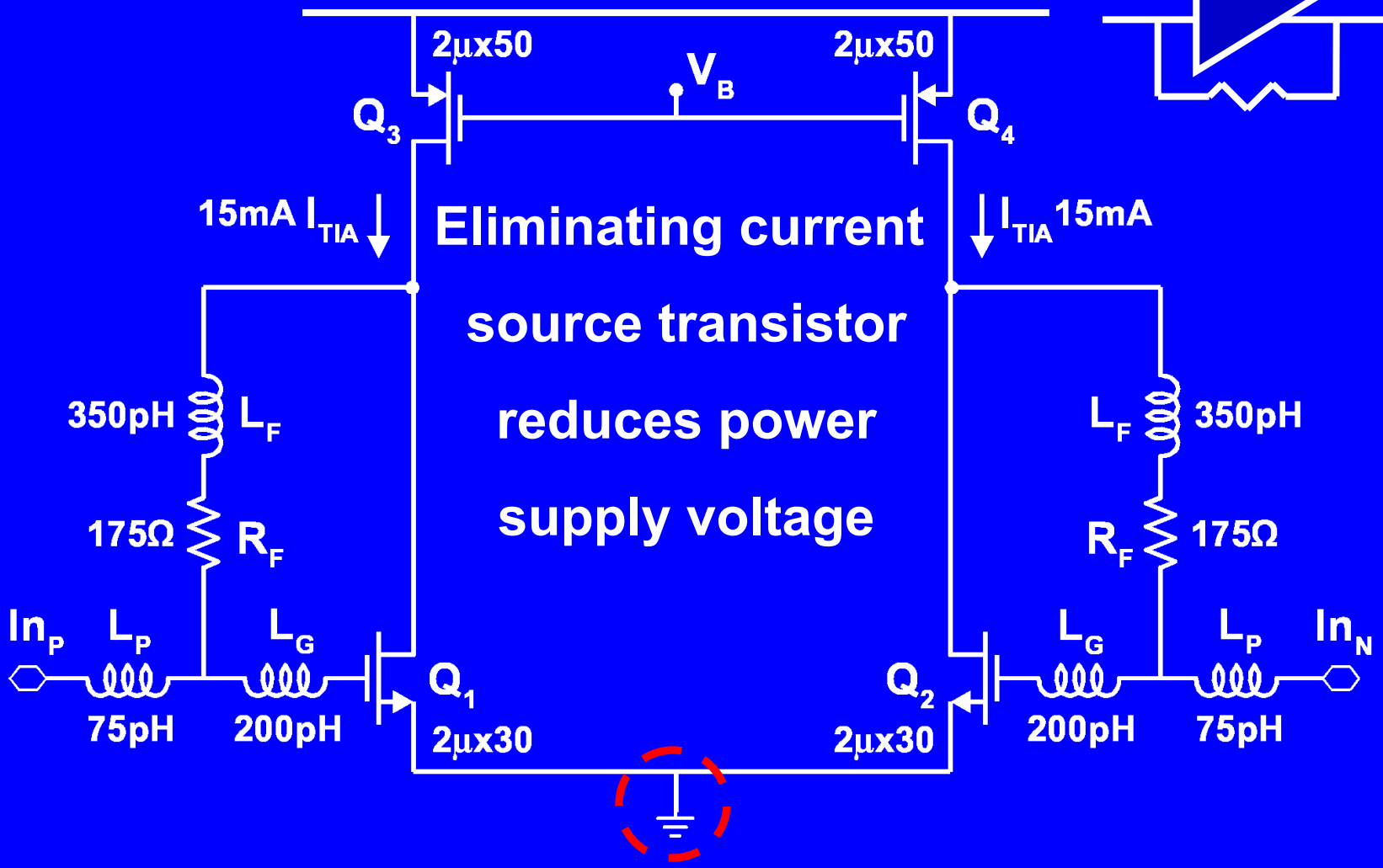
THA Block Diagram



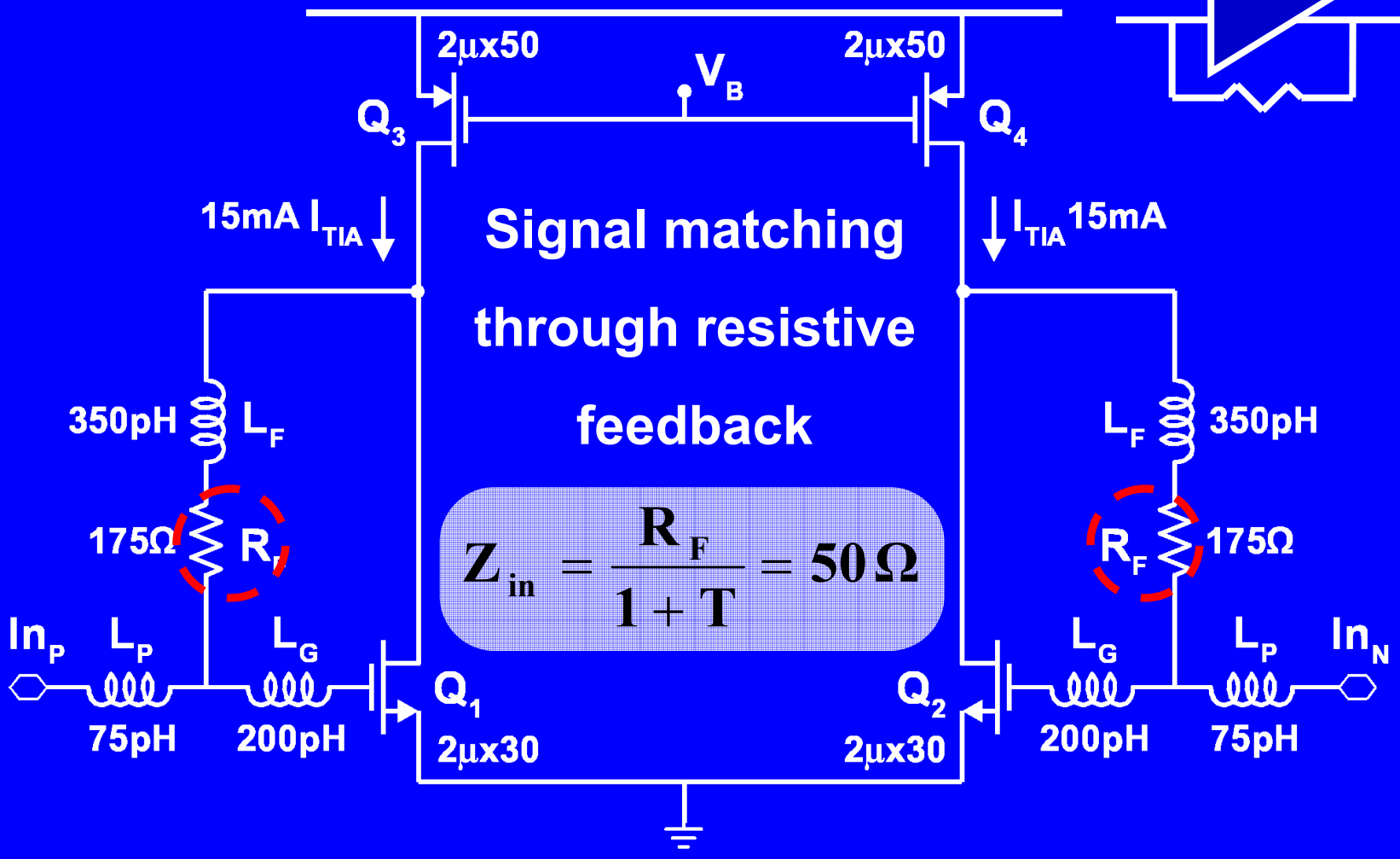
Input Stage Design



Input Stage Design



Input Stage Design



Input Stage Design

2μx50 2μx50

V_B

Q_3 Q_4

15mA I_{TIA} I_{TIA} 15mA

Noise matching through transistor sizing

350pH L_F L_F 350pH

175Ω R_F R_F 175Ω

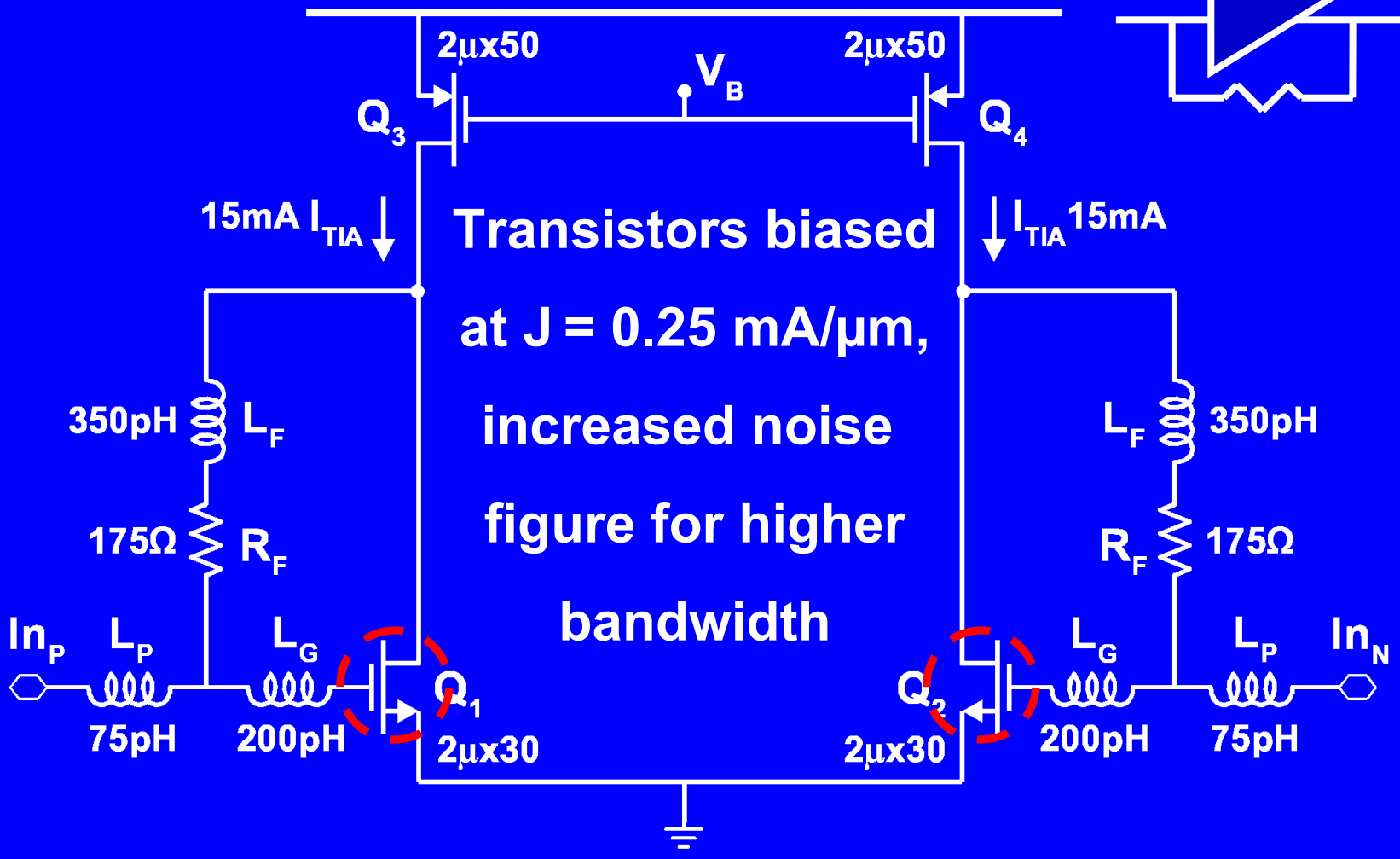
In_P L_P L_G L_G L_P In_N

Q_1 Q_2

75pH 200pH 2μx30 2μx30 200pH 75pH

$$W_{OPT} = \frac{1}{\omega}\left[\frac{1}{R_F\left(1+\omega_o^2\right)}+\frac{1}{Z_o}\right]\sqrt{\left(\frac{R}{\frac{G}{R}+G_C^2+B^2}\right)}$$

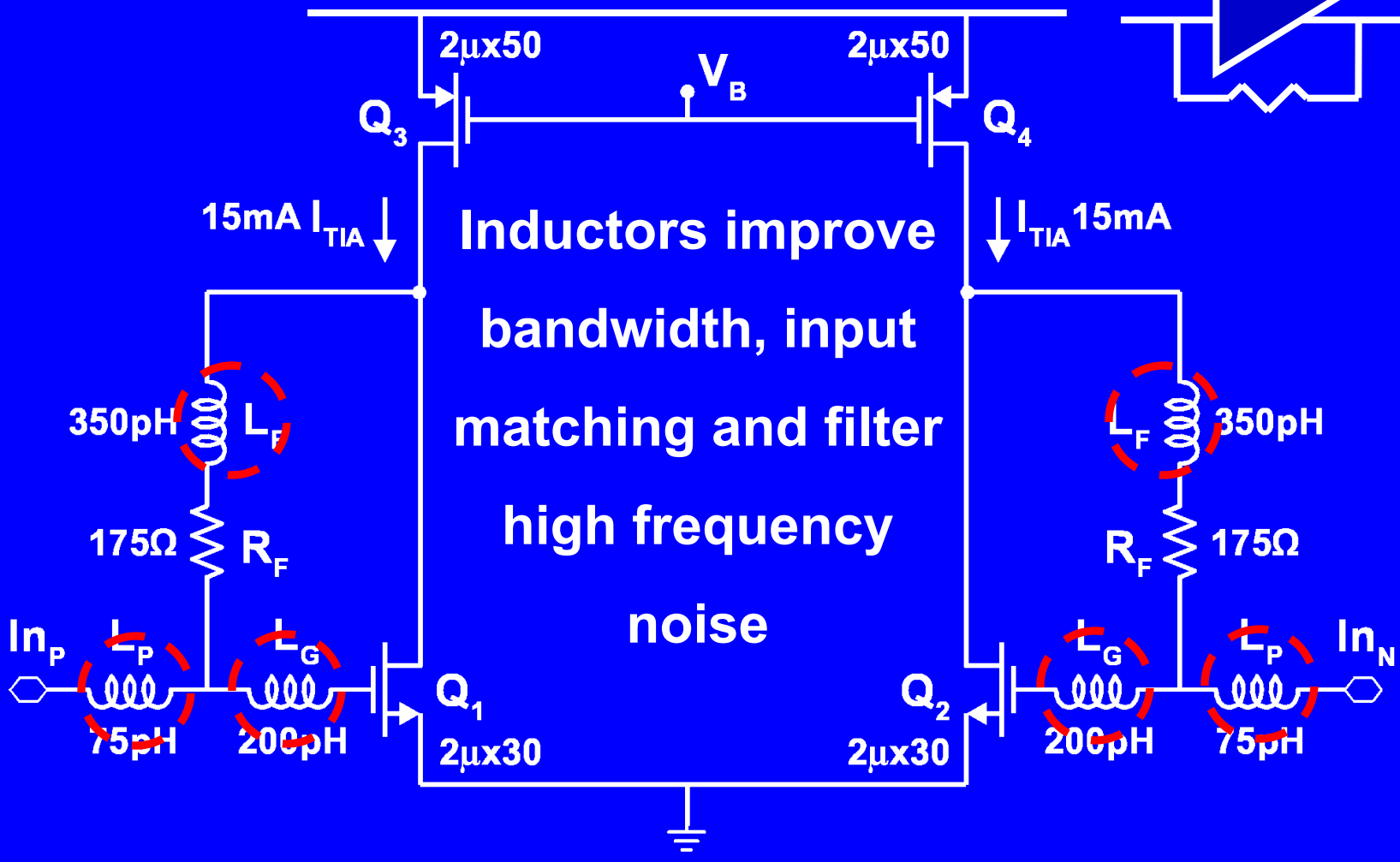
Input Stage Design



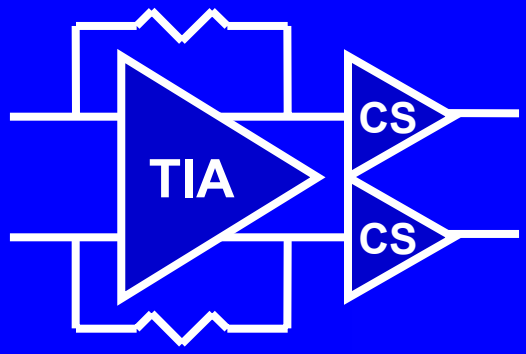
Simulated bandwidth: 30 GHz

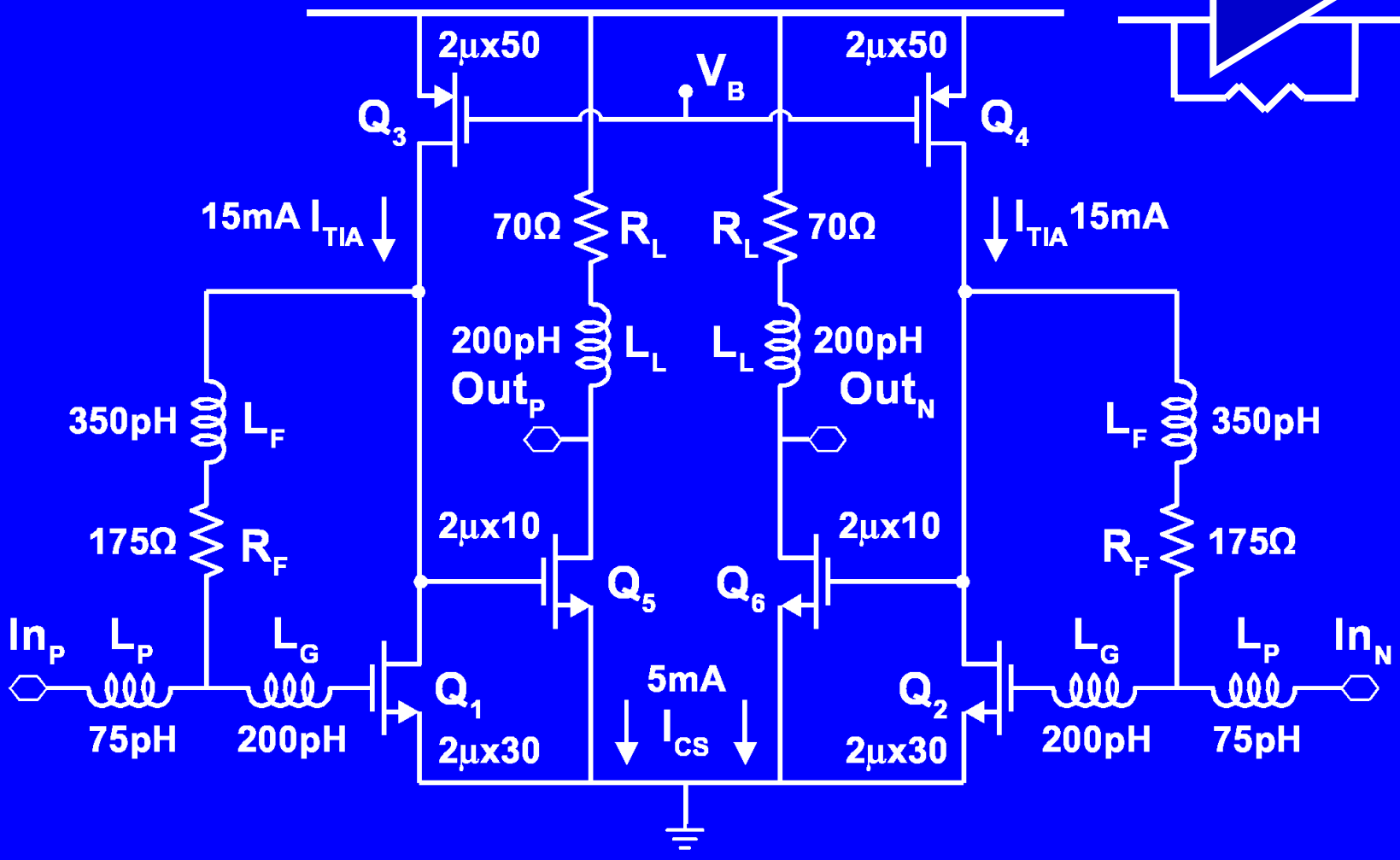
Simulated input integrated noise over 30 GHz: 0.5 mV_{rms}

Input Stage Design



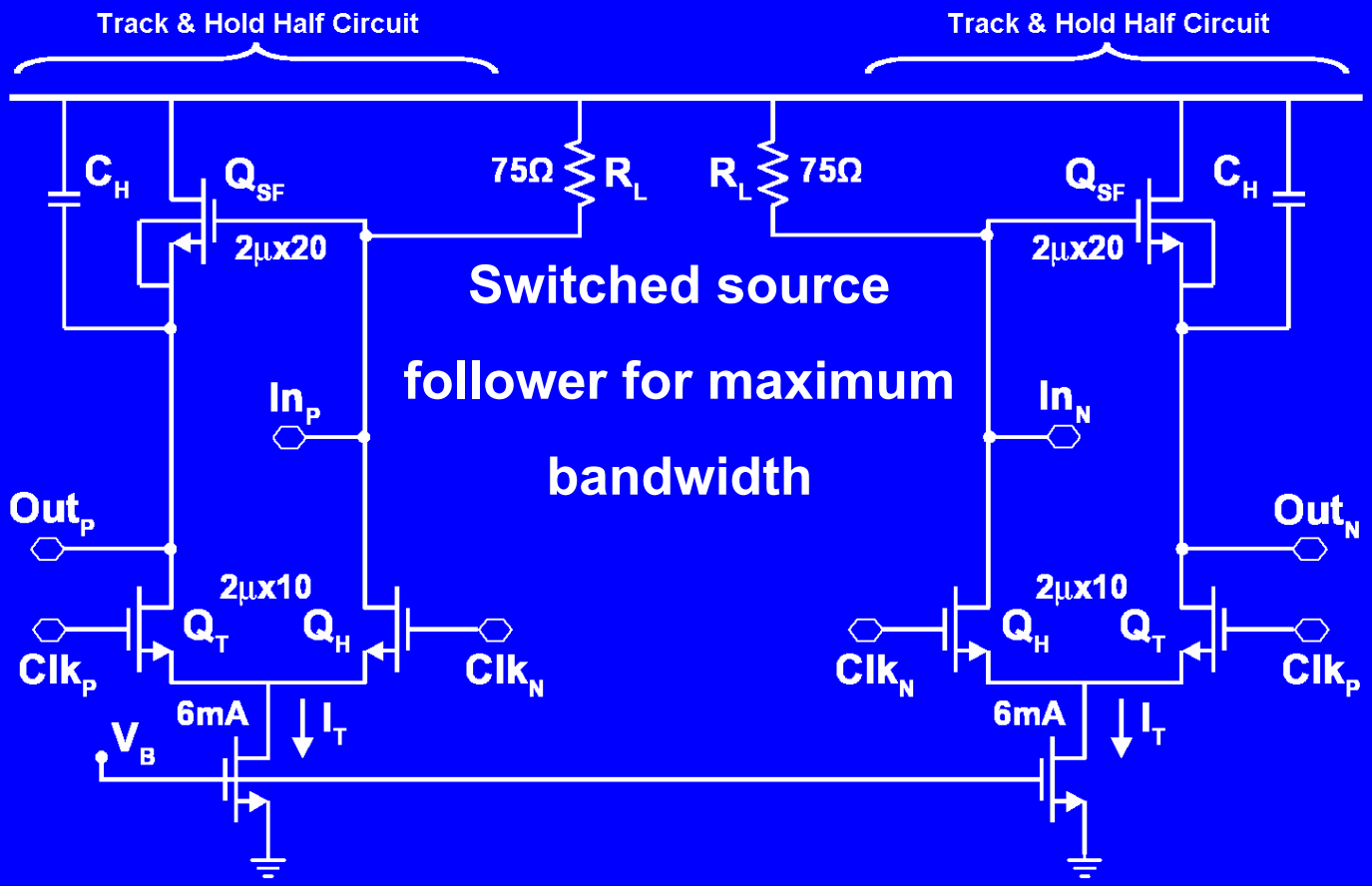
Input Stage Design



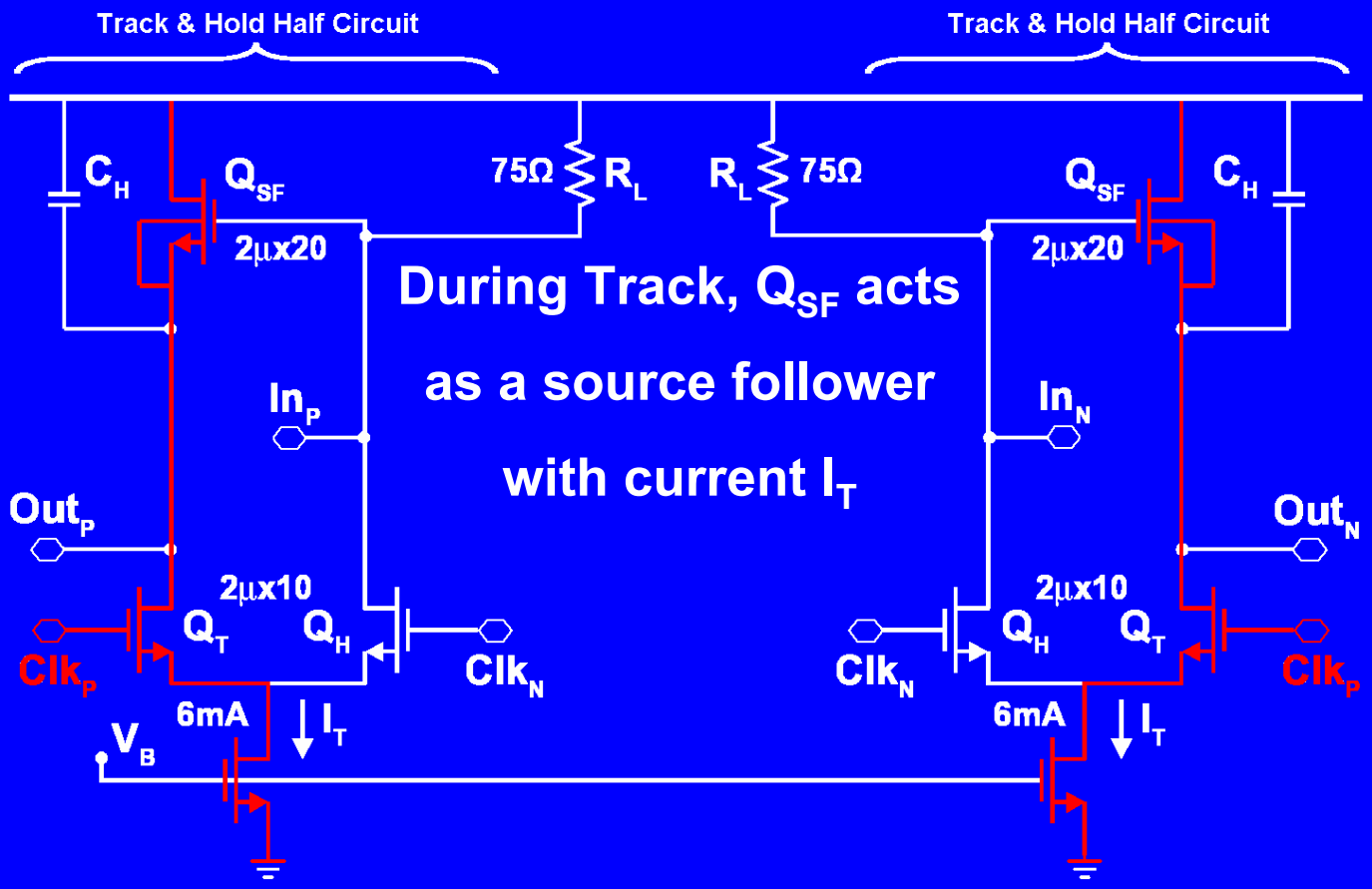


Transistors Q_1 and Q_2 are diode-connected at DC and therefore can bias the next CS stage

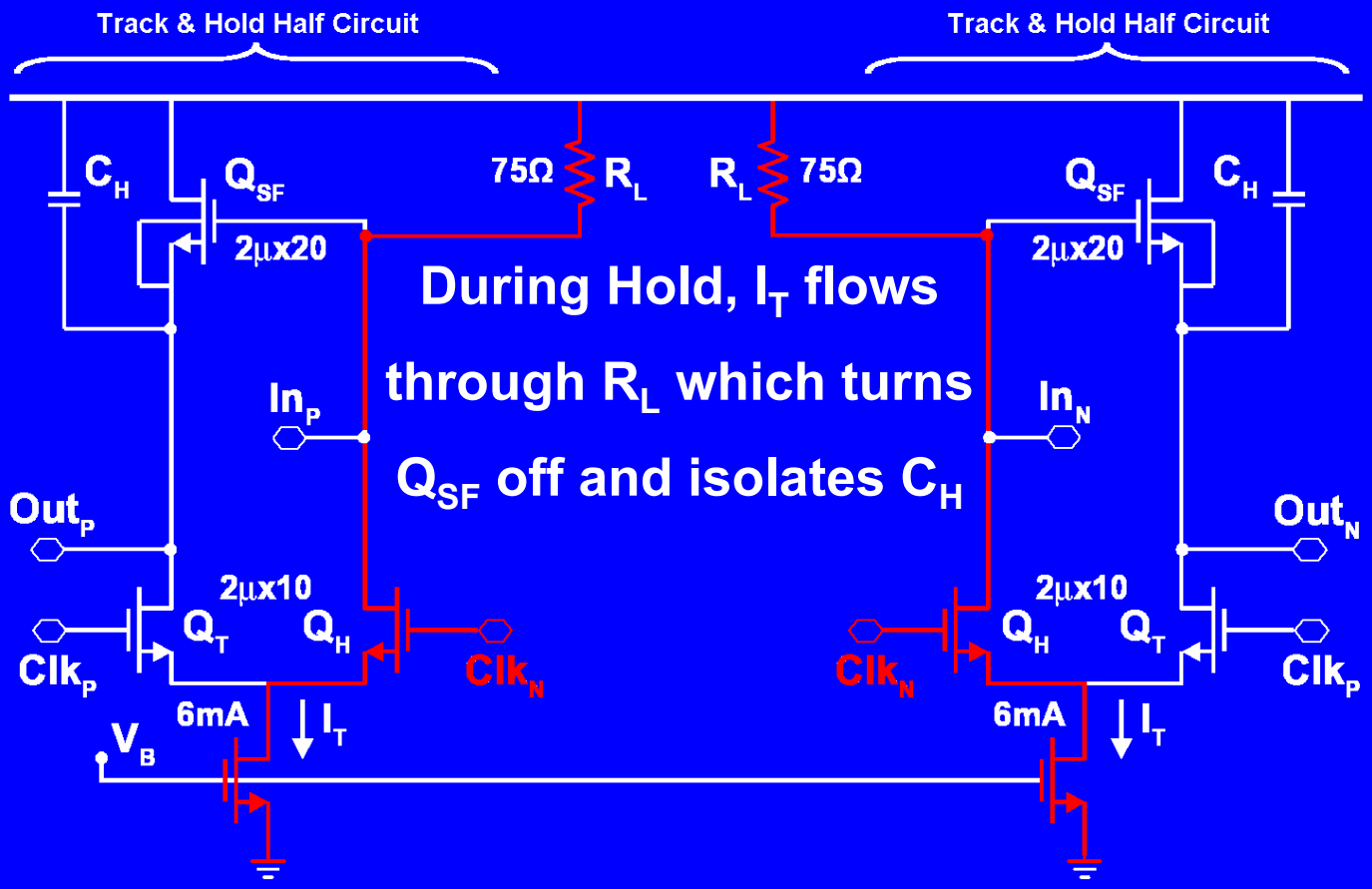
THA Stage Design



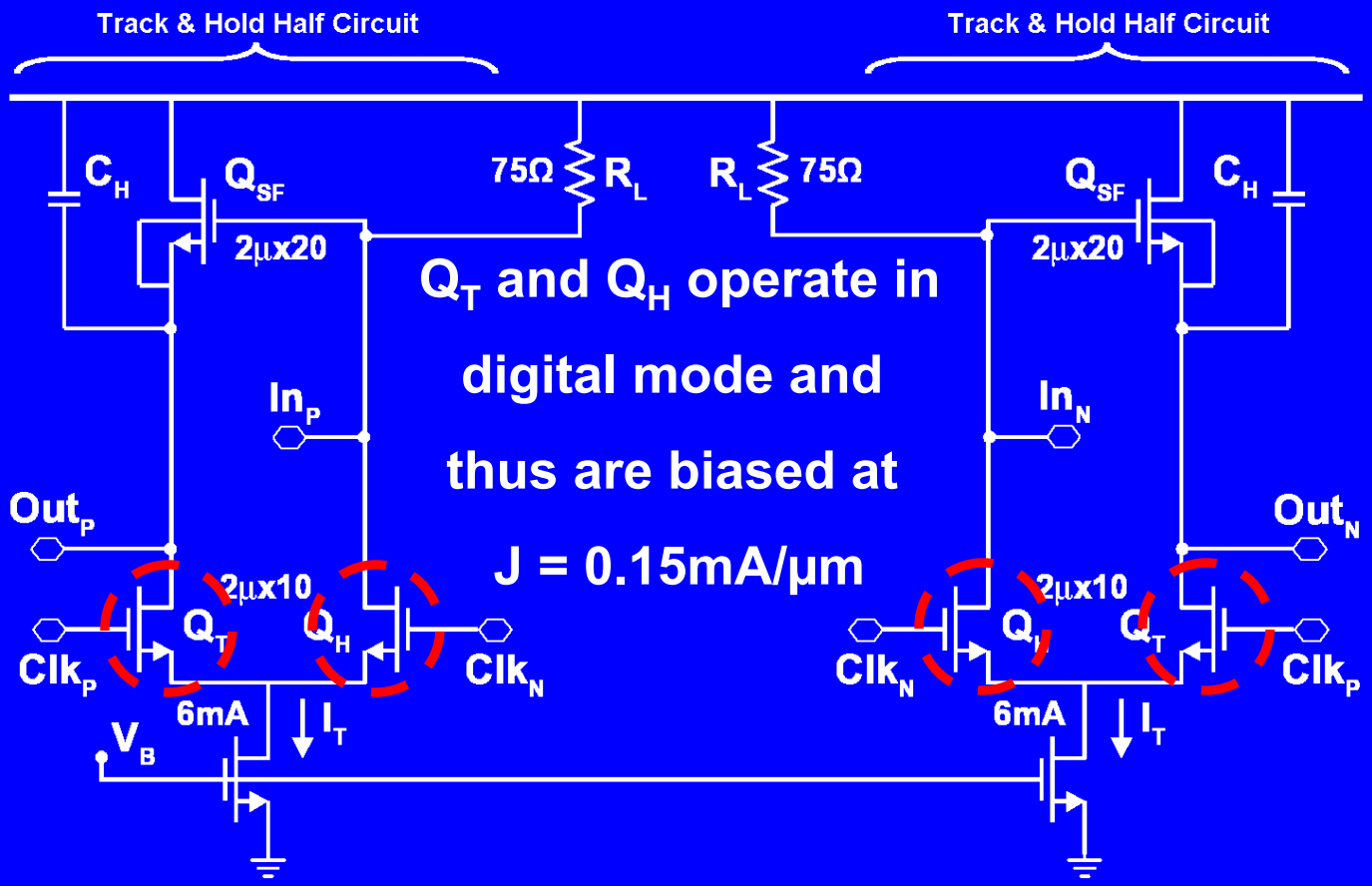
THA Stage Design



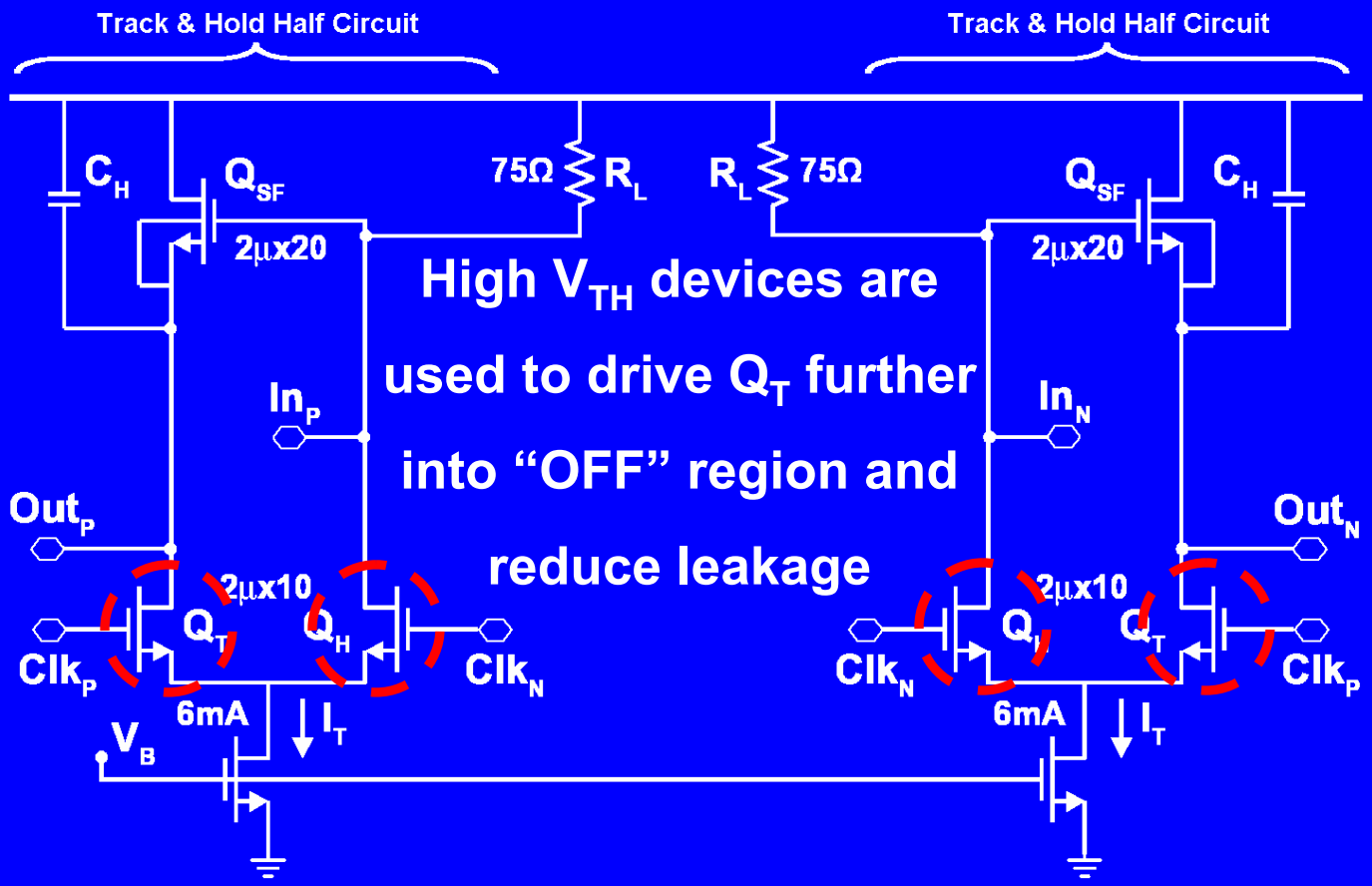
THA Stage Design



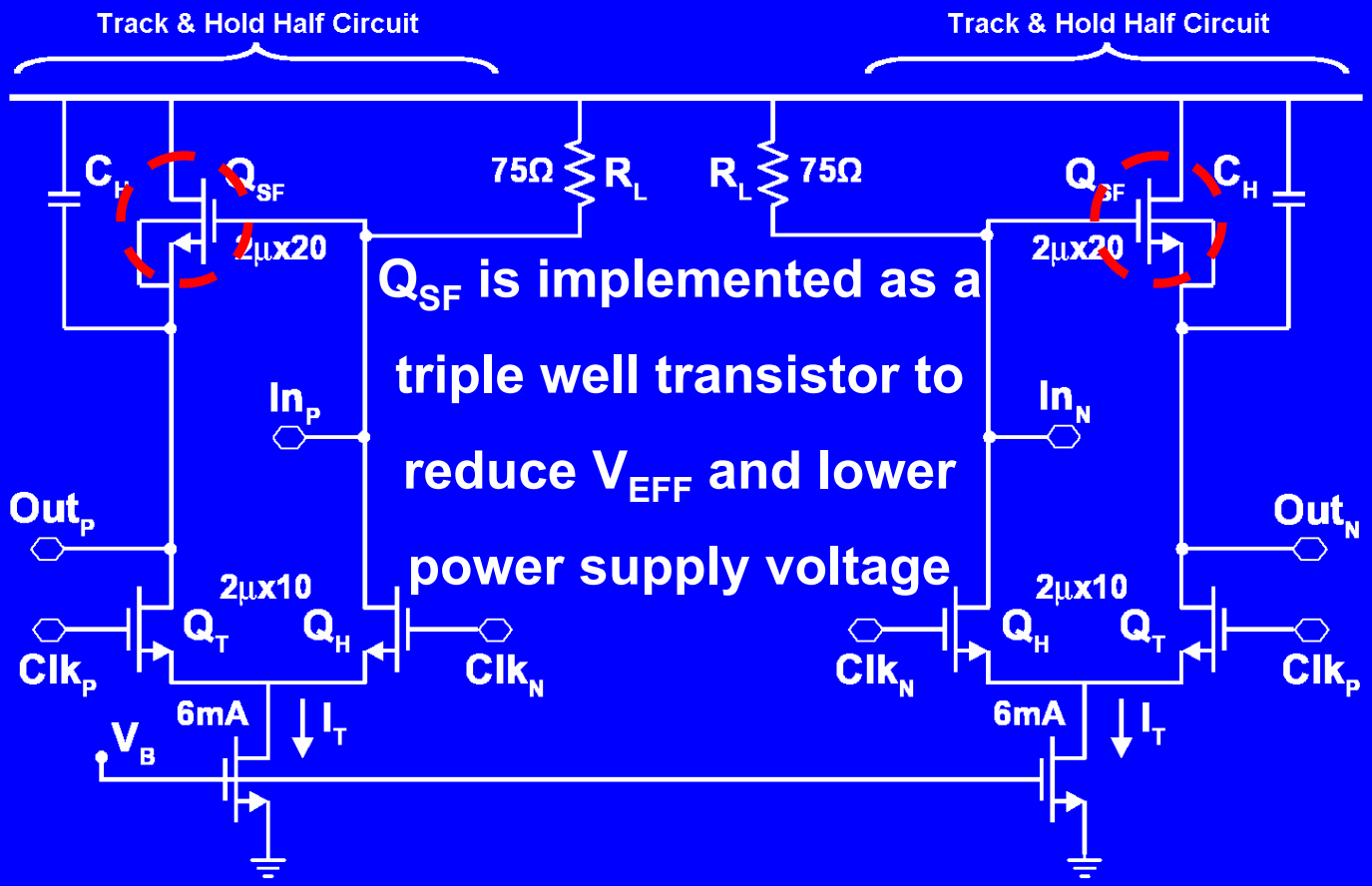
THA Stage Design



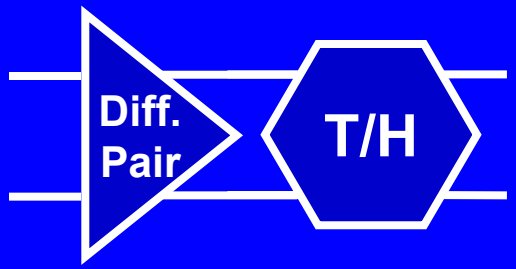
THA Stage Design



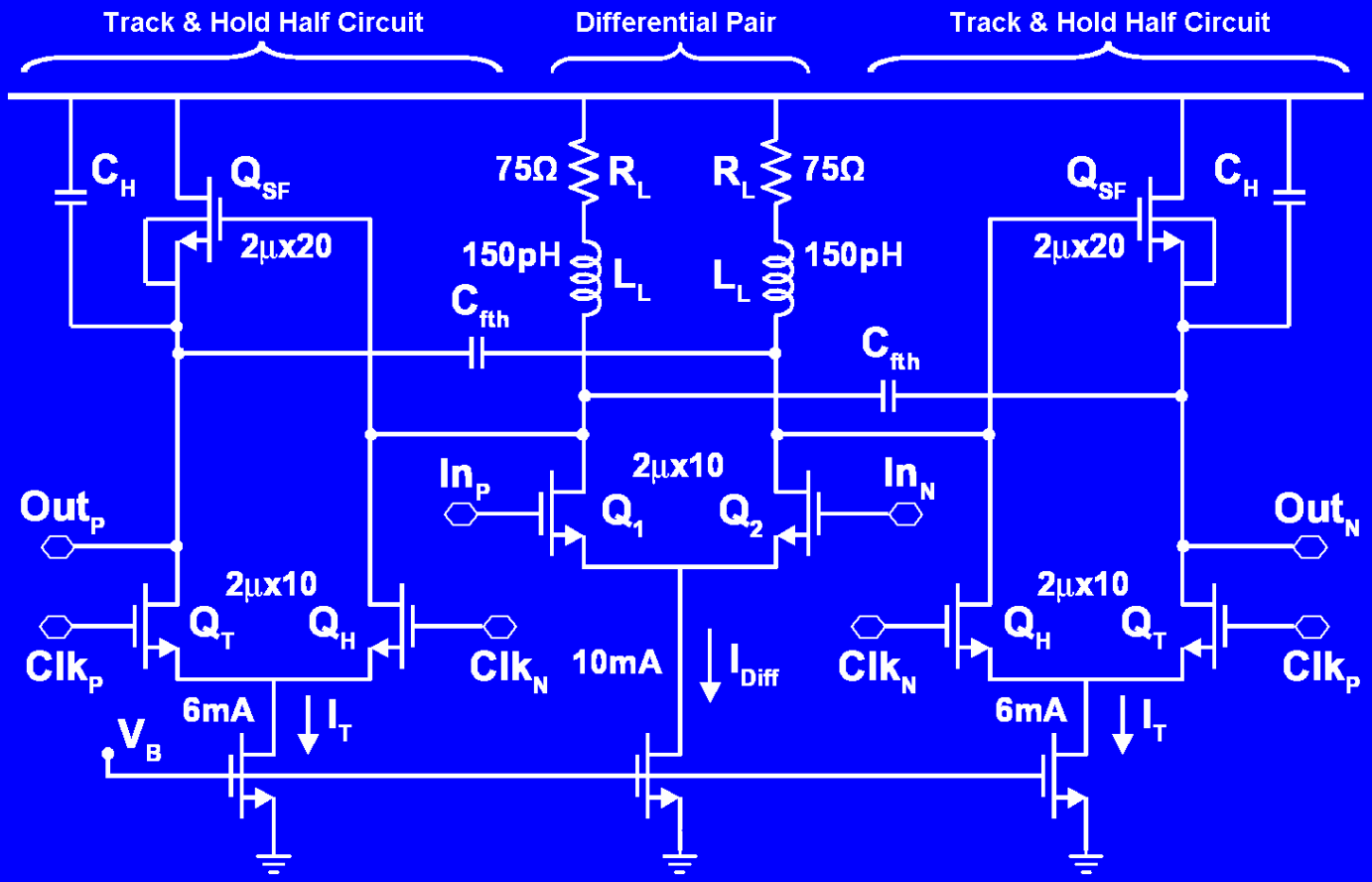
THA Stage Design



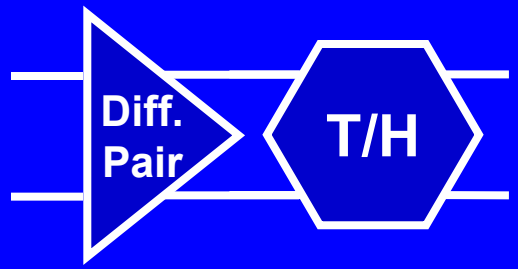
THA Stage Design



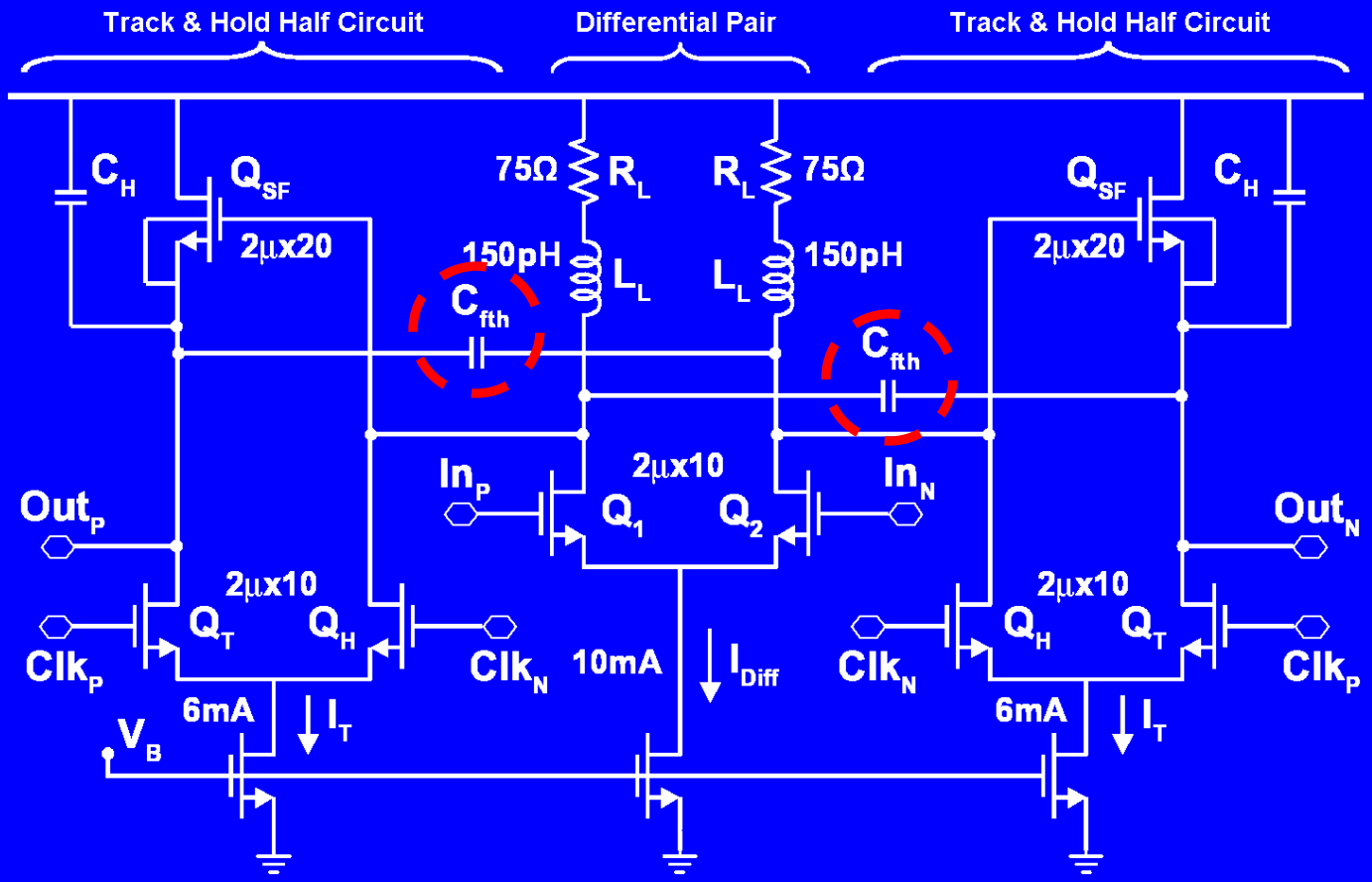
A linear buffer drives the T/H block with 600mV$_{PP}$ input and output swing



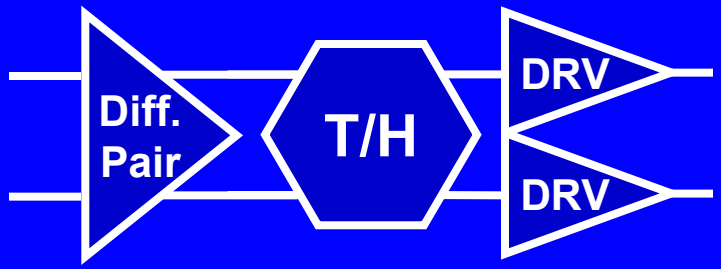
THA Stage Design



Capacitor C_{fth} is used to match $Q_{SF\text{-}CGS}$ and thus cancel input signal feedthrough during hold mode

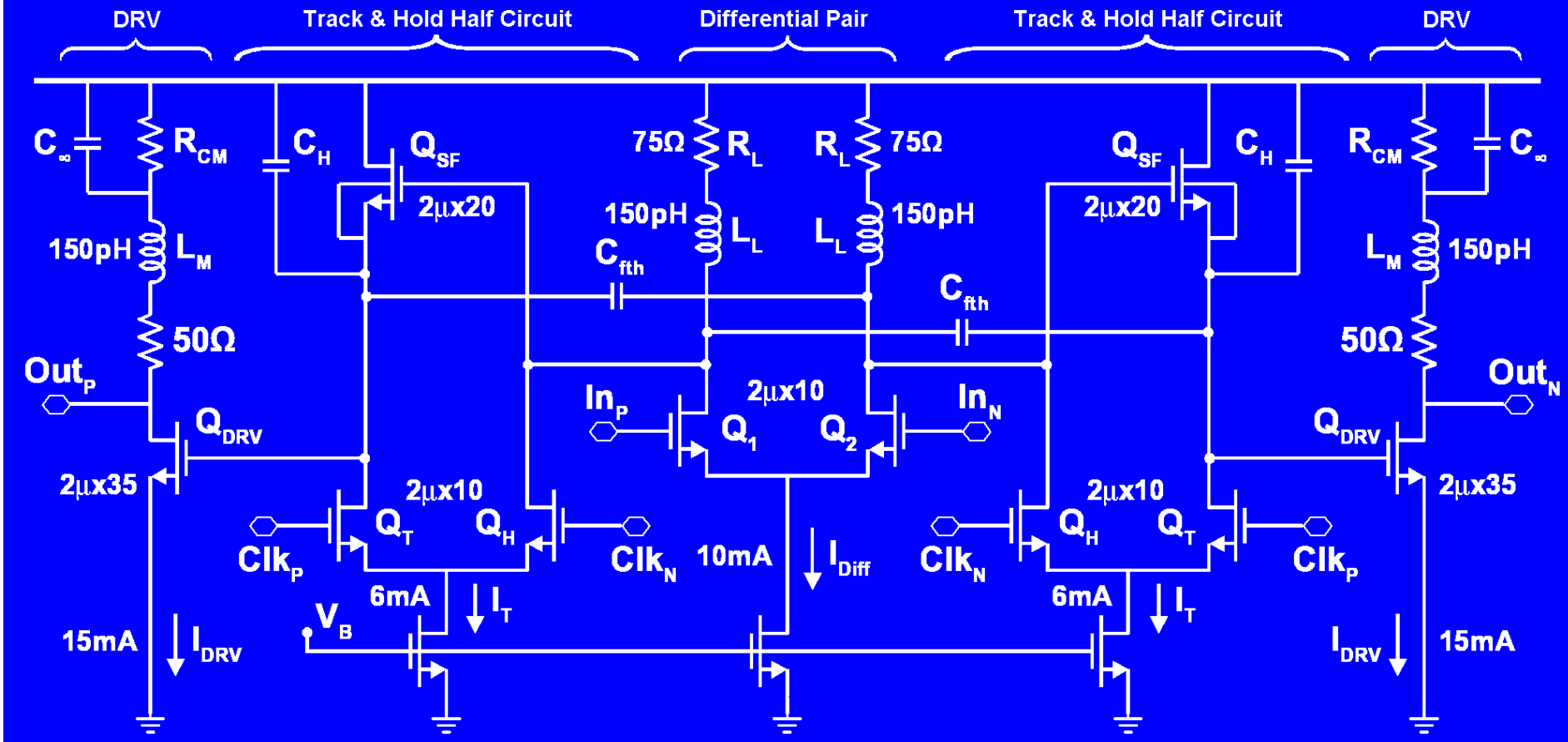


THA Stage Design



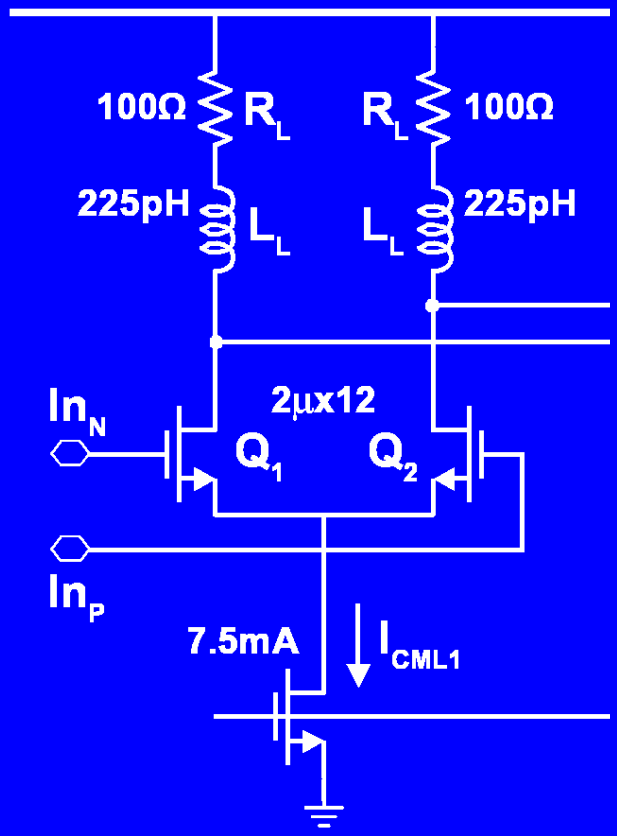
A linear output driver provides signal to external

50Ω resistors and measurement equipment



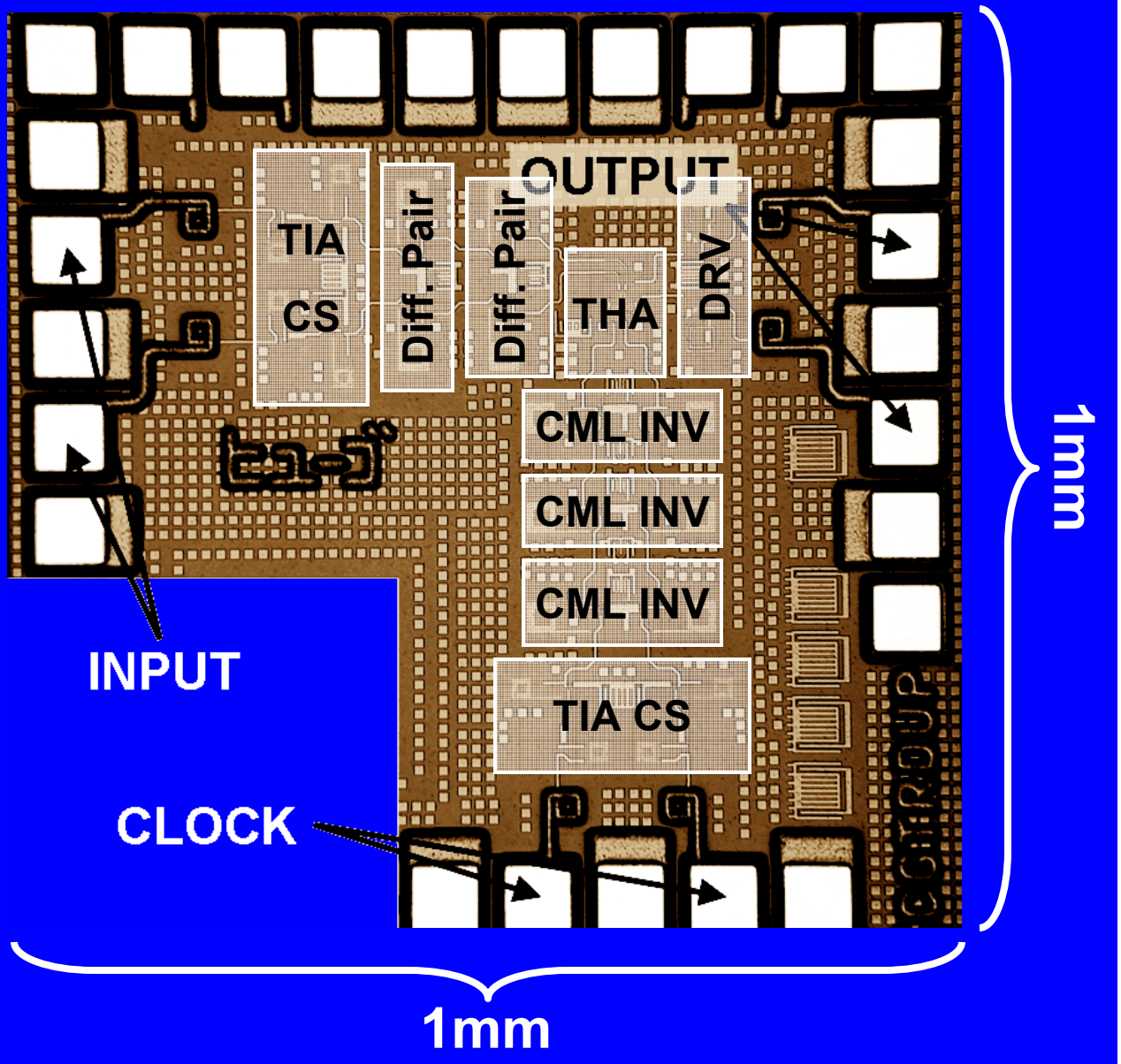
Clock Distribution

Converts a single-ended 30-GHz clock signal to a differential signal with 750mV$_{PP}$ swing

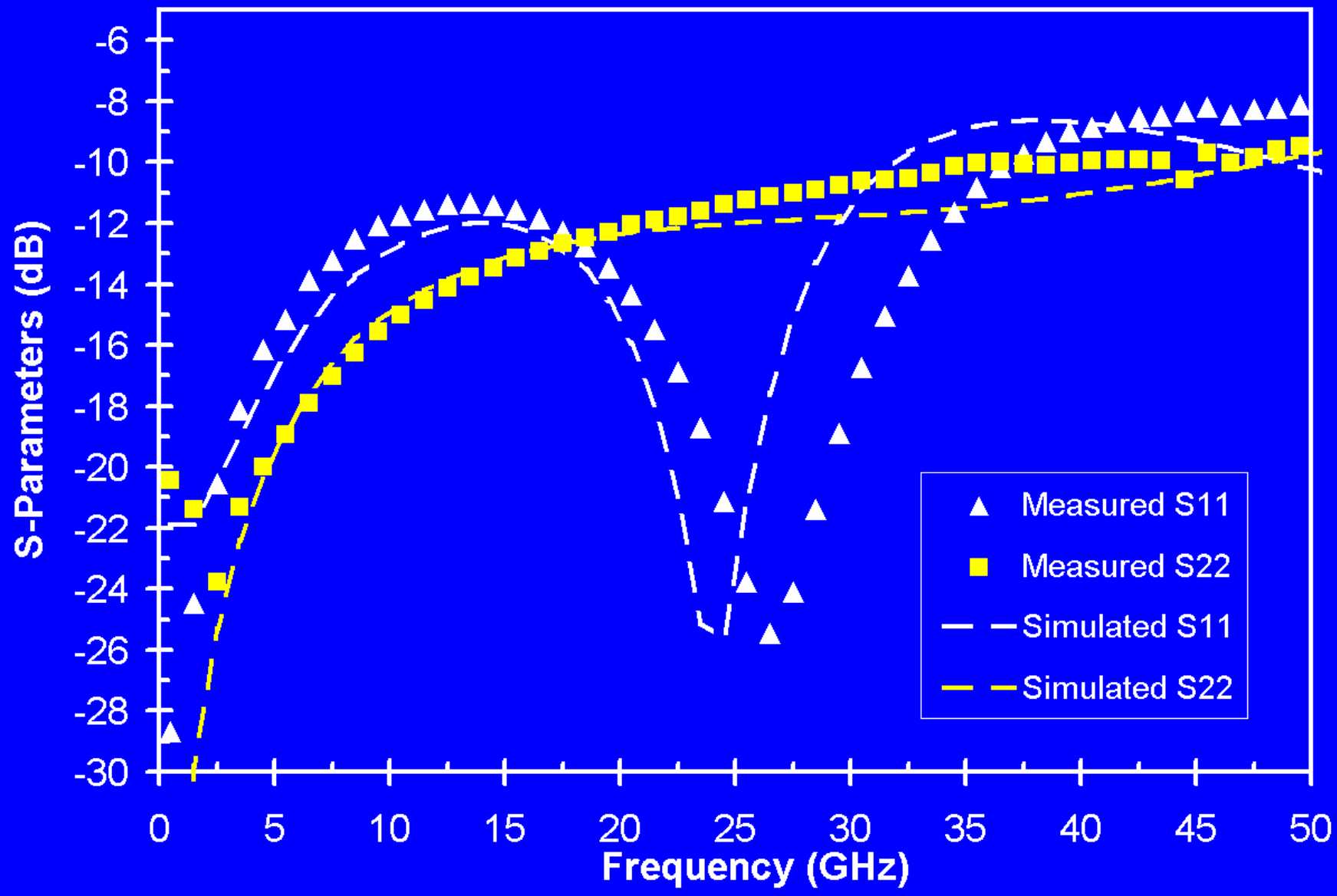


Chip Micrograph

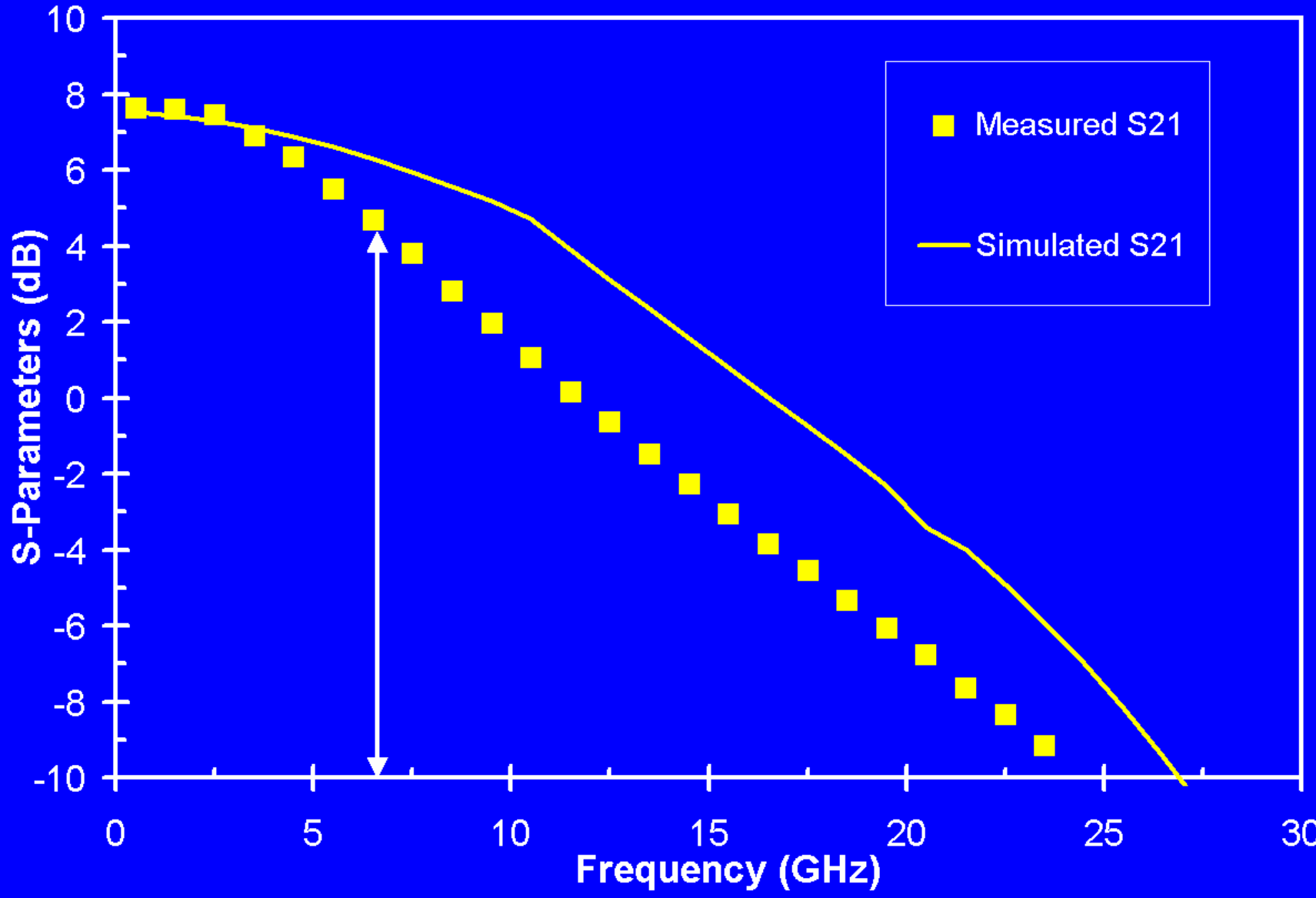
- Manufactured using IBM's 0.13µm CMOS technology
- The circuit operates from a 1.8V supply and consumes 150mA.



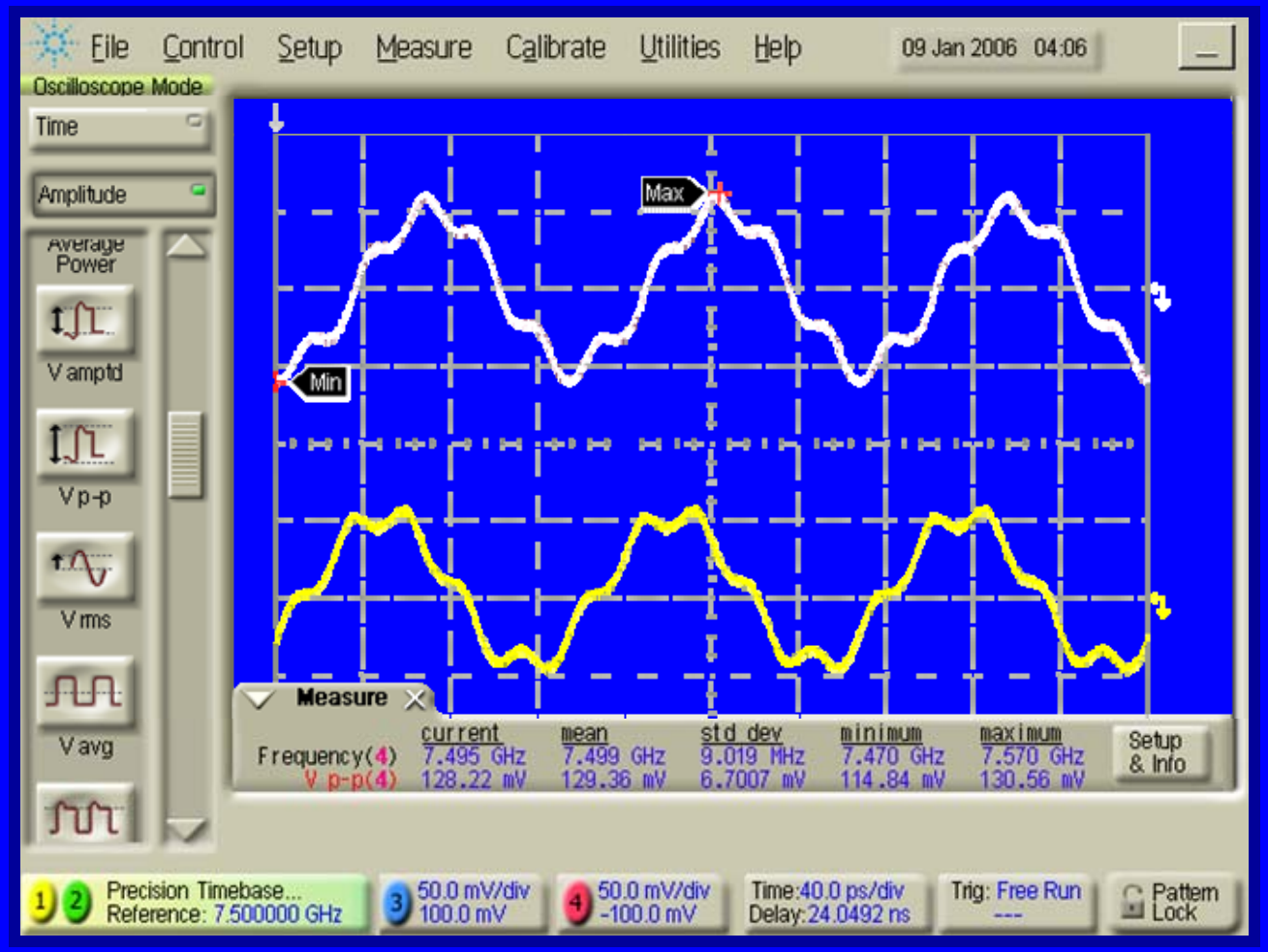
Measurement Results: SP



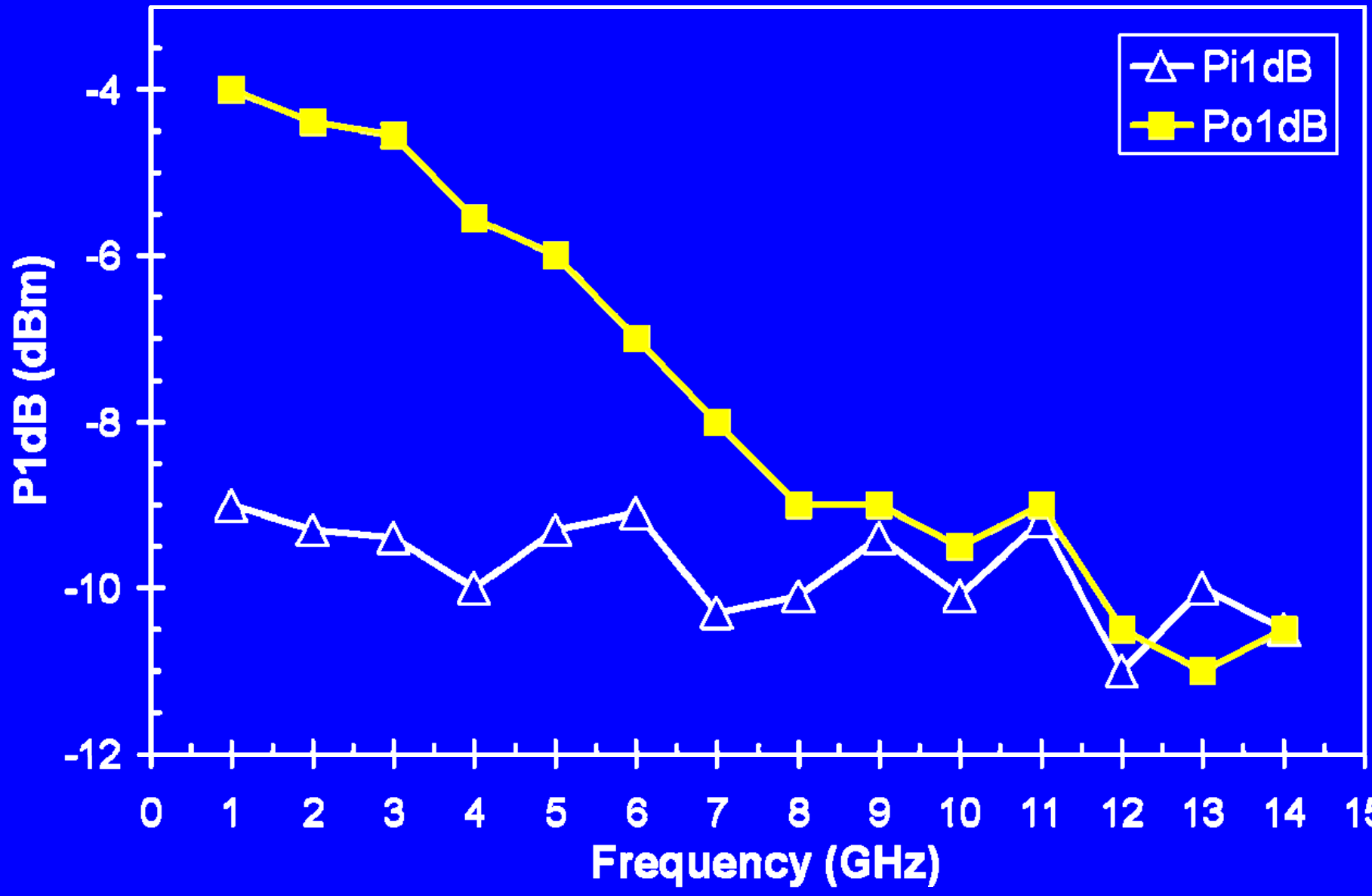
Measurement Results: SP II



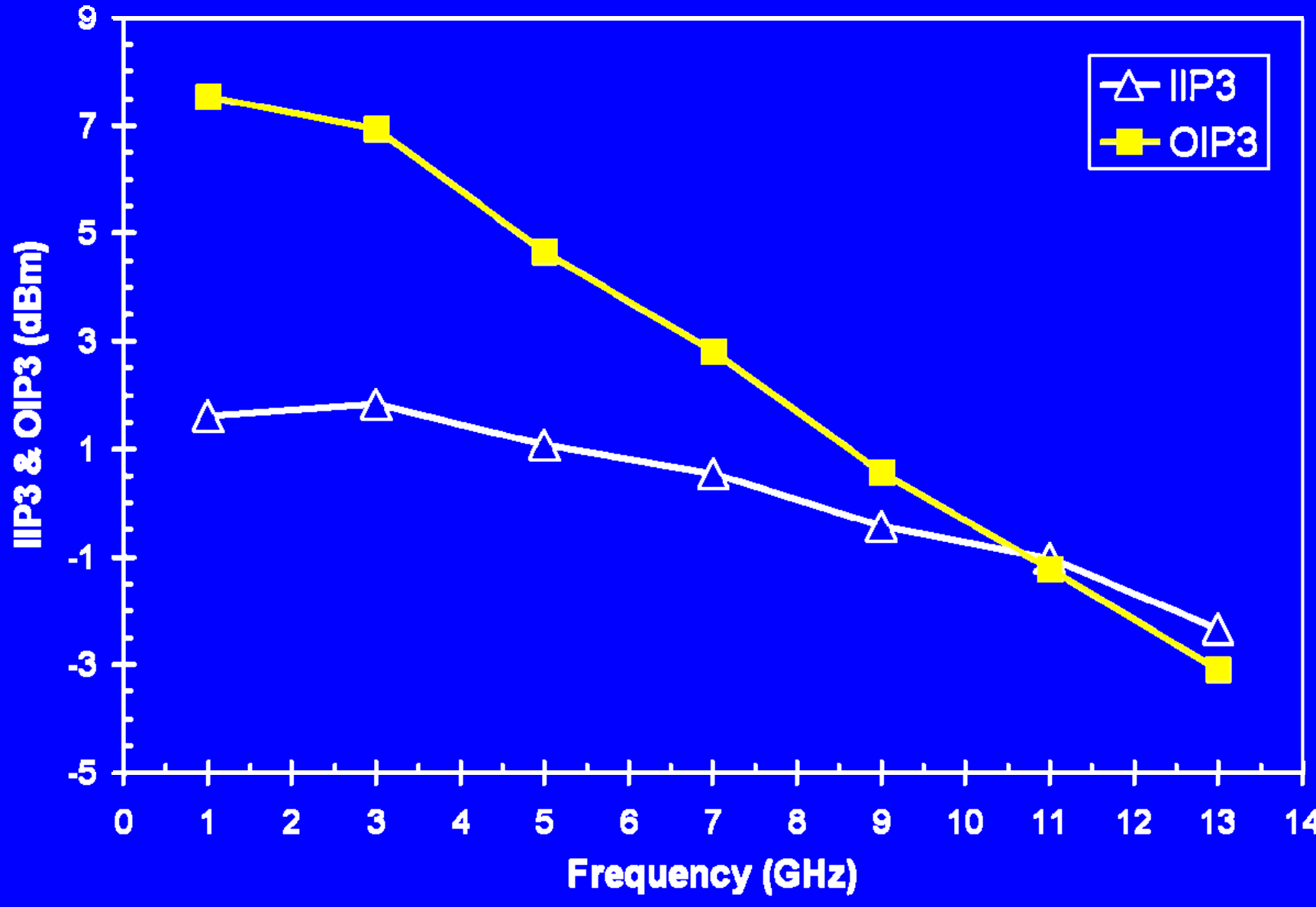
Time Domain


File Control Setup Measure Calibrate Utilities Help
09 Jan 2006 04:06
Oscilloscope Mode
Time
Amplitude
Average Power
Vamptd
Vp-p
Vrms
Vavg
Max
Min
Measure
current mean std dev minimum maximum
Frequency(4) 7.495 GHz 7.499 GHz 9.019 MHz 7.470 GHz 7.570 GHz
V p-p(4) 128.22 mV 129.36 mV 6.7007 mV 114.84 mV 130.56 mV
Setup & Info
Precision Timebase...
Reference: 7.500000 GHz
50.0 mV/div
100.0 mV
50.0 mV/div
-100.0 mV
Time:40.0 ps/div
Delay:24.0492 ns
Trig: Free Run
Pattern Lock

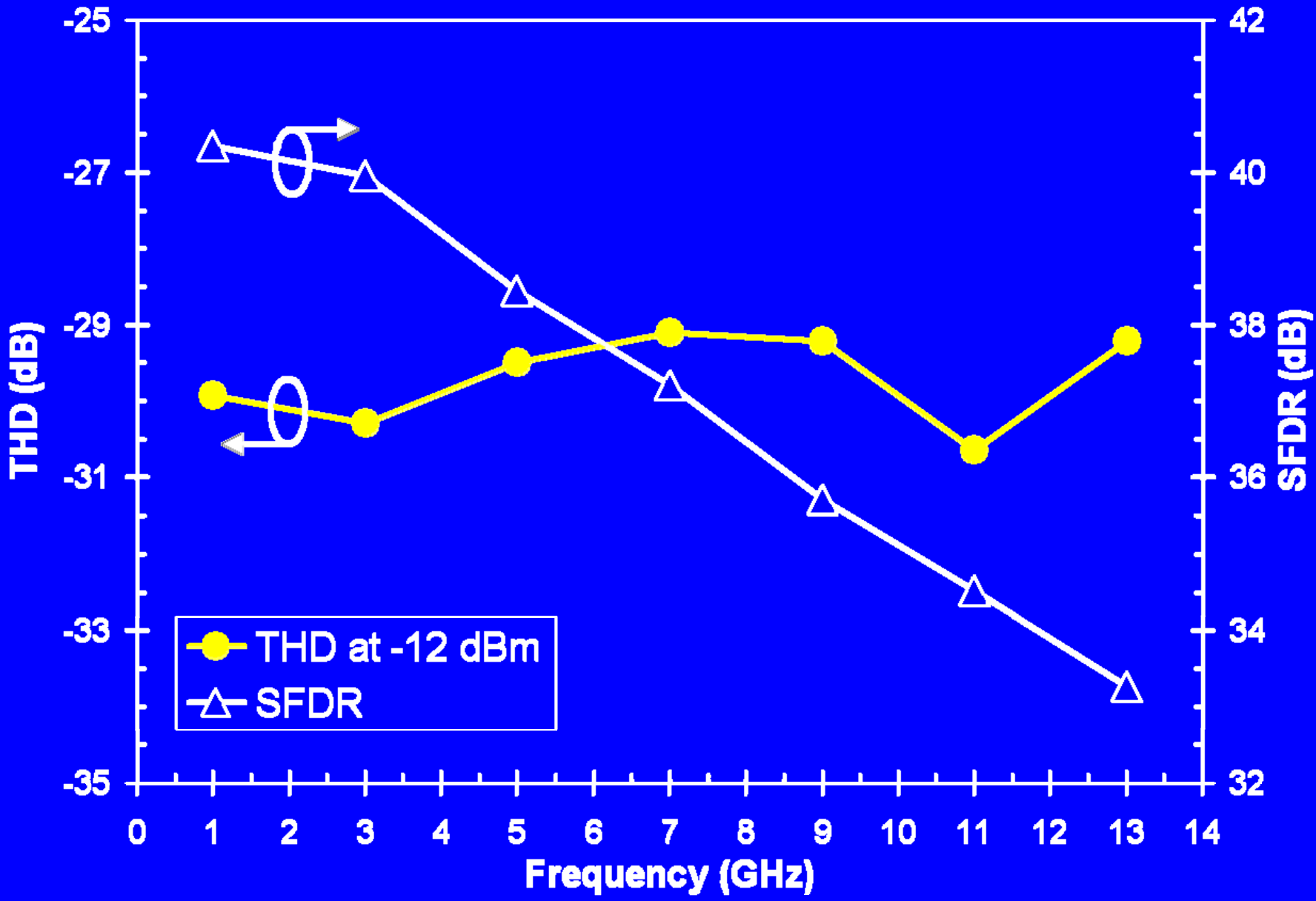
Frequency Domain I



Frequency Domain II



Frequency Domain III



Circuit Comparison

	f_{sample} [GS/s]	Track BW [GHz]	THD [dB @ f_{in}]	Supply [V]	Power [mW]	Process [N / f_T]
This Work	**30**	**7**	**-30 @ 1GHz -29 @ 7GHz**	**1.8**	**270**	**CMOS 0.13µm**
I. H. Wang el. al. Electronic Letters 06	10	N/A	-24.7 @ 5GHz	1.8	200	CMOS 0.18µm
J. Lee et. al. JSSC 03	12	14	-23.3 @ 12GHz	-5.2	390	InP 120 GHz
S. Shahramian et al. CSICS 05	40	43	-27 @ 20GHz -29 @ 10GHz	3.6	540	SiGe 160 GHz
Y. Lu et. al. BCTM 05	12	5.5	-52.4 @ 1.5GHz	3.5	700	SiGe 200 GHz

Conclusion

- CMOS emerges as a contender for high speed DSP based equalizers
- Discussed the design methodology for CMOS switched source follower THA
- Demonstrated the first 30-GS/sec THA in CMOS

Acknowledgement

- CMC for chip fabrication and providing CAD tools
- NSERC for financial support
- OIT and CFI for equipment
- ECIT for providing the network analyzer