A Delta-Sigma Modulator with a Widely Programmable Center Frequency and 82-dB Peak SNDR

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Abstract–A 4-bit fourth-order delta-sigma modulator with a widely programmable center frequency is presented. Novel methods for quantizing and implementing the digitally programmable modulator coefficients enable performance comparable to state-of-the-art discrete-time fixed-frequency modulators at any center frequency from dc to $0.31 f_s$ in steps of $0.0052 f_s$. The 0.18-μm 1.8-V CMOS prototype consumes 115 mW at a sampling frequency of 40 MHz. The peak SNDR and SNR over a 310-kHz bandwidth are 82 dB and 86 dB respectively.

I. INTRODUCTION

The trend in recent signal processing systems is to replace as many analog components with digital circuits as possible for reliability and portability and to take advantage of CMOS technology scaling. For example, Fig. 1(a) shows a typical digital radio receiver system with a bandpass analog-to-digital converter (ADC) followed by a digital quadrature down conversion mixer. Due to the fixed center frequency (f_c) of the bandpass ADC, such a radio receiver usually requires an oscillator with a variable frequency to place the signal band of interest within the passband of the ADC. A delta-sigma modulator with a variable f_c replaces the variable local oscillator with a fixed one [1] as shown in Fig. 1(b), and may allow the same modulator to be used for different intermediate frequencies (IFs) or applications.

Continuous-time bandpass delta-sigma modulators with analog tuning of the loop filter's resonant frequency have been reported in [2, 3]. Both are single-bit modulators requiring a high over sampling ratio (OSR) and high sampling frequency (f_s) to provide sufficient SNR and bandwidth. Hence, both were fabricated in non-CMOS technologies. Also, both have relatively narrow tuning range ($< 0.15 f_s$).

Little work has been done on discrete-time implementations of delta-sigma modulators with programmable center frequencies. Two implementations of programmable discrete-time modulators were reported in [4, 5]. Single-bit quantization and limited programmability of just a few modulator coefficients restricted these designs to narrow tuning ranges ($\leq 0.2 f_s$) and high OSRs (narrow bandwidths) for modest SNRs (< 60 dB).

In this work, a discrete-time multi-bit delta-sigma modulator with f_c programmable from dc to $0.31 f_s$ in steps of $0.0052 f_s$ is described. Architectural and circuit-level techniques to min-
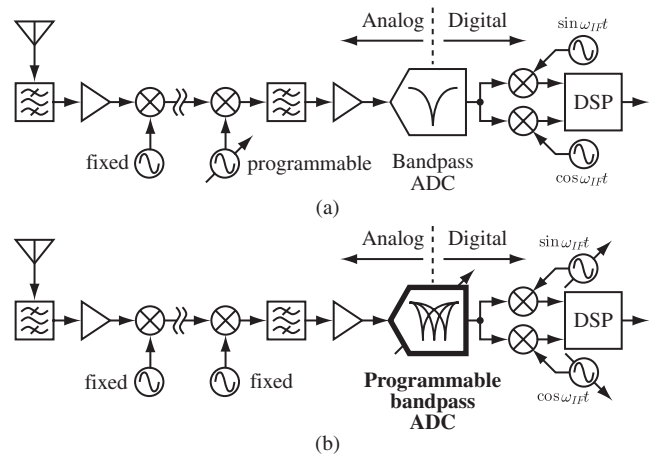

Fig. 1. (a) A typical digital radio receiver with a bandpass ADC and (b) a possible digital radio receiver with a bandpass modulator with a programmable center frequency.

imize the power and area overhead associated with this programmability will be described in sections II and III respectively. Despite the wide f_c tuning range, the modulator demonstrates performance competitive with that of recently reported discrete-time bandpass delta-sigma modulators with a fixed f_c. The 0.18-μm CMOS prototype consumes 115 mW from a 1.8-V supply at a sampling frequency of 40 MHz. The peak SNDR and SNR over a 310-kHz bandwidth are 82 dB and 86 dB respectively.

II. SYSTEM-LEVEL DESIGN

A. Modulator Architecture

In bandpass delta-sigma modulators, resonators are designed to provide a high loop gain for the band of interest and, hence, to attenuate quantization noise at frequencies around f_c. Therefore, f_c-programmability of a bandpass delta-sigma modulator can be achieved by varying the resonant frequencies of its resonators.

Although the resonant frequencies can be controlled by adjusting just one or two gain settings in each resonator, this approach is only suitable when adjusting f_c over a narrow range and for modest SNRs, as in [4, 5]. In order to maintain excellent dynamic range over a wide range of center frequencies, it is necessary to perform dynamic range scaling at each f_c setting. Hence, in this work all of the modulator coefficients are
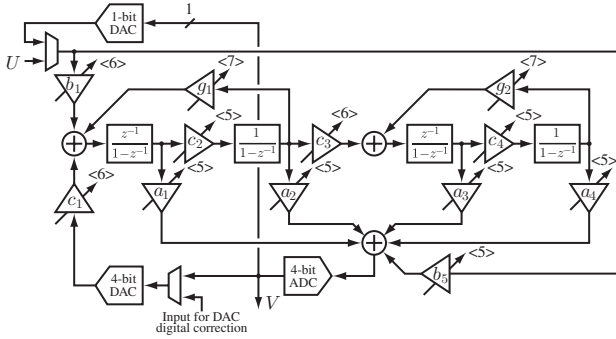
Fig. 2. The programmable delta-sigma modulator architecture.

Fig. 3. Modulator coefficients after quantization.

programmable to maintain reasonable signal swings throughout the loop filter for all possible f_c settings.

The modulator coefficients are programmed using banks of digitally switchable unit capacitors. The number of unit capacitors in each bank determines the resolution of the corresponding coefficient. In order to accurately set the noise transfer function (NTF) pole and zero locations and perform dynamic range scaling, and hence achieve the best possible signal-to-quantization noise ratio (SQNR), high resolution modulator coefficients are required. However, increasing the coefficient resolution results in a larger capacitor banks and, hence, more silicon area and power dissipation. Therefore, the resolution of the modulator coefficients should be made as low as possible while still maintaining the performance of the modulator. This was a primary consideration in choosing a modulator topology.

Providing an input feed forward path directly to the quantizer can eliminate input signal components from the loop filter, thus improving the modulator's linearity [6]. This approach can be applied to modulators with either the cascade of resonators with feedback (CRFB) topology or the cascade of resonators with feed forward (CRFF) topology. In either case, it is desirable to maintain a flat signal transfer function (STF) so that out-of-band interferers do not overload the modulator. However, compared with the CRFF topology, the CRFF topology requires fewer switched capacitor banks to maintain a flat STF while still having the improved linearity offered by the additional input feed forward path. Therefore, this work employs the CRFF topology with input feed forward, as shown in Fig. 2. This is in contrast to prior programmable discrete-time implementations which employed a CRFB topology without input feed forward [4, 5].

B. Optimization of Quantized Coefficients

A straightforward approach to quantizing the coefficients of a delta-sigma modulator would be to perform the optimization assuming full precision in the coefficients, then round each coefficient to the nearest quantized level. However, if the finite precision of the modulator coefficients is taken into account while performing the optimization, better accuracy in setting the NTF can be obtained.

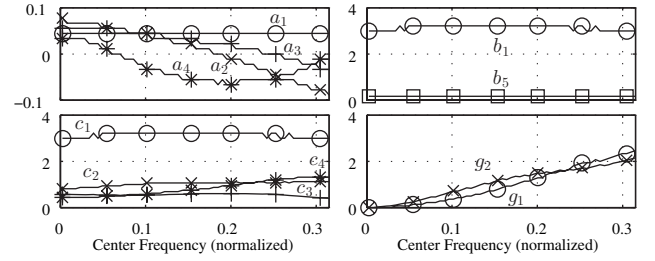The resonant frequencies of the resonators in Fig. 2 are,

$$\omega_{r1} = \tan^{-1}\left(\frac{4c_2g_1 - c_2^2g_1^2}{2 - c_2g_1}\right) \quad (1)$$

$$\omega_{r2} = \tan^{-1}\left(\frac{4c_4g_2 - c_4^2g_2^2}{2 - c_4g_2}\right) \quad (2)$$

Hence, each resonant frequency depends only on the product of two coefficients: c_2g_1 and c_4g_2. The modulator's SQNR is particularly sensitive to the NTF zero locations, which are determined by ω_{r1} and ω_{r2}. Hence, it is simply necessary for the products c_2g_1 and c_4g_2 to be close to the products of the optimal (full-precision) coefficient values. This observation can be used to reduce the resolution of one of the quantized coefficients. Specifically, c_2 and c_4 are quantized coarsely (5 bits). Then, error terms are added to g_1 and g_2 that take into account the quantization errors in c_2 and c_4. Finally, g_1 and g_2 are quantized with a higher resolution (7 bits). The numbers inside angled brackets in Fig. 2 indicate the resolution of each coefficient in bits, and Fig. 3 shows the optimized coefficient values versus f_c after quantization.

C. DAC Nonlinearity Compensation

Although dynamic element matching (DEM) is a popular technique for the compensation of the DAC nonlinearities in multi-bit delta-sigma modulators, it's application to a modulator with f_c- programmability would be complicated by the need to tune the DEM transfer function for different values of f_c. Therefore, the digital correction technique described in [7] for off-line calibration of a multi-bit DAC was employed instead. This technique requires the DAC nonlinearities to be linearly measured off-line. Then, the DAC nonlinearities can be canceled digitally at the output of the modulator during the normal operation [7].

For this modulator, off-line measurement of the DAC can be performed by reconfiguring the original modulator as a second order single-bit delta-sigma modulator, which is inherently linear. The input is then driven by the multi-bit feedback DAC output [8]. Since the modulator must be highly reconfigurable to accommodate f_c-programmability anyway, this facility is implemented with very little overhead.

III. CIRCUIT DESIGN

The SC representation of the modulator is shown in Fig. 4. The first four OTAs form four SC integrators arranged into two SC resonators. The last OTA and its SC branches add the feedforward signals from the integrators and the modulator input to-
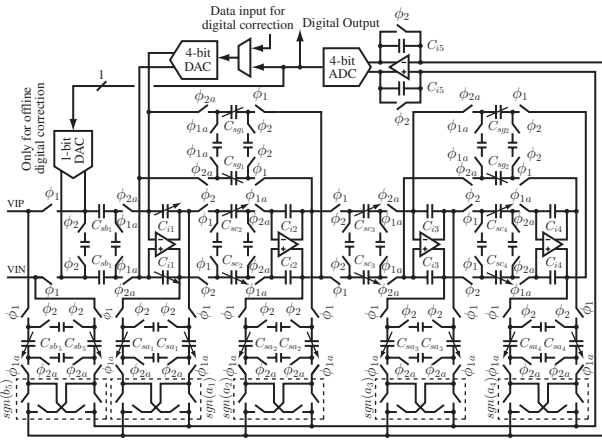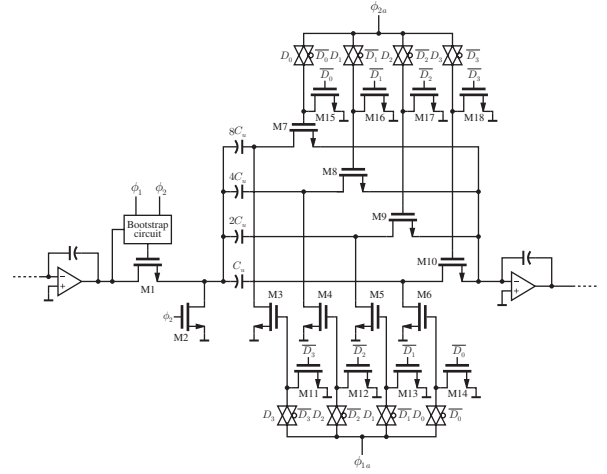
Fig. 4. SC representation of the modulator.

Fig. 5. Simplified schematic of the programmable integrator.

Fig. 6. Die photo of the modulator.

gether. The sum is passed to the 4-bit flash ADC. The digital output of the ADC is fed back to the 4-bit SC DAC.

Except for the first integrator, the sampling capacitors were made programmable, thus providing linear control of the coefficients. In the first integrator, the SC multi-bit DAC and the input sampling capacitor C_{sb_1} strongly influence the overall SNR. Hence, the integrating capacitor C_{i_1} was made programmable instead to avoid impacting those components. All capacitors are metal-insulator-metal (MiM) structures.

A. Thermal Noise

Programming the modulator coefficients involves changing the sizes of switched-capacitors. Doing so affects the modulator's input-referred thermal noise and the SNR. Therefore, the input referred thermal noise has to be analyzed for all possible f_c to ensure sufficient SNR.

The dominant contributors to the input referred thermal noise are the first resonator and the SC multi-bit DAC. The in-band input-referred thermal noise contributed by the other components is negligible due to the high gain of the first resonator. The input referred noise contributed by the first resonator and the SC DAC can be expressed as

$$\overline{e_i^2} = \frac{4kT}{\text{OSR}} \left(\frac{1}{C_{sb_1}} + \frac{\sum C_d}{C_{sb_1}^2} + \frac{C_{sg_1}}{C_{sb_1}^2} + \frac{1}{b_1^2 C_{sc_2}} \left| 1 - e^{-j2\pi f_c} \right|^2 \right),$$

(3)

where C_{sx_n} are the values of the sampling capacitors corresponding to the coefficients x_n, and C_d is the unit capacitor size of the DAC. The input referred noise increases with f_c mainly due to accompanying increases in C_{sg_1} (which is proportional to g_1) and $\left| 1 - e^{-j2\pi f_c} \right|$. This analysis is used to size the capacitors whose ratios correspond to the modulator coefficients obtained in the previous section.

B. Programmable Integrator

A simplified single-ended version of a 4-bit programmable integrator is shown in Fig. 5. It utilizes a binary weighted capacitor bank with gated clock signals that select which capacitors to charge and discharge. This structure provides a digitally programmable SC without placing additional MOS switches in series with the capacitors. Therefore, the programmability does
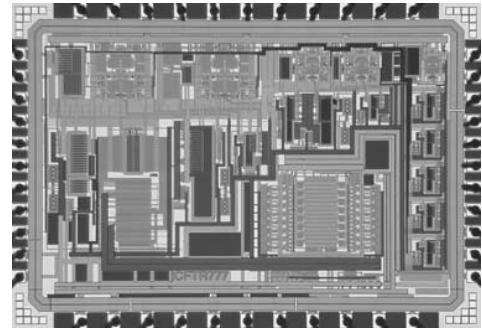
not increase the RC time constants of the switched-capacitor circuits.

Compensating two-stage OTAs would have been difficult since their load capacitances change dramatically for different values of f_c. Therefore, all five OTAs are single-stage fully-differential PMOS-input folded-cascode OTAs. The first four OTAs have gain enhancement circuits.

C. Multi-bit ADC and DAC

The ADC is a standard 4-bit flash ADC with dynamic comparators. The feedback DAC is a 4-bit SC DAC that uses the same OTA as the first integrator. The total capacitance of the DAC is 4.5 pF per side.

IV. EXPERIMENTAL RESULTS

The modulator (including the pad frame) occupied 4.5 mm^2 in a 1P6M 0.18-μm CMOS technology. Fig. 6 shows a die photo of the modulator. The f_c programmability is demonstrated in Fig. 7 which plots the filtered output spectra obtained for different f_c settings with zero input. As expected from the thermal noise analysis, the in-band noise floor of the output increases as f_c is increased.

Fig. 8 shows the SNR versus the input amplitude for all possible center frequencies. The SNR saturates at high input amplitudes because it is limited by noise from the signal generator. The SNR did not saturate for $f_c = 0$ Hz since a better (low-frequency) signal generator was used for that test. Therefore, a
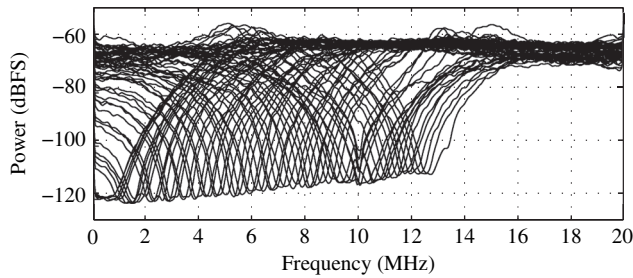
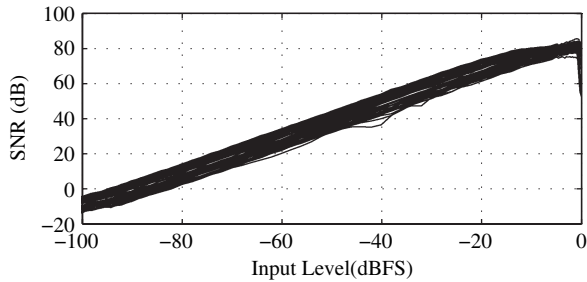Fig. 7. Filtered zero-input output spectra of the modulator for all possible f_c.

Fig. 8. SNR versus the input amplitude for all possible f_c.

Fig. 9. Measured peak SNDR, SNR, IMD, and DR over f_c.
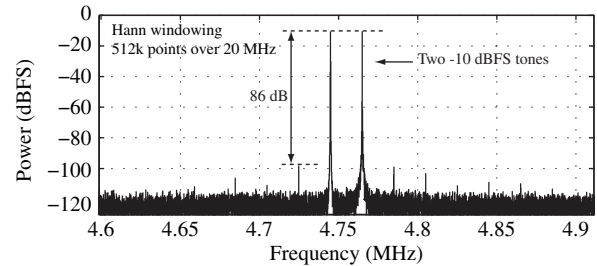
Fig. 10. Measured output spectrum for f_c=4.78 MHz.

peak SNR of 86 dB was obtained for $f_c = 0$ Hz.

Fig. 9 shows the measured peak signal-to-noise and distortion ratio (SNDR), SNR, intermodulation distortion (IMD), and dynamic range (DR) for each f_c. The SNR and DR were measured with a single-tone input. For $f_c = 0$, the SNDR and was also measured with a single-tone input. For bandpass configurations, the SNDR and IMD were measured with a two-tone input signal. The peak SNDR was observed with two -10-dBFS input tones, so IMD was measured with that same input level. Fig. 10 shows the output spectrum obtained from one of the two-tone tests.

V. CONCLUSIONS

Table I compares this work with recently reported fixed-f_c discrete-time bandpass delta-sigma modulators. It shows that this work offers comparable performance despite the wide programming range of f_c.

Furthermore, since all of the modulator coefficients are programmable it is possible to exercise independent control of the NTF zeros. Hence, although not yet tested, this modulator should also operate efficiently for lower OSRs by optimizing the NTF zero locations. With f_c programmable all the way down to dc, this modulator could be useful for digital wireless receiver applications, and many others.

TABLE I
COMPARISON WITH RECENT FIXED-f_c DISCRETE-TIME BANDPASS
DELTA-SIGMA MODULATORS

	f_s	f_c	BW	SNDR	SNR	DR	IMD	P
	(MHz)	(MHz)	(kHz)	(dB)	(dB)	(dB)	(dBc)	(mW)
This work	40	0-12.6	310	82-71	86-75	93-76	-(90-73)	115
[9]	37.05	10.7	200	-	72	78	-65	88
[10]	42.8	10.7	200	61	-	74	-75	76
[11]	80	20	270	78	80	86	-	24

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