8.2 A 6.8mW 7.4Gb/s Clock-Forwarded Receiver with up to 300MHz Jitter Tracking in 65nm CMOS

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High density multilink interfaces such as QPI and HyperTransport include a dedicated link to carry a synchronous clock from the transmitter to receiver and shared by 5 - 20 data transceivers. Sub-rate clocks ameliorate jitter amplification in lossy channels. The forwarded clock must be frequency-multiplied and aligned with the data at each receiver. Per pin deskewing is done at startup [1]; the optimum deskew setting is stored and the calibration circuitry turned off during normal operation. Jitter on the forwarded clock is correlated with jitter on the data because both are generated by the same transmitter. Hence, jitter tolerance is improved by retiming the data with a clock that tracks correlated jitter on the forwarded clock [2]. However, since the delay of the data and clock paths typically differ by several UI, very high frequency jitter will appear out-of-phase at the receiver and should not be tracked. For a delay mismatch of L UI between clock and data, jitter tolerance is improved by tracking jitter up to $f_{bit}/4L$ [2]. If the mismatch is 5UI, at 4Gb/s and 8Gb/s the clock path jitter tracking bandwidth (JTB) should be 200MHz and 400MHz respectively. In summary, the clock path in a clock forwarded transceiver should provide flexible clock multiplication, a controlled phase shift, and a JTB adjustable over 100's of MHz to accommodate different channel losses, bit rates, and path delay mismatches.

A PLL can provide clock multiplication [3], but its limited bandwidth filters out useful correlated jitter [4]. A MDLL is allpass, tracking both correlated and uncorrelated jitter. Injection locked oscillators (ILO) are a power- and area-efficient alternative to PLLs and DLLs. In [5,6] an ILO performs both jitter filtering and clock deskew by introducing a frequency offset between the ILO's free-running frequency and the injected frequency. With this simple architecture the jitter tracking bandwidth is a strong function of the phase deskew setting, and clock multiplication is not performed. In [7] a MDLL provides clock multiplication and generates a multi-phase clock output; a ILO is used to interpolate between the coarse MDLL skew settings and filter out high frequency periodic jitter generated in the MDLL. Since only one jitter filter appears in the clock path, a low JTB is required to efficiently filter the high frequency periodic jitter, but that also filters out correlated jitter on the forwarded clock. Moreover, compared to a DLL-only or ILO-only solution, the MDLL-ILO architecture consumes more power.

This work combines a frequency-multiplying injection locked oscillator (MILO) and per pin local injection locked oscillators (LILO) as in Fig. 8.2.1. A single MILO shared by all receivers provides both clock multiplication and an adjustable JTB. The LILO provides per pin clock deskew and additional filtering of very high-frequency jitter. A 3-stage ring oscillator is used as the MILO with a 1.7 to 4.5GHz tuning range. Transistors M_3 serve as a cross-coupled common-gate clock buffer providing a 200mV clock swing across 1mm of on-die transmission line to the LILO. Inductor L_1 provides low Q bandpass filtering to reduce high frequency jitter. If injected with a sub rate (quarter-rate or lower) clock, significant amplitude distortion and reference spurs appear at the MILO output. This problem is ameliorated by injecting a pulse train. Unlike NRZ signals, pulse trains effect the MILO output only at their transitions. As a result, amplitude distortion and frequency spurs are significantly reduced. Pulse trains are simply generated using a delay and XOR gate integrated into the clock transmitter of this prototype link (Fig. 8.2.1). The MILO JTB is set by the effective injection strength which is controlled by changing the pulse repetition rate and duty cycle thereby providing continuous adjustment of the JTB from 25MHz to 300MHz. The shared clock circuitry consumes more power than any other block in the link to ensure that even when set to a low JTB, a low phase noise clock is distributed to the LILOs.

Low swing passive clock distribution is used due to its low latency, supply noise immunity and reduced power consumption. This distributed clock is injected to the LILO to further filter high frequency jitter and provide a deskewed clock to the data samplers (Fig. 8.2.2). The 4-stage ring oscillator used as the LILO has both coarse and fine tuning. Using the coarse tuning, all LILOs are frequency-locked to the distributed clock. However, due to mismatch there will be small frequency offsets between the LILOs which are compensated with the fine controls during phase deskew. Existing ILO-based deskew circuits use frequency offset to control phase shift. Unfortunately, jitter tracking bandwidth also decreases with frequency offset. Thus for large phase shifts, correlated jitter is filtered and the ILOs self phase noise increases recovered clock jitter. Instead we inject the clock into the ring at two points with adjustable polarity and three possible injection strengths to select between 8 coarse deskew settings (Fig. 8.2.3). Interpolation between these coarse settings is done by slightly detuning the LILO's free-running frequency. Since only small frequency offsets are required to achieve ±23° phase shifts, high JTB can be maintained. The LILO's JTB exceeds 600MHz so that the overall JTB of the clock path is determined by the MILO, independent of the phase deskew setting. Moreover, with such high JTB very little of the LILO's self phase noise appears in the recovered clock. Very high frequency jitter due to DCD and reference spurs is attenuated by both ILOs. CML delay stages are used in both the MILO and LILO providing good supply noise immunity.

The 4-7.4Gb/s 65nm CMOS prototype is tested in a QFN package and operates from a 1V supply. It incorporates a programmable passive equalizer to provide up to 5dB of boost at one-half the bit rate. The shared clock circuitry consumes 8mW, the LILO phase interpolator consumes 4.4mW and the samplers consume 2.4mW. Excluding shared clock power, each receiver consumes 6.8mW which equals 0.92pJ/bit at 7.4Gb/s. The BER of the receiver for a 2^{31}-1 pattern is shown in Fig. 8.2.4 as a function of deskew setting over 5" FR4 interconnect. Jitter tolerance is tested at 7.4Gbps; BER is less than 10^{-12} with .45UIpp DJ in addition to 1.5UIpp sinusoidal PJ at 200MHz (Fig. 8.2.5). The proposed architecture is compared with state-of-the-art receivers in Fig. 8.2.6. The proposed solution combines the functionality of PLL- or DLL-based solutions without sacrificing the excellent power- and area-efficiency offered by injection locking. The high-frequency jitter tolerance achieved (1.5UI at 200MHz) is comparable to oversampling CDRs, a significant improvement over previous low-power clock forwarded receivers.

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References:
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[4] A. Agrawal, P. Hanumolu and G. Wei, "A 8x5 Gb/s Source-Synchronous Receiver with Clock Generator Phase Mismatch Correction," *Custom Integrated Circuits Conference*, San Jose, California, September 2008
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[6] K.Hu et al. "A 0.6mW/Gbps,6.4-8.0Gbps Serial Link Receiver Using Local Injection-Locked Ring Oscillators in 90nm CMOS", *VLSI Circuits Symposium, Kyoto, Japan*, June 2009
[7] Farjad-Rad et al., "A 33mW 8Gb/s CMOS Clock Multiplier and CDR for Highly Integrated I/Os", *IEEE J. Solid-State Circuits*, vol. 39, pp1553-1561, Sep., 2004.

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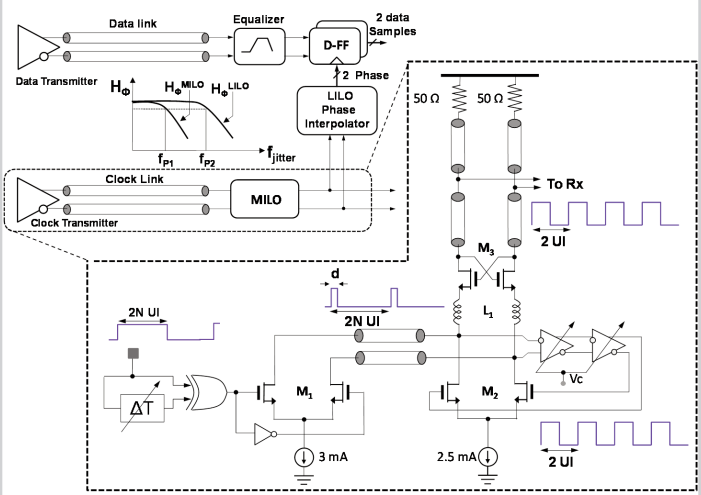


Figure 8.2.1: Forwarded clock receiver architecture in 65nm CMOS. The clock transmitter and frequency-multiplying injection locked clock multiplier (MILO) are elaborated in the figure.

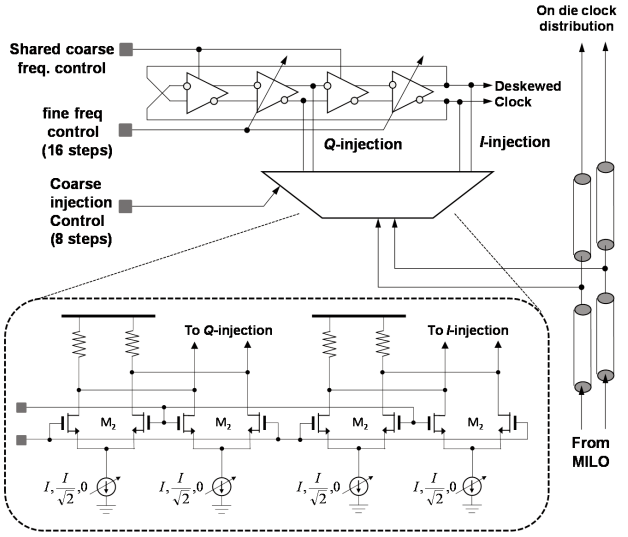


Figure 8.2.2: The local injection locked oscillator (LILO) using a 4-stage ring. The clock injection stage providing coarse deskew control is inset.

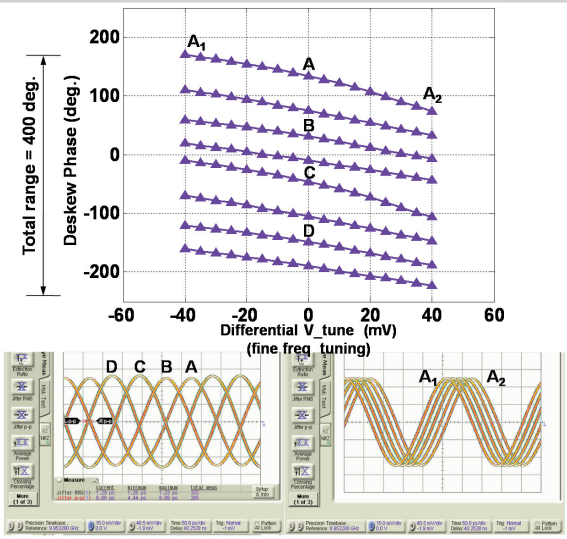


Figure 8.2.3: Measured deskew with coarse and fine control. Four coarse and fine deskewed phases are at the bottom.

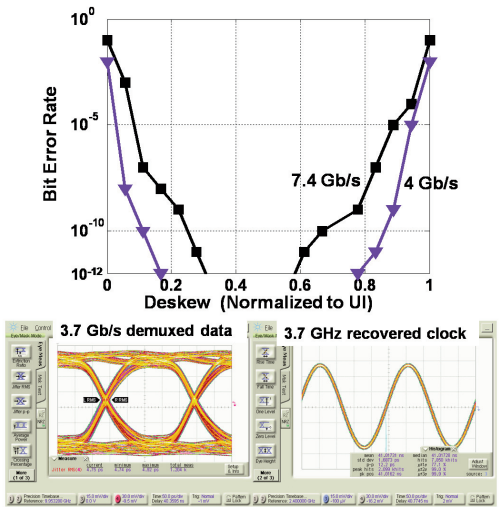


Figure 8.2.4: BER as a function of phase deskew at 4Gb/s and 7.4Gb/s over 10" and 5" FR4 traces respectively for 2^{31}-1 pattern. Demuxed data and recovered clock are at the bottom.

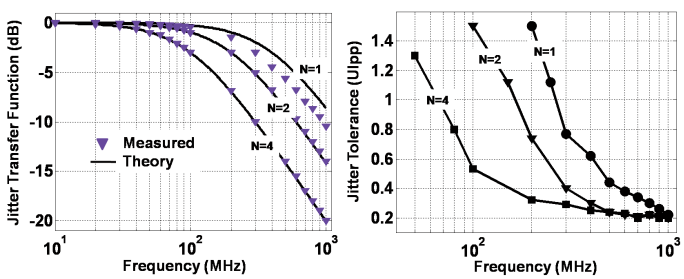
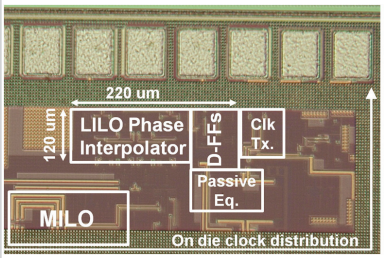


Figure 8.2.5: JTF and Jtol at different jitter tracking bandwidth settings. The forwarded clock pulse is at a frequency 1/2N-th the data rate. Jitter tolerance is measured in the presence of an additional 0.45UIpp DJ (5" FR4 channel) at 7.4 Gb/s.

	[3]	[4]	[5]	[6]	[7]	(This work)
Architecture	PLL-PI	DLL	ILO	ILO	MDLL-ILO	MILO-ILO
Data Rate	6.25Gb/s	5Gb/s	27Gb/s	7.2Gb/s	8Gb/s	7.4Gb/s
Clock Multiplication Ratio	16x	1x	1x	1x	1x,2x,4x,5x, 8x,10x	1x,2x,4x,8x,16x
Clock frequency	½-rate	¼-rate	½- rate	¼-rate	¼-rate	½-rate
Ref. Spur	------	-----	---------	---------	-32 dBc	-41.5 dBc
Clock Jitter (ps rms)	------	-----	---------	1.4 —3 ps	1.8—6.6 ps	1.4 ps(N=1) 4 ps (N=16)
Jitter Tracking BW	------	All pass	100MHz-750MHz (varies w/ skew)	30MHz -100MHz	------	25MHz-300MHz
Jitter tolerance (UIpp)	--------	0.72UI @ 15MHz 0.3UI @ 100MHz	--------	--------	--------	1.5UI@ 200MHz
Technology	90nm	0.13um	45nm	90nm	0.13um	65nm
Area	0.153 mm²	0.157 mm²	0.015 mm²	0.017 mm²	0.08 mm²	0.03 mm²
Rx Power	8.2mW	32.25mW	43mW	4.3mW	33mW	6.8mW
CMU Power	3.6mW	-----	------	------	0	4mW (+4mW tx)
FOM (pJ/bit)	1.31	6.45	1.6	0.6	4.125	0.92

Figure 8.2.6: Comparison with state-of-the-art low-power clock forwarded receivers.



	Area (mm^2)	Power (mW)
Clock Tx	.005	4
MILO (CMU)	.025	4
Passive Eq	.006	0
LILO (Deskew)	.020	4.4
D-FF (Samplers)	.008	2.4

Figure 8.2.7: Die photo of the implemented 65 nm CMOS receiver with area and power breakdown.

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