Analogue adaptive filters: past and present

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Abstract: Analogue adaptive filters represent an important niche in adaptive-filter theory and practice. The paper provides an overview of the field. Important adaptive algorithms, filter structures, circuit techniques and applications are all discussed. Considerable attention is paid to historically significant developments which have provided a foundation for modern analogue adaptive filters. Future directions are also surmised.

1 Introduction

Filters are general signal processing blocks used in virtually every modern electronic system. Whenever a filter's parameters must track poorly-controlled or time-varying conditions, adaptive filters are an attractive option. At low speeds, adaptive filtering is easily and efficiently performed using digital circuits. On the other hand, analogue filters are preferable at high speeds when low power consumption, small integrated area, and moderate linearity are required. As digital logic continues to shrink and increase in speed, the minimum speed at which analogue signal processing becomes beneficial increases. At present, the vast majority of adaptive filters are implemented digitally and a wealth of literature has been published on the topic [1]. This paper provides an overview of analogue adaptive filters which represent an important niche in adaptive filter theory and practice. The focus is on filters suitable for high-speed applications where they will continue to be an important part of systems for years to come. At the same time, attention has been paid to historical developments which may no longer be of practical use, but which provided a foundation for the development of techniques in use today.

The designer of a modern analogue adaptive filter is required to simultaneously consider both system- and circuit-level issues. However, to provide this paper with some logical organisation, a top-down approach is used. Specifically, the reader is first introduced to the algorithms and filter structures used in analogue adaptive filters. Next, the circuit techniques required to implement these algorithms and structures are discussed in Section 4. Consideration is then given to specific applications where analogue adaptive filters are currently used. Finally, future directions are surmised in the conclusion.

2 Adaptive algorithms

This Section will focus on the mechanisms by which analogue filters can adapt to optimise their performance in an unknown and possibly time-varying environment. Specifically, consider a completely general analogue filter (continuous-time or discrete-time) with N variable parameters $\boldsymbol{p} = [p_1\ p_1\ \ldots\ p_N]^T$. Let ε denote an error function used to quantify the filter's performance. The error ε will be smallest when the filter parameters are equal to their optimal values $\boldsymbol{p}^*$. Therefore, the problem is to search $\Re^N$-space over all possible combinations of filter parameters $\boldsymbol{p}$ to find the minimum value of $\varepsilon(\boldsymbol{p})$. In this general formulation, filter adaptation is seen to be nothing more than a classical optimisation problem for which a myriad of possible algorithms has been developed. For example, there are adaptive lattice algorithms [2–4], the recursive least squares algorithm [5, 6], and algorithms based on hyperstability [7–10], simulated annealing [11], genetic optimisation [12, 13], and random [14] or linear [15, 16] searches of $\Re^N$-space. However, these algorithms are primarily reserved for digital adaptive filters. Currently, only two main approaches are widely used for the adaptation of analogue filters: least-mean-square (LMS) algorithms and heuristic algorithms. This Section focuses on these two approaches.

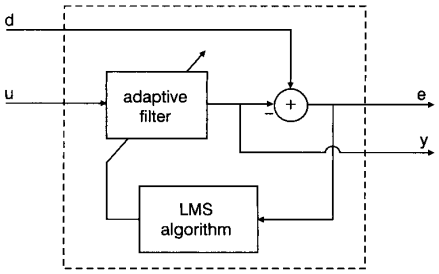

Fig. 1 *General LMS adaptive filter as a two-input, two-output system*

2.1 LMS algorithm

An LMS adaptive filter can be thought of as a two-input/two-output system as shown in Fig. 1. The inputs are the signal to be filtered u and a desired output signal d. The outputs are the filter output y and the error in the filter output $e = (d - y)$. The performance criteria used for LMS adaptation is the mean-squared error (MSE):

$$\varepsilon(\boldsymbol{p}) = E[(d-y)^2] = E[e^2] \tag{1}$$

The operator $E[\cdot]$ in eqn. 1 denotes expectation. The LMS algorithm searches $\Re^N$-space by updating the filter's parameters iteratively in a direction opposite to the gradient $\nabla_p\varepsilon$. In discrete time, the update rule is

$$\boldsymbol{p}(k+1) = \boldsymbol{p}(k) - \mu \cdot \nabla_p\varepsilon \tag{2}$$

where μ is a constant determining the rate of adaptation.

IEE Proceedings online on. 20000052

DOI: 10.1049/ip-cds:20000052

Paper first received 15th June and in revised form 1st November 1999

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The simple yet brilliant idea put forward by Widrow and Hoff in [17] was to drop the expectation operator when substituting eqn. 1 into eqn. 2. In doing so, the instantaneous value of the squared-error $e^2 = (d - y)^2$ is taken to be a noisy estimate of its expected value. The resulting update rule is

$$\boldsymbol{p}(k+1) = \boldsymbol{p}(k) - 2\mu \cdot e(k) \cdot \phi(k) \quad (3)$$

where $\phi(k)$ is the gradient $\nabla_p y(k)$. The LMS algorithm for adaptive filters is defined by eqn. 3. The method used to obtain the gradient signals $\phi(k)$ will depend on the filter structure and is discussed for several different cases in Section 3. Continuous-time implementations of the LMS algorithm are also made possible by simply converting the iterative update represented by eqn. 3 into a continuous integral [18]:

$$\boldsymbol{p}(t) = 2\mu \int_{-\infty}^{t} e(u) \cdot \phi(u) \cdot du \quad (4)$$

In either case, the choice of μ is critical. In most applications, the MSE after convergence will exceed the minimum MSE due to random fluctuations in $\boldsymbol{p}$ around $\boldsymbol{p}^*$. These fluctuations, and hence the excess MSE, can be decreased by taking a small value for μ. Unfortunately, decreasing μ also decreases the rate of convergence. With these conflicting requirements in mind, designers have often employed a 'gear-shifting' approach whereby a large value of μ is used at start-up to provide fast initial convergence. Later, the algorithm switches to a smaller value of μ to decrease the excess MSE in steady state.

2.2 Variants of the LMS algorithm

It was known early on that the product $\varepsilon \cdot \phi$ in eqns. 3 and 4 can be generalised to include any nonideal multiplier of the form

$$e \times \phi = e \cdot f(\phi) \quad \text{or} \quad e \times \phi = f(e) \cdot \phi \quad (5)$$

so long as f is a monotonically increasing function [19]. As early as 1970, this fact was being used to simplify the implementation of the LMS algorithm by taking only the sign of the gradient signal [20]. In the literature, this has been referred to as the 'clipped-data LMS' or 'sign-data LMS' (SD-LMS) algorithm (eqn. 6).

$$\boldsymbol{p}(k+1) = \boldsymbol{p}(k) - 2\mu \cdot e(k) \cdot \mathrm{sgn}\{\phi(k)\} \quad (6)$$

The 'sign-error LMS' (SE-LMS) and 'sign-sign LMS' (SS-LMS) algorithms are similarly defined by taking the sign of the error and/or gradient signals in eqn. 3 [21]:

$$\boldsymbol{p}(k+1) = \boldsymbol{p}(k) - 2\mu \cdot \mathrm{sgn}\{e(k)\} \cdot \phi(k) \quad (7)$$

$$\boldsymbol{p}(k+1) = \boldsymbol{p}(k) - 2\mu \cdot \mathrm{sgn}\{e(k)\} \cdot \mathrm{sgn}\{\phi(k)\} \quad (8)$$

These simplifications can also be applied to the continuous-time LMS algorithm by making straightforward modifications to eqn. 4.

The hardware advantages of these algorithms over conventional LMS are great. If the adaptation is to be performed using analogue circuitry, these simplifications eliminate the need for linear multipliers which are particularly challenging in pure-CMOS VLSI. If digital circuits are used for the adaptation, a full multiplier is reduced to a (trivial) one-bit multiplier or, for SS-LMS, to a single exclusive-OR gate.

On the other hand, these algorithms converge more slowly than the LMS algorithm and with greater excess MSE in steady state [22, 23]. Fortunately, these shortcomings can be compensated for by careful selection of the constant μ and, perhaps, by using gear shifting. A more serious problem for the SD-LMS and SS-LMS algorithms is that instability has been demonstrated [24] due to gradient misalignment. Specifically, the vector term $\mathrm{sgn}\{\phi(k)\}$ in eqns. 6 and 8 is not necessarily parallel to $\phi(k)$, so it is possible for the filter parameters, $\boldsymbol{p}$ to 'climb' the performance surface, thereby increasing the output's MSE until the algorithm diverges. Nevertheless, these algorithms are often used in practice and have proven useful for many applications.

2.3 DC-offset effects in analogue LMS

A block diagram of the LMS-parameter-update rule appears in Fig. 2. If the parameter updates are being performed using analogue circuitry, DC offsets will appear at the inputs to the multiplier and integrator blocks. It has been shown that these offsets prevent the LMS algorithm from converging to the optimal filter parameter values $\boldsymbol{p}^*$ [25–27]. In fact, DC offsets represent a significant performance limitation in many analogue adaptive filters [28, 32, 33].

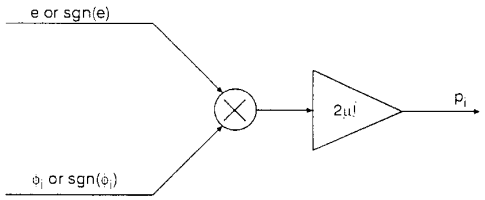

Fig.2 *Block diagram for LMS parameter update*

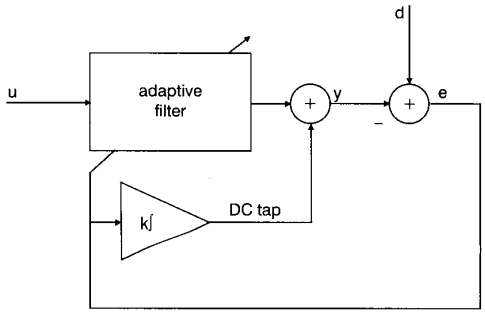

Fig.3 *DC tap for adaptive offset cancellation*

Excess MSE due to a DC offset in the filter output may be eliminated by adding an offset-cancellation tap. Shown in Fig. 3, this tap essentially forces the error signal e to have zero DC content. Its use is now common practice in the design of analogue adaptive filters. Unfortunately, it does not eliminate excess MSE entirely. DC offsets introduced between the multiplier and the parameter update integrator persist.

It was shown in [29] that the SE-LMS and SS-LMS algorithms are more robust than full-LMS with respect to DC offsets. An algorithmic approach to combating DC-offset effects in transversal filters was proposed in [25] which required another set of N adapted coefficients. Circuit-level techniques for offset-compensation in analogue adaptive filters have also been used with varying degrees of success in, for instance, [27, 30, 31]. However, a low-complexity technique for combating DC-offset effects in a general analogue adaptive filter is still lacking.

2.4 Heuristic algorithms

Several heuristic algorithms have been developed which are based on adjusting filter parameters to satisfy some desirable and easily observed condition. For instance, in [32] the resonant frequency of a continuous-time biquad is adapted

to track a sinusoidal input by forcing zero correlation between the biquad's lowpass and notch outputs. Since the biquad structure used in [32] already has lowpass and notch signals available at internal nodes, little additional circuitry was required to implement the adaptive algorithm.

In [33] both the resonant frequency and Q-factor of a lowpass continuous-time biquad were adapted for baseband pulse shaping. The resonant frequency was adapted to force the delay between zero-crossings at the filter input and output to equal some optimum value while the Q-factor was adapted to ensure that the maximum slope of the output waveform equaled some prescribed value. Again, all of the signals required for adaptation were available in the biquad so little additional analogue circuitry was required. This technique was recently extended for use in 100Mbit/s ethernet [34].

Finally, in [35] the high-frequency gain of a receive filter for baseband pulse amplitude modulation was adjusted to eliminate any overshoot or undershoot in the received waveform. The overshoot/undershoot was easily measured by observing the output waveform after each level transition. In combination with adaptive gain compensation, this simple scheme provided enough equalisation for that particular application.

All of these algorithms have a few things in common. First, they are relatively simple, both conceptually and in terms of their hardware implementation. Secondly, each is tailored to a specific application and a specific filter structure. Thirdly, they are limited to situations where adapting one or two parameters is sufficient. So although these heuristic approaches are often efficient, they are not easily generalised to new applications, particularly those requiring high-order filters with several adapted parameters.

3 Filter structures

It should be clear from the preceding discussion that the best adaptive algorithm for a particular situation is often dictated by the filter's structure. An important criterion in selecting a filter structure is that a suitable adaptation algorithm exists, preferably with a straightforward and robust hardware implementation. Also, the filter structure should not go unstable during adaptation. The filter structures in this Section are discussed with these criteria in mind. Since both discrete-time and continuous-time signal-processing functions are possible using analogue circuits, filter structures falling into both categories will be presented.

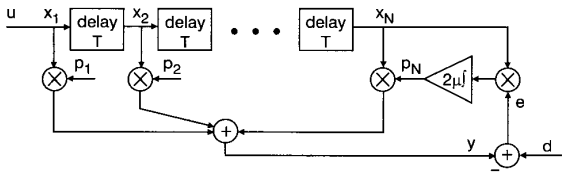

Fig. 4 *Third-order lattice filter for discrete-time signal processing*

3.1 Transversal filters

As shown in Fig. 4, the input to a transversal filter is applied to an equally spaced tapped delay line. Each tap output is then applied to a variable gain and the results are summed together to form the filter output. The adapted parameters are the tap gains $\boldsymbol{p}$. This structure can be implemented in either continuous or discrete time with analogue circuits. In either case, only the transfer-function zeros are adapted and all poles are fixed. By virtue of this fact, the transversal filter is unconditionally stable. Another advantage of transversal adaptive filters is that their performance surface (using the minimum-MSE criteria) is an N-dimensional paraboloid. As a result, convergence to the global minimum is guaranteed by using a gradient-search technique such as the LMS algorithm. Furthermore, the gradient signals required for LMS adaptation are easily obtained at the tap outputs, as shown for one tap in Fig. 4. Finally, any stable transfer function can be approximated with arbitrary accuracy by a transversal filter of sufficient length, although recursive structures can often provide the desired frequency response using much smaller hardware.

3.2 Biquad filters

Although a biquad is really just any second-order transfer function, it possesses several features which make it a popular choice for analogue adaptive filters. A general continuous-time biquadratic transfer function is shown in eqn. 9:

$$H(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0} = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \quad (9)$$

Since any transfer function with real-valued coefficients can be factored into a series of real second-order transfer functions, they can be implemented by a cascade of biquads. This has been such a popular technique for the realisation of fixed high-order analogue filters that there now exists a wealth of theoretical and experimental information on the design of analogue biquads [36].

A useful feature of biquads is that the lowpass, highpass, bandpass, and/or notch outputs are often simultaneously available at various nodes in the circuit. These additional outputs can be used for the adaptation process, as in [32, 33], thereby simplifying the adaptation hardware. Also, both the resonant frequency ω_0 and Q-factor of an analogue biquad can be adapted without approaching instability.

3.3 Laguerre filters

In the early 1930s Norbert Wiener recognised that a set of orthogonal functions named for the French mathematician E. Laguerre could be useful in the design of analogue filters [37]. The Laguerre-filter structure, shown in Fig. 5, is based on Wiener's observations. It realises the set of orthogonal functions $L_i(s)$ in eqn. 10 with a first-order lowpass filter $H_0(s)$ followed by a cascade of first-order allpass filters $H_1(s)$:

$$\begin{cases} L_0(s) = \frac{1}{\sqrt{\pi}} \cdot \frac{1}{1+s} = \frac{1}{\sqrt{\pi}} \cdot H_0(s) \\ L_n(s) = \left(\frac{1-s}{1+s}\right)^n \cdot L_0(s) \\ \qquad = \frac{1}{\sqrt{\pi}} \cdot H_1^n(s) \cdot H_0(s) \qquad \text{for } n > 0 \end{cases} \quad (10)$$

The Laguerre structure realises any linear combination of the transfer functions $L_0(s)$, $L_1(s)$, ... $L_N(s)$. Since the Laguerre functions are an infinite set spanning all finite-energy time signals, any linear transfer function can be approximated closely using a Laguerre filter of sufficient order with the appropriate set of parameter values $\boldsymbol{p}$.

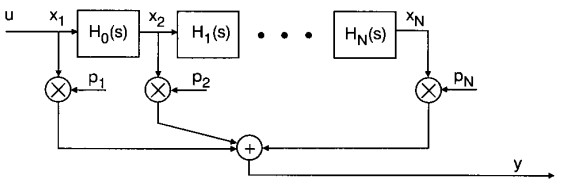

Fig. 5 *Laguerre filter structure*
$H_0(s) = 1/(1 + s)$ and $H_1(s) = (1 - s)/(1 + s)$

In practical implementations, the transfer functions in eqn. 10 would be denormalised to move the pole frequency above the frequency range of interest. In that case, each all-pass section $H_1(s)$ will have a nearly constant group delay. Hence, the Laguerre filter is essentially a continuous-time transversal filter. Like transversal filters, Laguerre filters are well suited to LMS adaptation because the gradient signals ϕ_i are equal to the internal state signals x_i. In addition, only the filter zeros are adapted i.e. all poles are coincident and on the negative real axis. Although stability of the filter is guaranteed, there are situations where the ability to adapt a pole can significantly reduce overall circuit size and complexity.

3.4 Orthonormal ladder filters

The orthonormal ladder filter structure offers several advantages for adaptive analogue signal processing. It is, essentially, a direct implementation of the state–space equations which come about when emulating the states in a singly terminated LC ladder filter:

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{b}u(t) \tag{11}$$

$$y(t) = \boldsymbol{c}^T\boldsymbol{x}(t) \tag{12}$$

where

$$\boldsymbol{A} = \begin{bmatrix} 0 & \alpha_1 & & & \mathbf{0} \\ -\alpha_1 & 0 & \alpha_2 & & \\ & -\alpha_2 & \cdot & \cdot & \\ & & \cdot & 0 & \alpha_{N-1} \\ \mathbf{0} & & & -\alpha_{N-1} & -\alpha_N \end{bmatrix}$$

$$\boldsymbol{b} = \begin{bmatrix} 0 \\ \cdot \\ 0 \\ \sqrt{\frac{\alpha_N}{\pi}} \end{bmatrix} \qquad \boldsymbol{c} = \begin{bmatrix} c_1 \\ c_2 \\ \cdot \\ c_N \end{bmatrix}$$

The structure for a third-order orthonormal ladder is shown in Fig. 6. Note that as the order of the filter increases, so does the number of inputs required at the output-summing node. To prevent this from limiting the bandwidth of a circuit implementation, an alternative structure which makes use of multiple feed-ins is presented in Fig. 7.

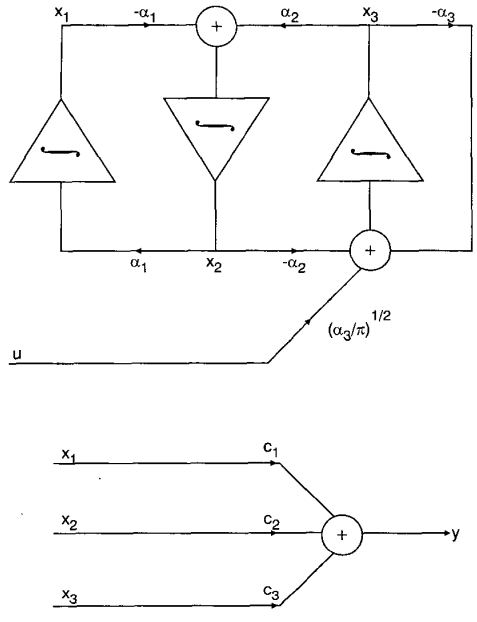

Fig. 6 *Third-order orthonormal ladder filter*

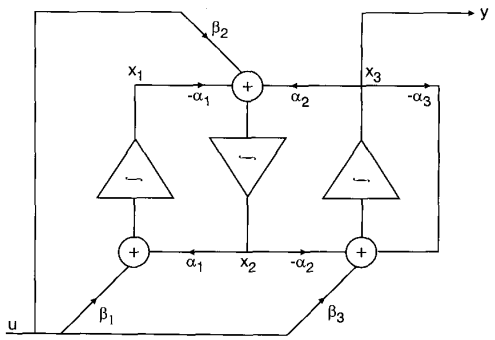

Fig. 7 *Third-order orthonormal ladder filter using multiple feed-ins for the input signal instead of a weighted output summing node*

An orthonormal ladder of sufficient order is capable of realising any rational transfer function. If only the transfer function zeros are to be adapted, the poles can be fixed arbitrarily and only the parameters c_i or β_i are updated. In this case, the orthonormal ladder is used as an adaptive linear combiner and, with a white input signal, the integrator outputs are orthogonal (i.e. uncorrelated) thereby ensuring fast and robust convergence using the LMS algorithm [1]. Alternatively, the poles of an orthonormal ladder filter can be adapted via the parameters α_i while maintaining near-optimum dynamic range scaling. The gradient signals required to adapt the parameters α_i are obtained by applying the corresponding state signals x_i to duplicates of the ladder filter [28]. The additional circuitry which this implies can be shared by multiple coefficient update blocks to reduce complexity and power consumption. Of course, whenever poles are adapted, care must be taken to ensure that the filter remains stable. Furthermore, it may be possible for the filter parameters to converge to a local minimum in the performance surface using LMS adaptation [39]. For a complete overview of orthonormal ladder filters, the reader is referred to [38].

4 Circuit implementations

Until now, this discussion has made reference to several basic analogue building blocks such as delay elements, summers, multipliers and integrators. The implementation of those building blocks is the subject of this Section. Although all of the circuit techniques described here were originally applied to the design of fixed analogue filters, the design of an adaptive analogue filter presents certain unique challenges. For instance, it must be possible to change the filter's parameters via some control signals. On the other hand, matching, process and temperature variations, which can make the design of accurate fixed analogue filters extremely difficult, are often not as critical in adaptive analogue filters because the filter is automatically optimised. (In fact, adaptive techniques are often employed to improve the accuracy of fixed analogue filters.) Practical issues affecting both discrete-time switched-capacitor circuits and continuous-time filters in adaptive applications are discussed below.

4.1 Discrete-time switched-capacitor circuits

Early analogue discrete-time filters used acoustic surface wave devices (SWDs) to implement fixed analogue delays [40]. Unfortunately, the maximum delay times which can be implemented by SWDs are severely limited by size. Bucket-brigade devices were also used to sample analogue waveforms for discrete-time signal processing [41], but they

suffered from poor charge-transfer efficiency. Adaptive signal processing using charge-coupled devices (CCDs) became an active area of research in the 1970s [42–48]. However, CCDs cannot be implemented in a digital CMOS process. As a result, switched-capacitor sample-and-hold (S/H) circuits are now used in almost all discrete-time analogue filters.

There are two main problems with using a chain of sample-and-hold stages to realise a tapped delay line. First, two S/Hs per tap are required because each one must sample during the hold phase of the previous S/H. Secondly, the DC offsets and noise introduced by each S/H accumulate as the signal propagates along the chain. Both problems are solved by introducing a 'rotating tap weight structure' [49] whereby the analogue input voltage is sampled at fixed sites while the tap gains are digitally shifted along the length of the filter, as shown in Fig. 8. Since the analogue sample values are stored at fixed sites rather than being transferred along a long chain of devices, only one S/H per tap is required and cumulative error are eliminated. (Interestingly, this structure is similar to a technique introduced three years earlier for the elimination of charge-transfer inefficiency in a CCD transversal filter [44].) An adaptive transversal filter with rotating tap weights was reported in [50].

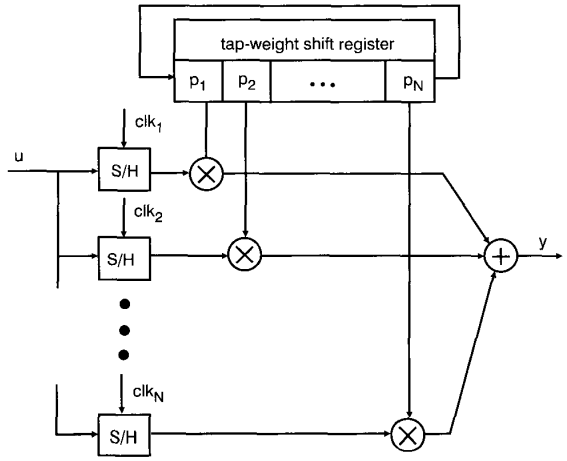

Fig. 8 *Rotating-tap-weight structure for transversal filters using sample-and-hold stages*

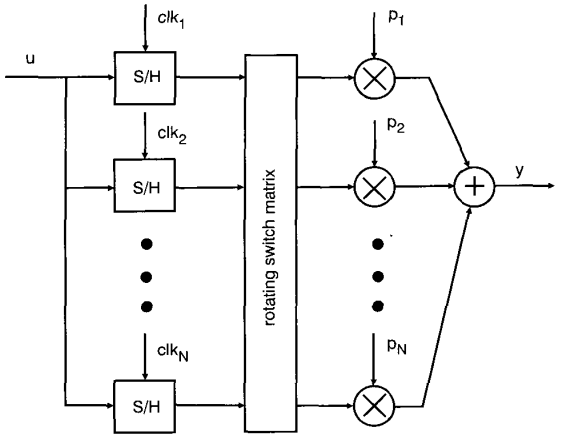

Fig. 9 *Rotating switch matrix used instead of rotating tap weights for transversal filters*

Unfortunately, a rotating tap weight structure operated at high sampling rates requires fast digital switching which is a significant noise source and consumes a lot of dynamic power. These problems are addressed by using a rotating switch matrix between the S/Hs and the multipliers as in Fig. 9 [51]. The input analogue signal is sampled at fixed sites and then routed to the appropriate multiplier via a switch matrix. Meanwhile, the digital tap weights remain stationary, thereby reducing switching noise and power consumption.

In high-speed applications, S/H settling times limit a filter's maximum clock rate. Parallelism can be used to reduce the settling-time requirements on each S/H. For instance, two or more parallel delay lines which are alternately clocked at a fraction of the sample rate can be used [53–55]. Alternatively, one can employ $L > N$ sample-and-hold stages in an N-tap filter [57, 58]. At any given time, the outputs of N S/Hs are routed to the appropriate multipliers via a rotating switch matrix while the other $(L - N)$ S/H stages are settling. This adds an extra $(L - N)$ sampling periods to the settling time of each S/H.

The dynamic range of filters with rotating S/Hs is limited by noise due to mismatches. There are several sources of mismatch between S/Hs. DC-offset mismatches are caused by amplifier offsets, clock feedthrough and/or charge injection, resulting in a fixed-pattern noise which appears as a constant tone in the output spectrum at f_S/L and its harmonics. Mismatches in the gain and sampling phase of each S/H cause sideband noise around f_S/L and its harmonics. Fully differential signalling can be used to reduce the effects of clock feedthrough and charge injection [52] while a master front-end S/H can eliminate sampling-phase mismatches [58]. Nevertheless, these considerations restrict discrete-time sample-and-hold filters to applications where only moderate performance is required.

Several other switched-capacitor building blocks have also been used in adaptive filters. For instance, the advent of switched-capacitor multiplying digital-to-analogue converters (MDACs) in the mid-1970s [59, 60] made digitally programmable tap weights more practical [49, 50, 53]. Around the same time, switched-capacitor filters using binary-ratioed capacitor arrays to program the zeros and/or poles became an active area of research [61]. A simple adaptive equaliser based on this technique appears in [62]. For an overview of these and other switched-capacitor building blocks, the reader is referred to [63].

Unfortunately, switched-capacitor circuits are unsuitable for extremely high-speed applications since switching noise becomes more significant as the clock frequency is increased. Furthermore, to ensure quick settling times the unity-gain frequency of the op amps in a switched-capacitor circuit should generally be at least five times greater than the signal bandwidth. This provides a strong motivation to look at continuous-time circuits for high-speed analogue adaptive filters.

4.2 Continuous-time analogue filters

In discrete-time filters, the fundamental building block is the delay element. However, in analogue continuous-time filters, the fundamental building block is the integrator. Two popular ways to implement continuous-time integrators are illustrated in Fig. 10. They represent two broad categories of analogue continuous-time filters: MOSFET-C (Fig. 10*a*) and transconductance-C (g_m-C) (Fig. 10*b*). An excellent summary of MOSFET-C filters is provided by [64] and examples of g_m-C filters appear in [65, 66, 68, 69, 72, 73].

For both categories, the two main challenges faced in high-speed applications are accurately setting integration

time constants and maximising the circuit bandwidth. Integration time constants in both MOSFET-C and g_m-C filters are usually matched to precision references by the use of on-chip automatic tuning mechanisms such as those described in [67–76]. Filter bandwidths are limited by parasitic poles in the active circuitry. These pole frequencies should be far beyond the filter's cutoff frequency to ensure that they do not effect the overall transfer function [69]. Compared with operational amplifiers, transconductors have simpler circuitry with few, if any, parasitic internal nodes resulting in superior high-frequency performance. Therefore, they are generally preferred in high-frequency analogue adaptive filters.

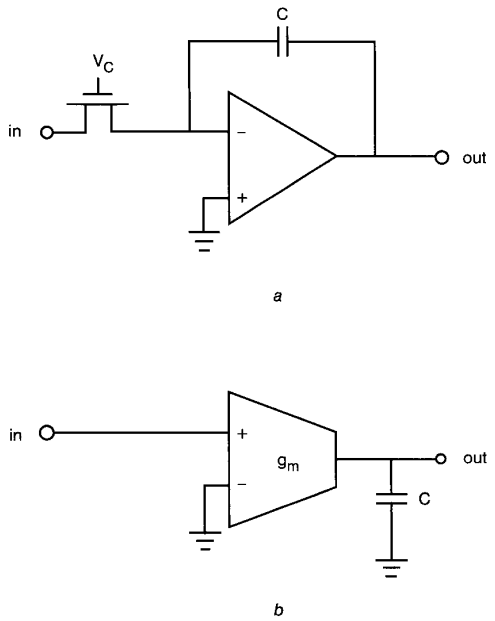

Fig. 10 *Continuous-time (single-ended) integrators suitable for integrated analogue filters*
a MOSFET-C integrator
b g_m-C integrator

5 Applications

This Section provides an overview of several application areas for analogue adaptive filters. These applications are discussed for two reasons. First, they provide excellent examples of the circuits and systems described thus far. Secondly, the applications have always defined research directions and will undoubtedly continue to do so in the future.

5.1 Early applications

Analogue adaptive filters were in use long before the advent of integrated circuits. Inspired by Norbert Wiener's work in the early 1930s, Y.W. Lee reported an efficient cascade of passive elements implementing a Laguerre-filter structure in 1932 [77, 78]. The so-called Lee–Wiener network was used by Wiener in the early 1940s to perform flight-trajectory prediction for use in World War II anti-aircraft fire control. Their work was declassified at the end of the war and the mathematics reported by Wiener in 1949 [79].

Adaptive antenna systems became an important application for adaptive filters in the late 1960s. An adaptive interference cancellation system for beamforming in antenna arrays was desired because the location of interfering sources could not be known *a priori*. The LMS algorithm was employed. At the time, digital electronics were not fast enough to perform the signal-path filtering. Therefore, analogue systems were often used. A review of adaptive antenna systems in the 1960s is provided by [18]. The LMS algorithm was also used in the 1960s to solve optimisation problems using analogue computers [80].

5.2 Digital magnetic storage

Digital magnetic storage emerged as the primary application area for analogue adaptive filters in the 1990s. The signals received from the read head in a magnetic storage channel consist of baseband pulses for which some forward equalisation is required prior to detection. Adaptive equalisation is desired because the characteristics of the read signal depend on the particular zone of the magnetic medium being accessed. High-speed operation allows high storage densities and fast access times. Furthermore, the adaptive filter should have a small area and consume little power to facilitate high levels of integration. Fortunately, only moderate linearity is required (approximately 40dB) to obtain satisfactory bit-error-rates.

Analogue discrete-time transversal filters with five to ten taps are common in modern magnetic storage systems. The delay lines are generally implemented using the S/H techniques described in Section 4.1. However, it is also possible to use a cascade of continuous-time constant-group-delay allpass filters as in [82]. Tap weighting in the transversal filters can be implemented using switched-capacitor MDACs [53], programmable transconductors [57] or, in a BiCMOS process, Gilbert multipliers [58]. If either of the latter two techniques is used, a current output is obtained and the output summer is easily realised by connecting together the appropriate nodes.

Often, the adaptation algorithm is implemented digitally and the optimal FIR coefficients for each zone of the magnetic medium are stored in a digital RAM. The SS-LMS [58, 83] or SD-LMS [56] algorithms are popular because they are easily realised with digital circuitry. The signs of all gradient signals can be obtained using just one comparator at the filter input [56, 58].

Recently, continuous-time adaptive analogue equalisers have been examined for the magnetic storage channel. These offer several advantages over both digital and discrete-time analogue adaptive equalisers. First, continuous-time IIR filters with just a few adapted parameters can provide performance comparable to that of a FIR filter with many more taps. Secondly, a continuous-time filter is also required for anti-aliasing prior to sampling in systems with digital or discrete-time equalisers, so power and area can be saved by combining the equaliser and anti-aliasing filter into a single circuit. Thirdly, when the equaliser is inside the system's timing recovery loop, as for a discrete-time or digital equaliser, the delay introduced can cause slower convergence at start-up.

A seventh-order adaptive continuous-time equaliser with four adapted zeros is described in [84]. Its performance is better than that of a fixed seventh-order continuous-time filter combined with a nine-tap adaptive FIR filter [85]. However, on-chip LMS adaptation circuitry for the filter was not provided. In [86], a continuous-time seventh-order orthonormal ladder g_m-C filter implemented in a CMOS process is used as both a lowpass anti-aliasing filter and an adaptive equaliser. Although only two parameters are adapted using simple digital SD-LMS circuitry, the performance is comparable with that of systems with five-tap adaptive FIR filters. These results are very encouraging and certainly warrant further research.

Table 1: Comparison of state-of-the-art equalisers for digital magnetic storage

	Reference	Number of taps/order	Process	Speed (MHz)	Vdd (V)	Size (mm^2)	Power (mW)
Digital FIR	Thon, 95 [87]	8 taps	0.8μm CMOS	240	3.7	2.9	426
	Pearson, 95 [88]	8 taps	0.5μm CMOS	250	3.7	1.8	340
	Thon, 96 [89]	8 taps	0.5μm CMOS	400	3.3	N/A	400
	Moloney, 98 [90]	5 taps	0.8μm CMOS	200	5.5	1.1	165
Analogue FIR	Xu, 96 [57]	9 taps	0.6μm CMOS	200	5	3.8	325
	Kiriaki, 97 [58]	5 taps	0.8μm BiCMOS	160	5	1.36	240
	Wang, 98 [91]	9 taps	1.0μm CMOS	170	3.3	2.65	70
Cont.-time	Pai, 96 [85]	6th order	1.0μm CMOS	160	3.3	8	65
	Brown, 99 [86]	7th order	1.0μm CMOS	80	5	6.7	280

Table 1 provides a comparison of state-of-the-art adaptive filters implemented using digital, analogue discrete-time, and analogue continuous-time equalisers. Although the process technologies are not exactly the same, analogue designs operating from a 3.3V supply demonstrate a significant power advantage. Furthermore, it is important to remember that Table 1 does not reflect the fact that analogue filters reduce the required analogue/digital (A/D) converter resolution and/or eliminate the need for additional anti-aliasing filters [81], thereby providing further power and area savings.

5.3 Wired digital communications

An adaptive equaliser for digital communications was first proposed by Lucky in 1965 [92]. Since then, data rates over wired communication channels have increased by several orders of magnitude. Modern applications often require multiple adaptive filters for echo cancellation and crosstalk cancellation as well as equalisation [93]. Although many of the adaptive functions in wired data communications can be efficiently performed digitally, analogue adaptive filters play a critical role in some applications.

Analogue adaptive equalisers offer essentially the same advantages in wired digital communications as they do in magnetic storage applications: smaller circuit area and power consumption at high speeds, largely due to the reduced A/D converter specifications. Again, analogue continuous-time equalisation can also eliminate the start-up problems associated with having an equaliser inside a timing recovery loop. However, a key difference between digital communication and magnetic storage applications arises when the wired channel's transfer characteristic has a pole frequency far below the information signal's bandwidth. For example, transformer coupling can introduce a pole at a few kilohertz in multimegabit-per-second channels. As a result, unlike magnetic storage channels where a 5–10-tap FIR equaliser is sufficient, the channel's impulse response can be very long and a large transversal filter may be required to perform equalisation.

Analogue adaptive filters are also used for echo cancellation in full-duplex communication systems where they are required to eliminate any vestiges of the transmit signal from the receive path. Fig. 11 shows a full-duplex system with digital (Fig. 11*a*) and analogue (Fig. 11*b*) adaptive echo cancellation. Note that the entire echo path in Fig. 11*a* including transmit D/A converter, line driver, receive filter and A/D converter must be highly linear to allow for linear echo cancellation in the digital domain. Therefore, an analogue adaptive echo canceller will often ease the D/A converter and line driver specifications, as well at the A/D converter specifications. These savings are particularly significant in applications using standard telephone lines since the echo signal can be up to 30dB louder than the far-end signal. For this reason, analogue adaptive echo cancellers have been used for voiceband modems [94], ISDN [95, 96] and more recently in asymmetric digital subscriber lines (ADSL) [97]. Due to low frequency poles in the echo-path transfer characteristic, the impulse responses required are very long so continuous-time IIR filters are sometimes used [94, 97].

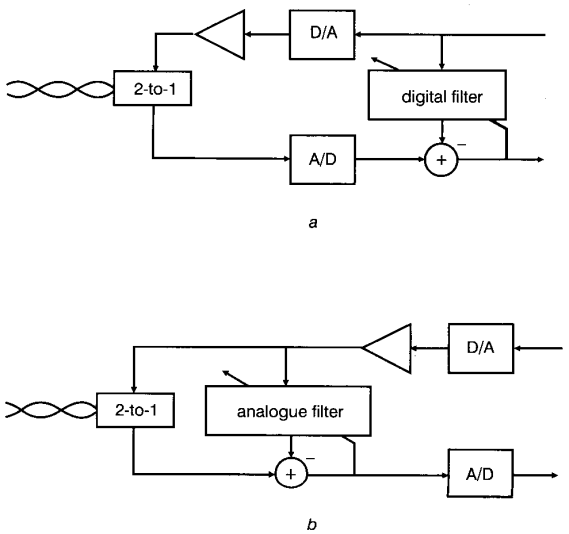

Fig. 11 *Adaptive echo cancellation in a full-duplex wired digital-communication transceiver*
a Digital
b Analogue

For very high-speed applications, an A/D converter and digital equaliser running in the gigahertz range may be impractical, so analogue continuous-time equalisation is the only option. Baseband communication over high-quality coaxial cable is an example of this [98, 99]. In [99] a BiCMOS analogue circuit is used for adaptive cable equalisation up to 2.5Gbit/s. Although new digital process technologies will certainly reach these speeds, there will still be a frequency limit beyond which analogue adaptive signal processing remains more efficient.

6 Conclusions

In the future, it is clear that to improve the reliability and cost of signal-processing electronics, entire systems must integrated on to a single chip. In many applications, an all-digital or all-analogue system is impossible because both analogue and digital external interfaces are required. We must therefore assume that both analogue and digital cir-

cuits will have to coexist on the same IC. The advance of digital process technologies will enable faster digital signal processing with smaller integrated-circuit area and lower power consumption. At the same time it will become increasingly difficult to implement accurate and linear analogue circuits. Therefore, analogue adaptive filters are likely to continue to be targeted at applications where they can simplify or reduce the analogue circuitry required elsewhere on the chip.

An important trend in many digital communication applications is that signal bandwidths are constantly increasing while the required adaptation rates remain fixed. Therefore, longer training sequences and slower adaptation algorithms may be used to simplify the hardware in future adaptive filters.

DC-offset effects introduced by using an analogue LMS algorithm were also discussed. They significantly limit the performance of analogue adaptive filters. There are now indications that digitally programmable analogue filters may be more robust in the presence of DC offsets [100]. Future research will consider hardware-efficient methods for digitally adapting general analogue-filter structures.

In spite of the wealth of theoretical and experimental work on analogue adaptive filters which has been summarised here, at present there are still many applications where they are not used to full advantage. It is hoped that this overview will educate engineers in both academia and industry and motivate future work in the area.

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