Practical Challenges for Electronic Dispersion Compensation in CMOS

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Abstract

Compared to fractional tap-spacing, baud-rate EDC offers simpler tap-weight adaptation while suffering little performance penalty. Unfortunately, the popular CMOS traveling-wave filter provides insufficient bandwidth for baud-rate tap-spacing.

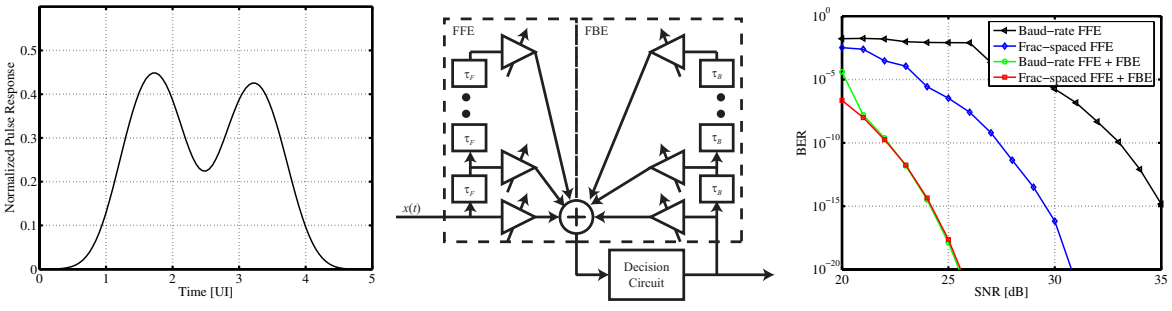
Polarization-mode dispersion (PMD) in single-mode fibre and modal dispersion (MD) in multimode fibre are now major limitations for high-speed optical links. Whereas chromatic dispersion can be efficiently compensated for optically, the varied and changing fibre responses caused by PMD and MD demand a flexible and continuously adaptive electronic compensator. This paper describes the architectural and circuit challenges associated with implementing electronic dispersion compensation (EDC) in CMOS process technologies.

Modal dispersion can cause a single transmitted light pulse to split into two distinct pulses. For example, figure 1(a) plots a normalized pulse response being considered a test case for the 10GBASE-LRM (10-Gb/s optical communication) standard. Called a "split-pulse response", this case is particularly problematic since the channel's frequency response has deep nulls. Any attempt to linearly restore the portion of transmitted spectrum attenuated by the channel's null would require large gain at the null frequency. Such large gains are generally difficult to implement in CMOS and amplify noise unacceptably. Hence, EDC must employ some form of nonlinear processing.

A decision-feedback equalizer (DFE) is a nonlinear system that uses past decisions made in the receiver to restore the lost spectrum. Figure 1(b) shows a general DFE comprising two linear filters: a feedforward equalizer (FFE) and a feedback equalizer (FBE). The FFE filters the received signal while the FBE operates on the output of a nonlinear decision circuit. It is common (though not necessary) to employ finite impulse response (FIR) filters for both the FFE and FBE. Such a structure is very flexible, capable of handling any pulse response so long as a sufficient number of taps is provided. Furthermore, stable adaptation of the FIR filter coefficients is always possible using conventional gradient-descent adaptation algorithms.

Figure 1(c) shows bit error rate curves for 4 different EDC architectures applied to the split-pulse channel. The number of taps is determined by the length of the worst-case pulse response. For instance, the FFE and FBE in figure 1(c) span 3 UI and 2 UI respectively to capture most of the energy in the split-pulse response of figure 1(a). In this case, decision feedback provides a 5-dB performance improvement of at a BER of 10^{-15}, clearly identifying the need for a FBE in EDC circuits.

In figure 1(c), a "baud-rate FFE" refers to an equalizer with $\tau_F = 1$ UI, whereas a "fractionally-spaced FFE" has $\tau_F = 0.5$ UI. Generally, fractionally-spaced equalizers can provide better performance than baud-rate equalizers since they serve as both matched filter and equalizer. In practice, however, the performance improvements are small. For example, in figure 1(c) negligible performance improvement is observed when the FFE is combined with a FBE. Furthermore, the adaptation of fractionally-spaced tap weights is problematic. For example, if the LMS algorithm is employed to adapt the FFE coefficients, a fractionally-spaced FFE may actually *increase* jitter and bit error rate compared with a baud-rate equalizer [1]. Furthermore, it is well known that fractionally-spaced equalizers can have difficulty converging because neighboring tap signals $x(t)$ and



(a) (b) (c)

Fig. 1. (a) A normalized split-pulse response typical for modal dispersion. (b) A decision feedback equalizer (DFE). (c) Bit error rates for various EDC architectures.

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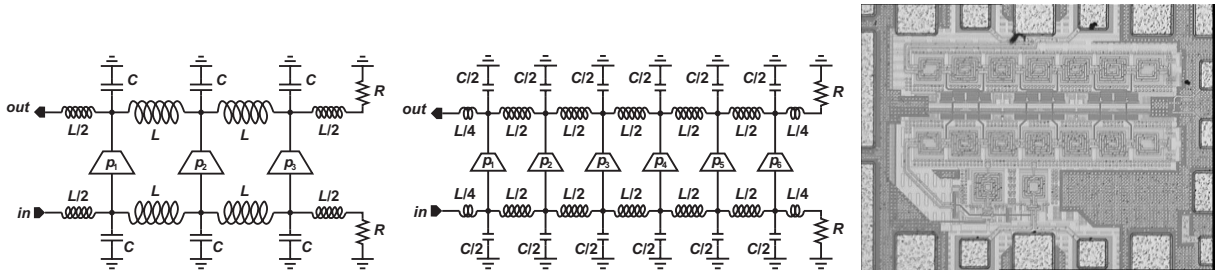

Fig. 2. (a) A 3-tap traveling-wave FIR filter. (b) A 6-tap traveling-wave filter with twice the bandwidth and one-half the tap spacing. (c) A die photo of a CMOS analog FIR filter employing a modified traveling-wave filter topology [8].

$x(t+\tau_F)$ are highly correlated [2]. In summary, baud-rate tap spacing in the FFE simplifies tap weight adaptation with little performance penalty compared to fractional tap spacing.

A fully-digital implementation of the EDC in figure 1(b) is possible if the optical signal is digitized with a resolution of 4 to 6 bits. Digital EDC promises a flexible, robust implementation. However, at 40 Gb/s the power consumption of digital EDC is likely to far exceed that of an analog or mixed analog-digital implementation in modern CMOS process technologies . For instance, just the front-end of a 30-GS/sec A/D converter with 7 GHz bandwidth consumes 270 mW in 0.13 μm CMOS [3], compared with only 70 mW for a complete 3-tap analog FIR filter operating up to 40 Gb/s in a 0.18-μm CMOS process [4].

Analog FIR filters require broadband analog delays. Either active [5], passive [6], or hybrid delay lines [7] can be employed; in any case a M^{th}-order delay line with a rational frequency response $T(s)$ will have the greatest possible group delay when $T(s)$ has M finite right-half-plane zeros. The resulting phase response $\arg T(j\omega)$ will monotonically decrease from 0 at dc to $-M\pi$ as $\omega \to \infty$. Therefore, if a (roughly) constant delay of $\tau_{\text{tot}} = -\frac{\delta \arg T(j\omega)}{\delta\omega}$ over a bandwidth W is required, the order of the delay line must be at least

$$M \geq \frac{W\tau_{\text{tot}}}{\pi}. \tag{1}$$

Equation (1) captures a fundamental delay-bandwidth tradeoff applicable to any analog delay line.

Many of the highest speed analog FIR filters in CMOS technologies have employed the traveling-wave filter architecture with passive artificial transmission lines as delays, as depicted in figure 2(a). Its symmetric layout ensures that the output summation is distributed over several circuit nodes, each with small parasitic capacitance thereby providing high bandwidth. To increase the passive delay line's bandwidth W with fixed total delay τ_{tot}, equation (1) indicates that the number of sections M must be increased. This may be done without changing the artificial transmission lines' characteristic impedance by doubling the number of LC sections and halving the inductances and capacitances, L and C. The result is a filter with twice the bandwidth and twice the number of taps, but one-half of the tap-spacing as shown in figure 2(b). Unfortunately, this tradeoff makes it particularly difficult to realize a baud-rate equalizer with sufficient bandwidth using a traveling-wave filter. Figure 2(c) shows the die photo of a CMOS equalizer employing a crossover technique to alleviate the resulting delay-bandwidth-gain tradeoffs in CMOS equalizers [8].

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