An Anti-Aliasing Multi-Rate $\Sigma\Delta$ Modulator

Anthony Chan Carusone
Depart. of Elec. and Comp. Eng.
University of Toronto, Canada

Franco Maloberti
Department of Electronics
University of Pavia, Italy

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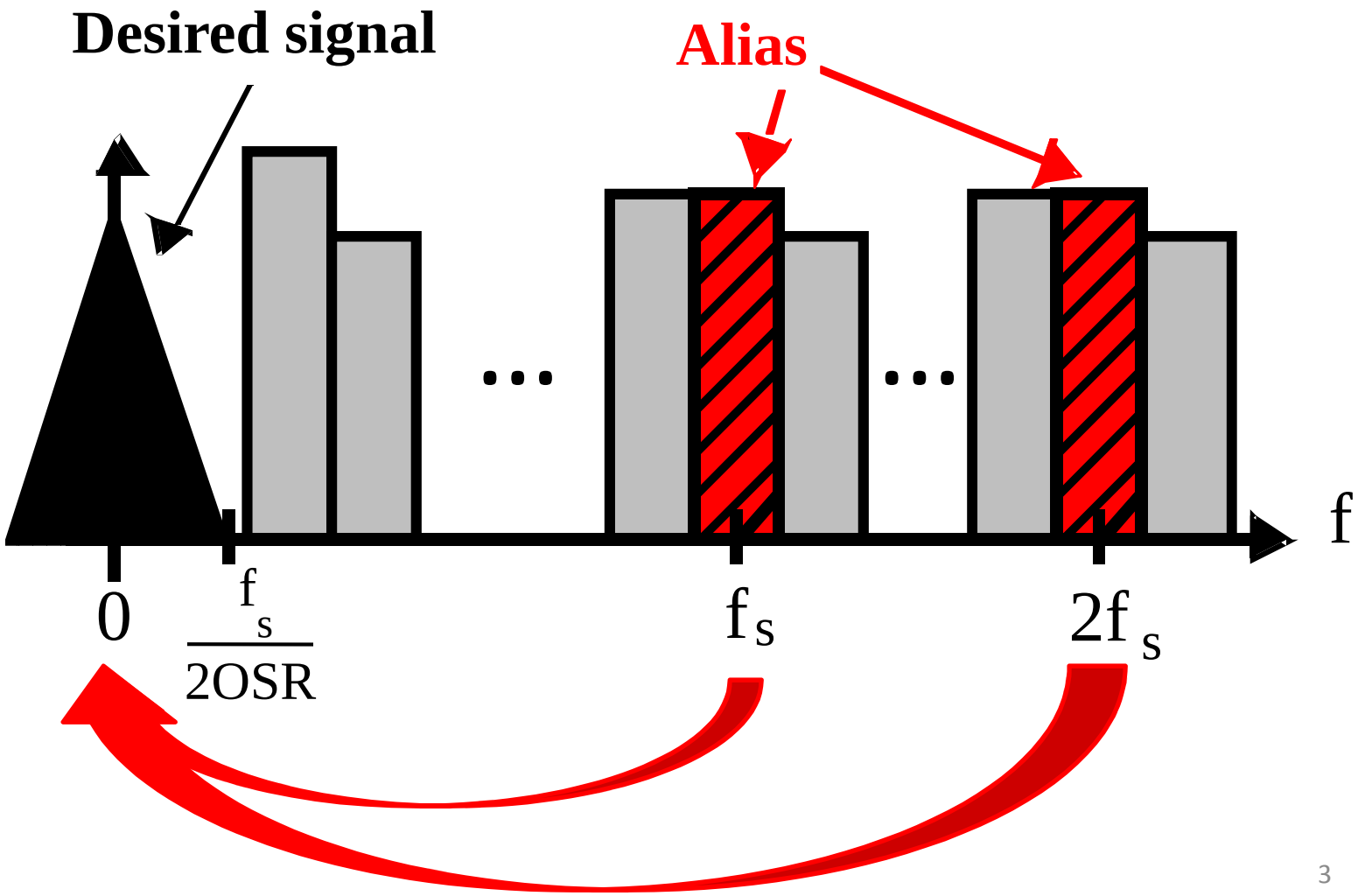
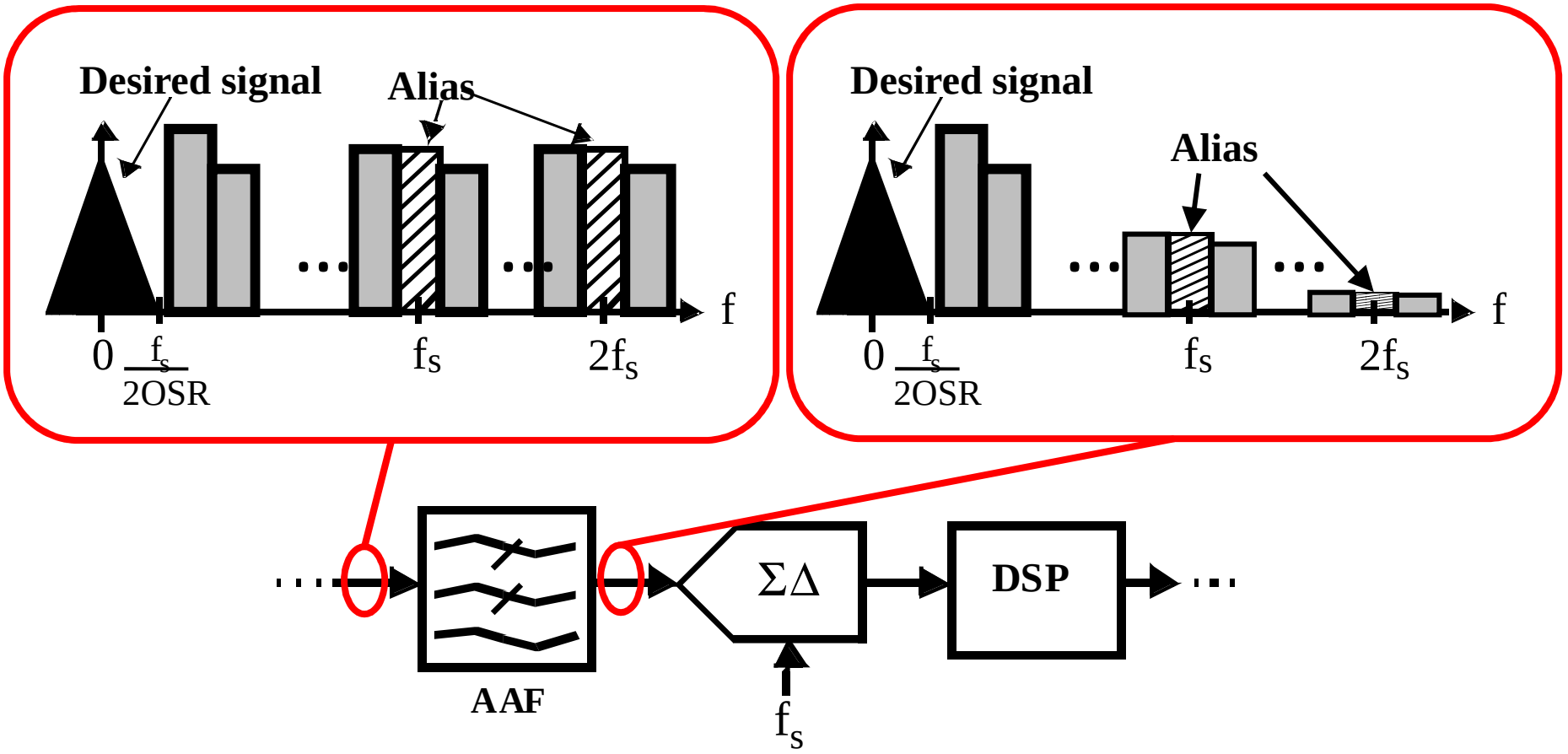
Outline

- Motivation and background
- Anti-aliasing multi-rate modulator front-end
- Practical considerations
  - Mismatch
  - Clocking
  - Opamp settling requirements
- Simulation results
- Conclusions

Aliasing in Discrete-Time ΣΔ Modulators

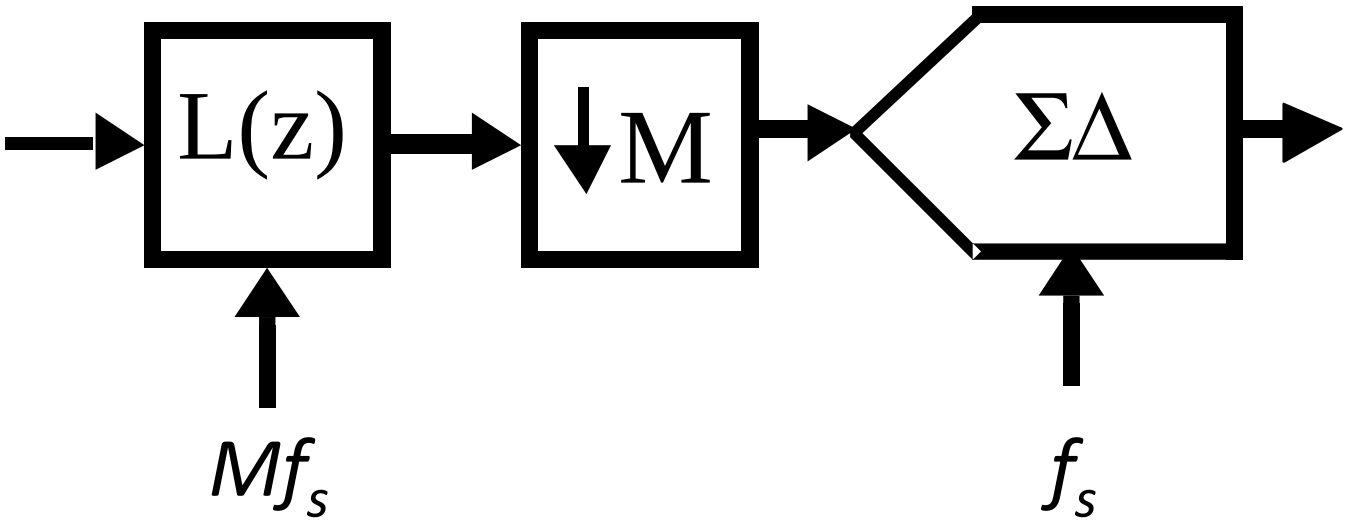


Anti-Aliasing in Discrete-Time ΣΔ Modulators



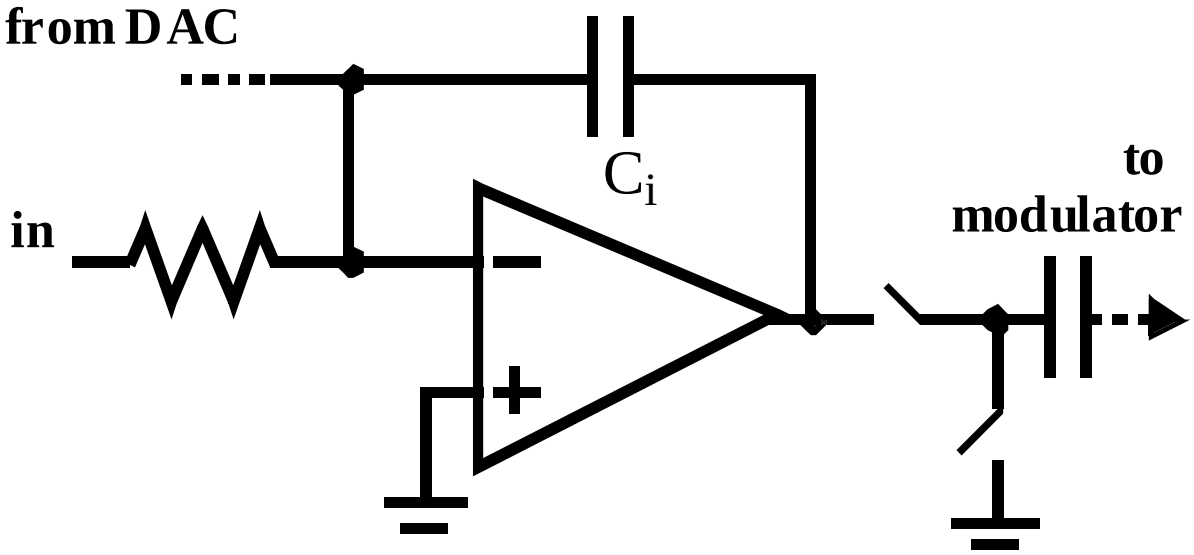
AAF may be either a continuous-time filter or a discrete-time filter operating at a higher sampling rate [6,7], Mf_s

Discrete-Time ΣΔ Modulator with Discrete-Time Anti-Aliasing Filter



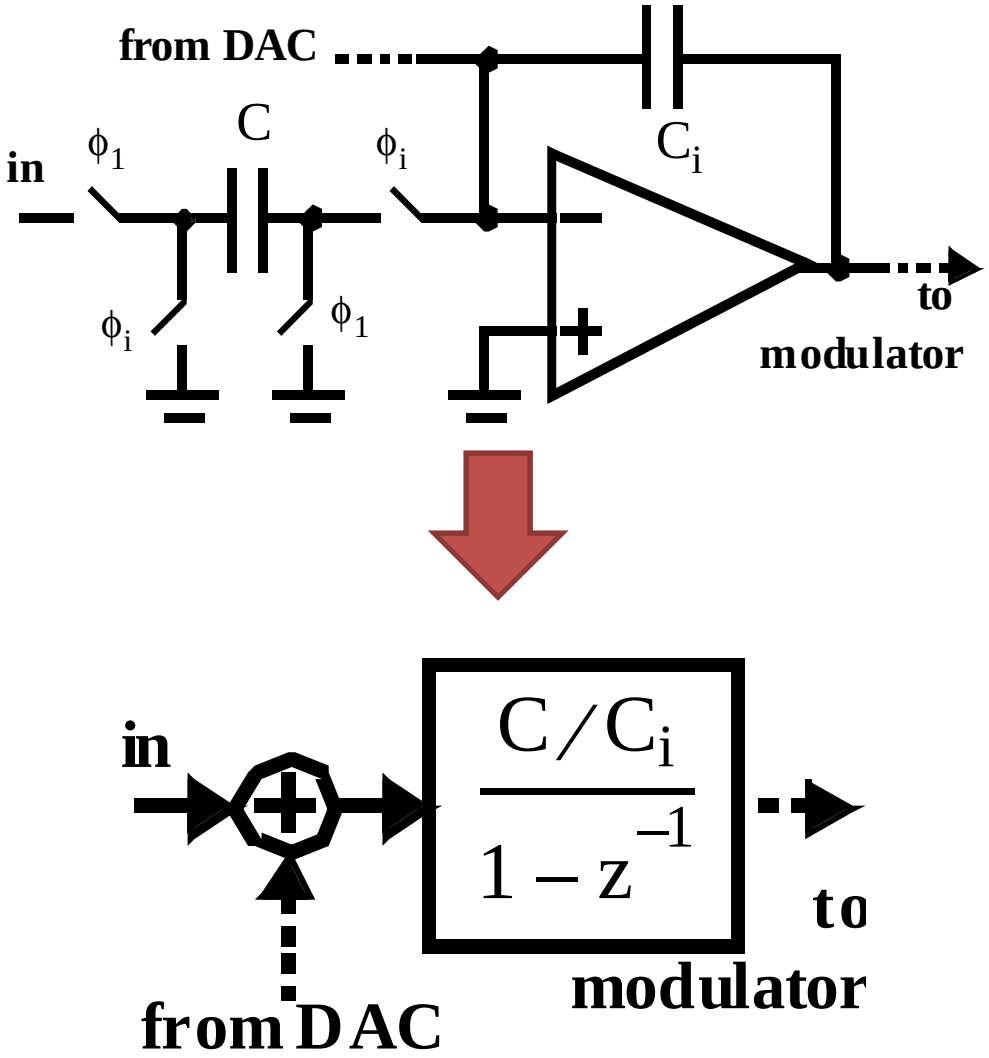
Basic idea is to incorporate L(z) into the front-end of the ΣΔ modulator with minimal circuit overhead

“Hybrid” ΣΔ Modulators

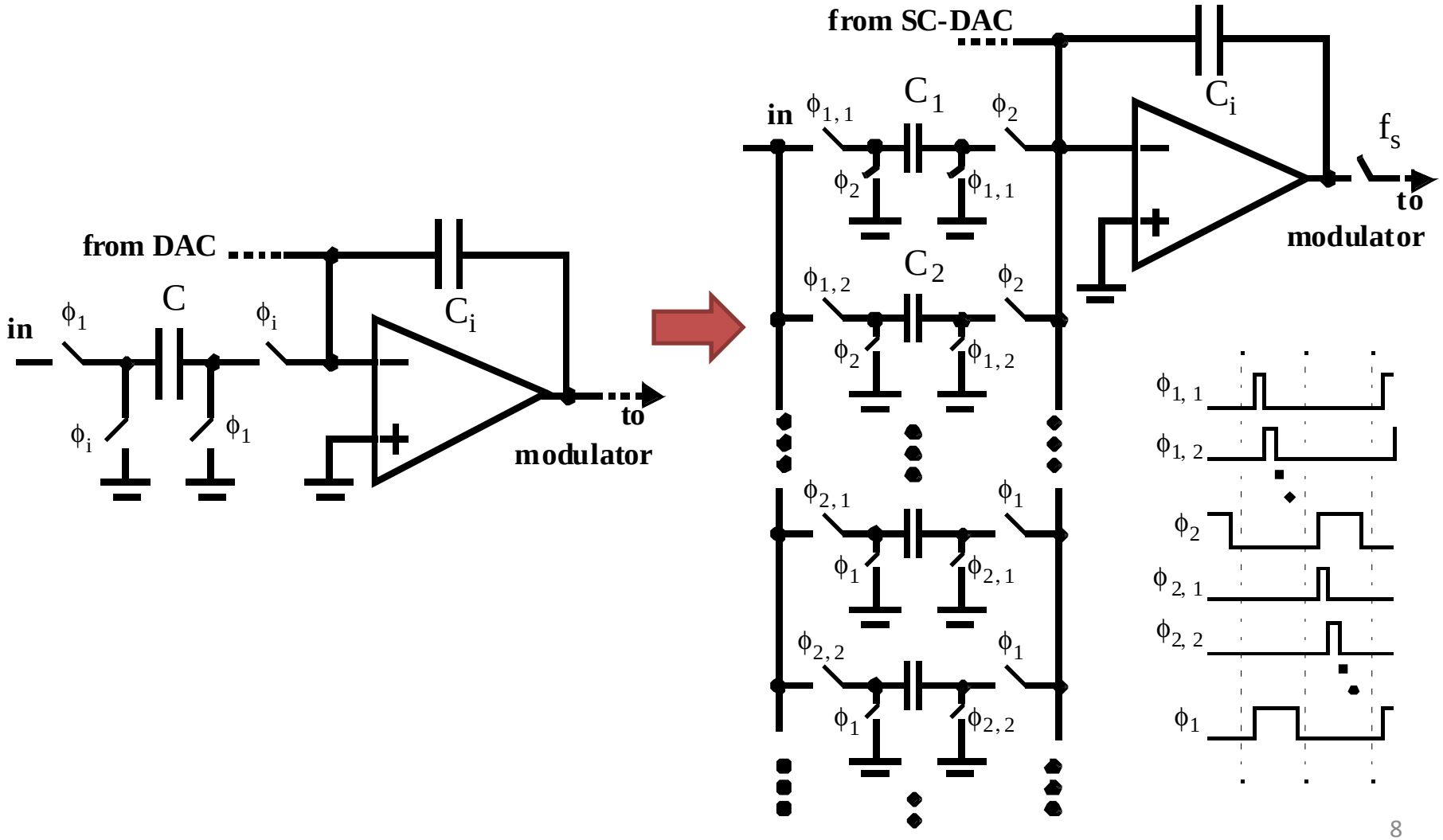


There are several examples of modulators incorporating a continuous-time front-end to provide an anti-aliasing STF [1-5], but these are still susceptible to clock jitter, like all CT modulators.

Conventional ΣΔ Modulator Front-end



ΣΔ Modulator with Anti-Aliasing Front-end Sampler



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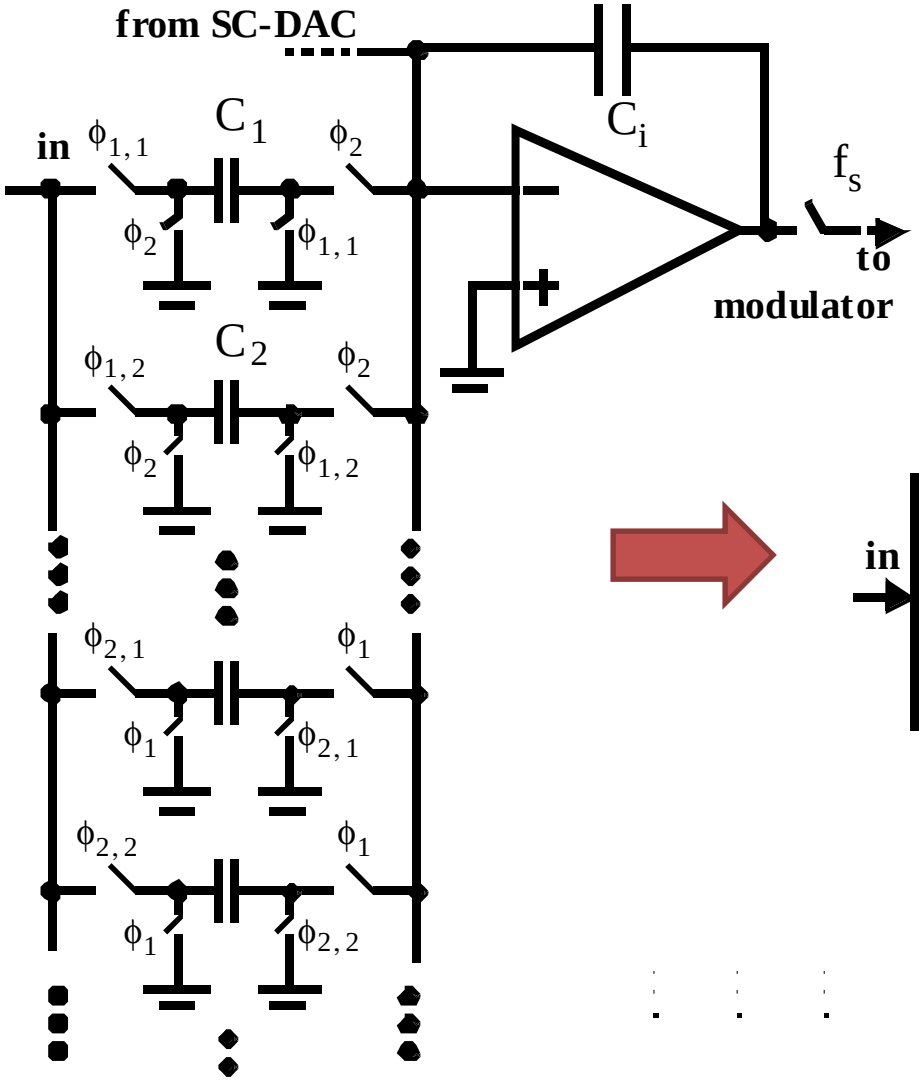

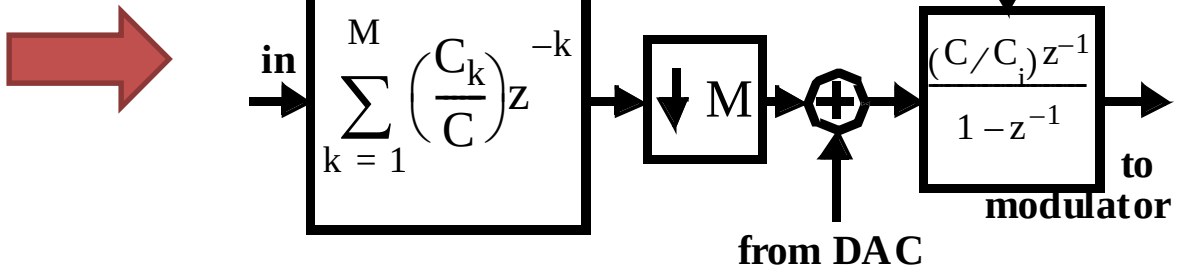

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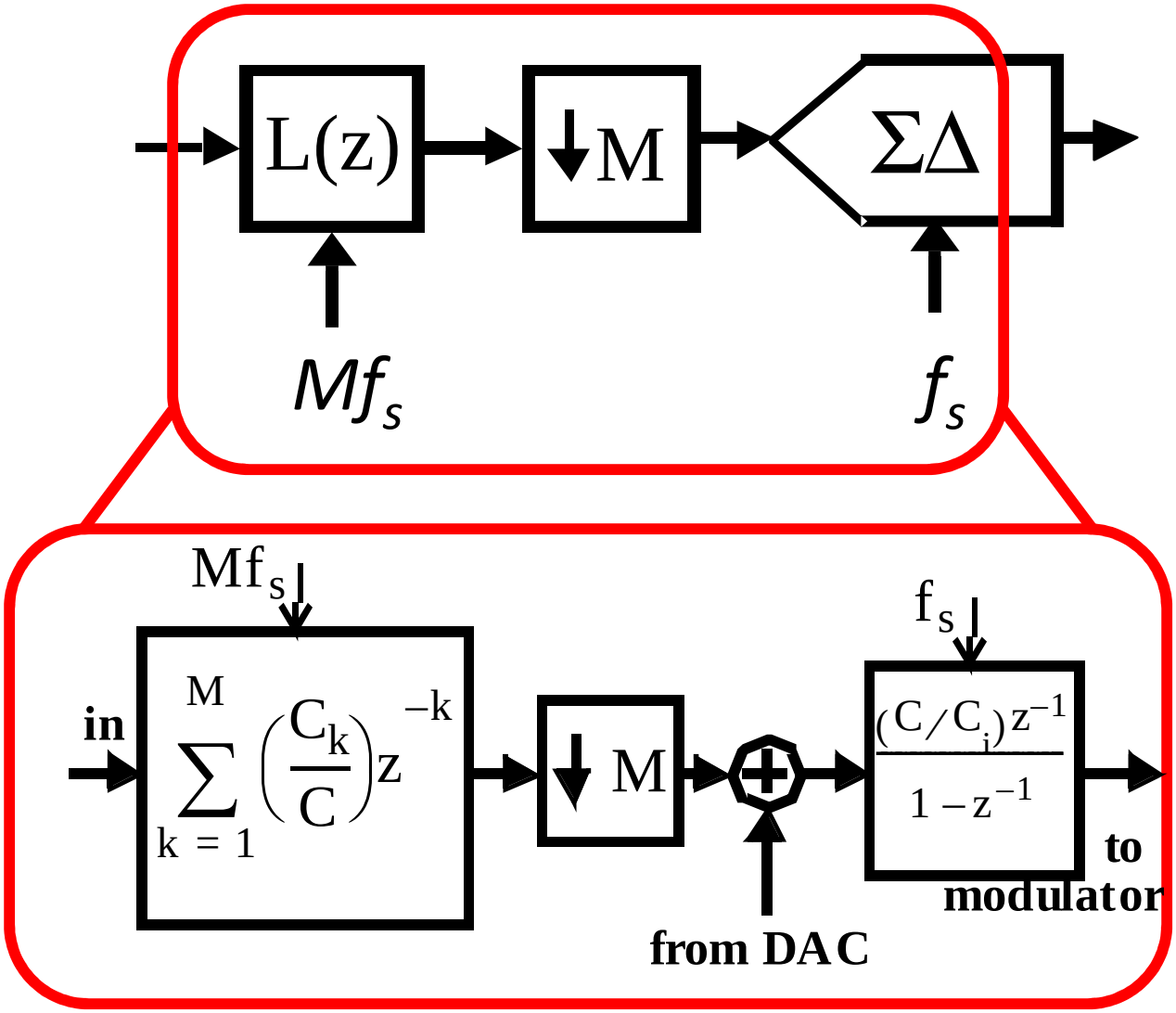
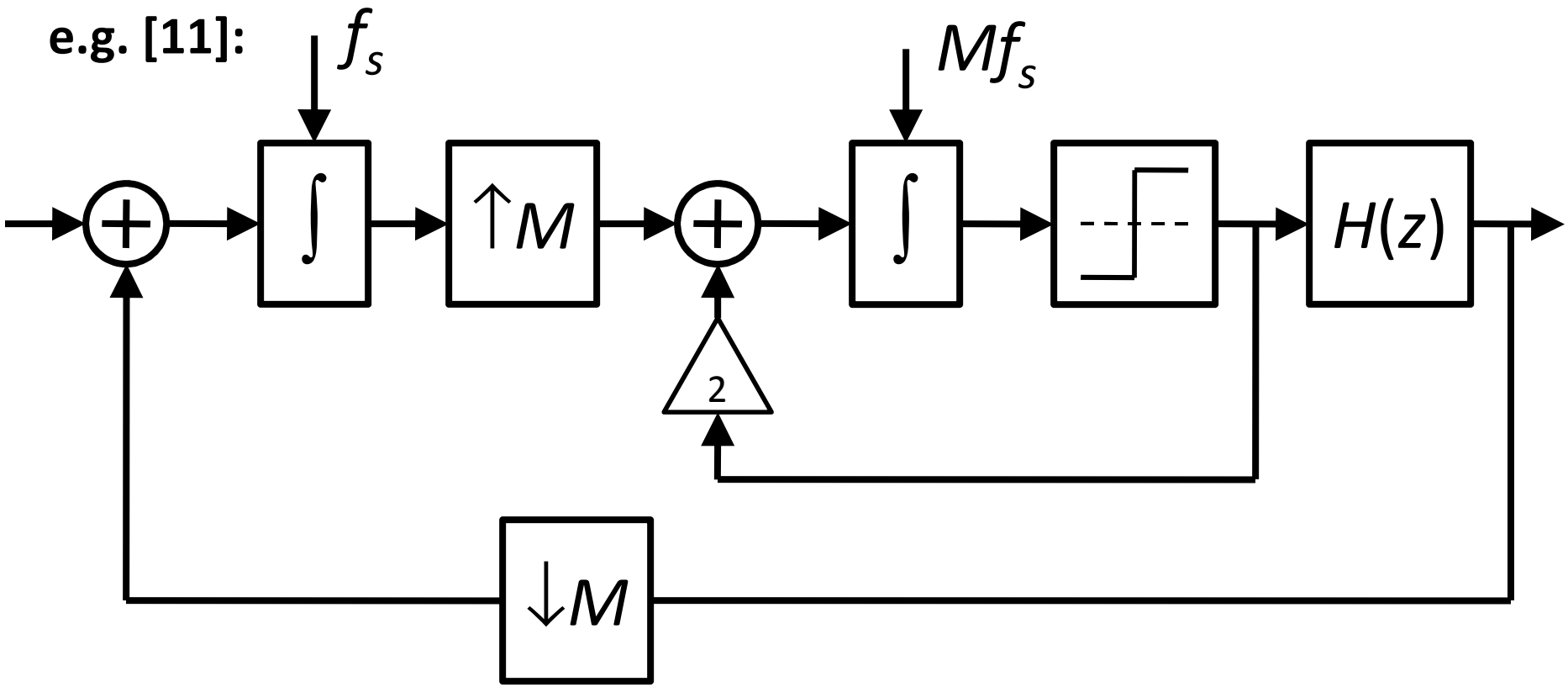


Similar approach has been applied to integrate anti-aliasing into the front-end of a discrete-time filter [8,9] and SAR ADC [10]

Other "Multi-Rate" ΣΔ Modulators

e.g. [11]:



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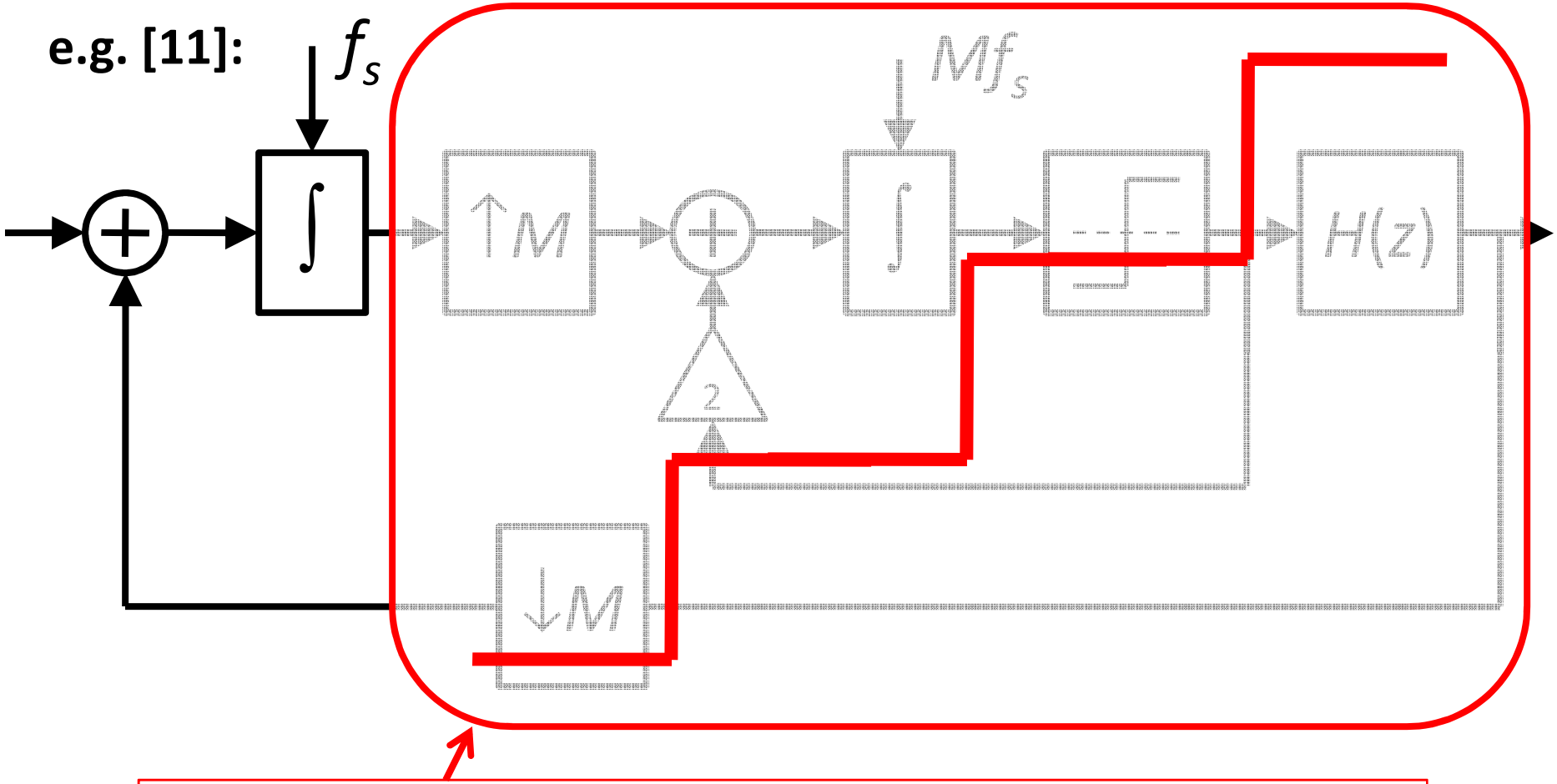
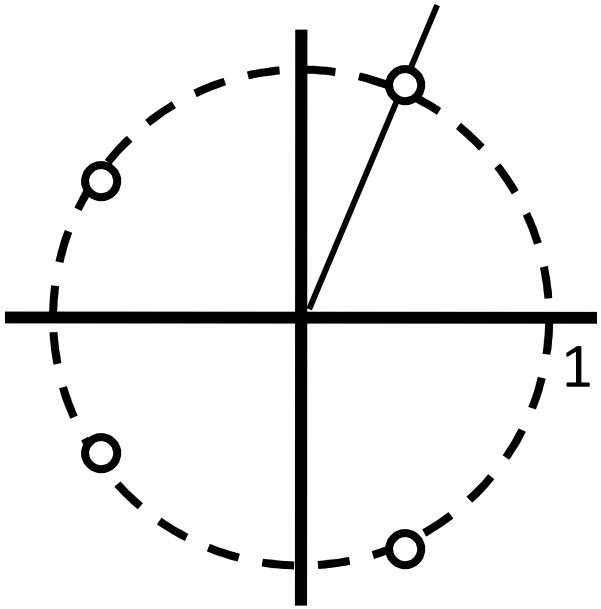


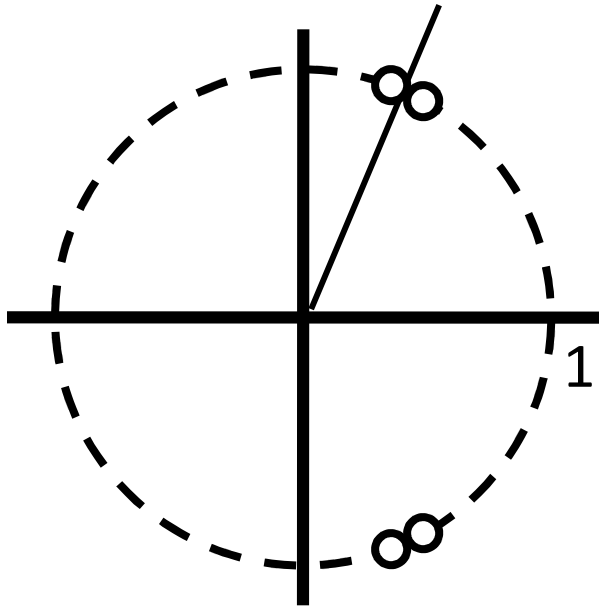
Multi-bit quantizer is replaced by a single-bit modulator + decimator operating at increased sampling rate

Choice of capacitor values, C_k

Zeros of $L(z)$ with $M = 5$:

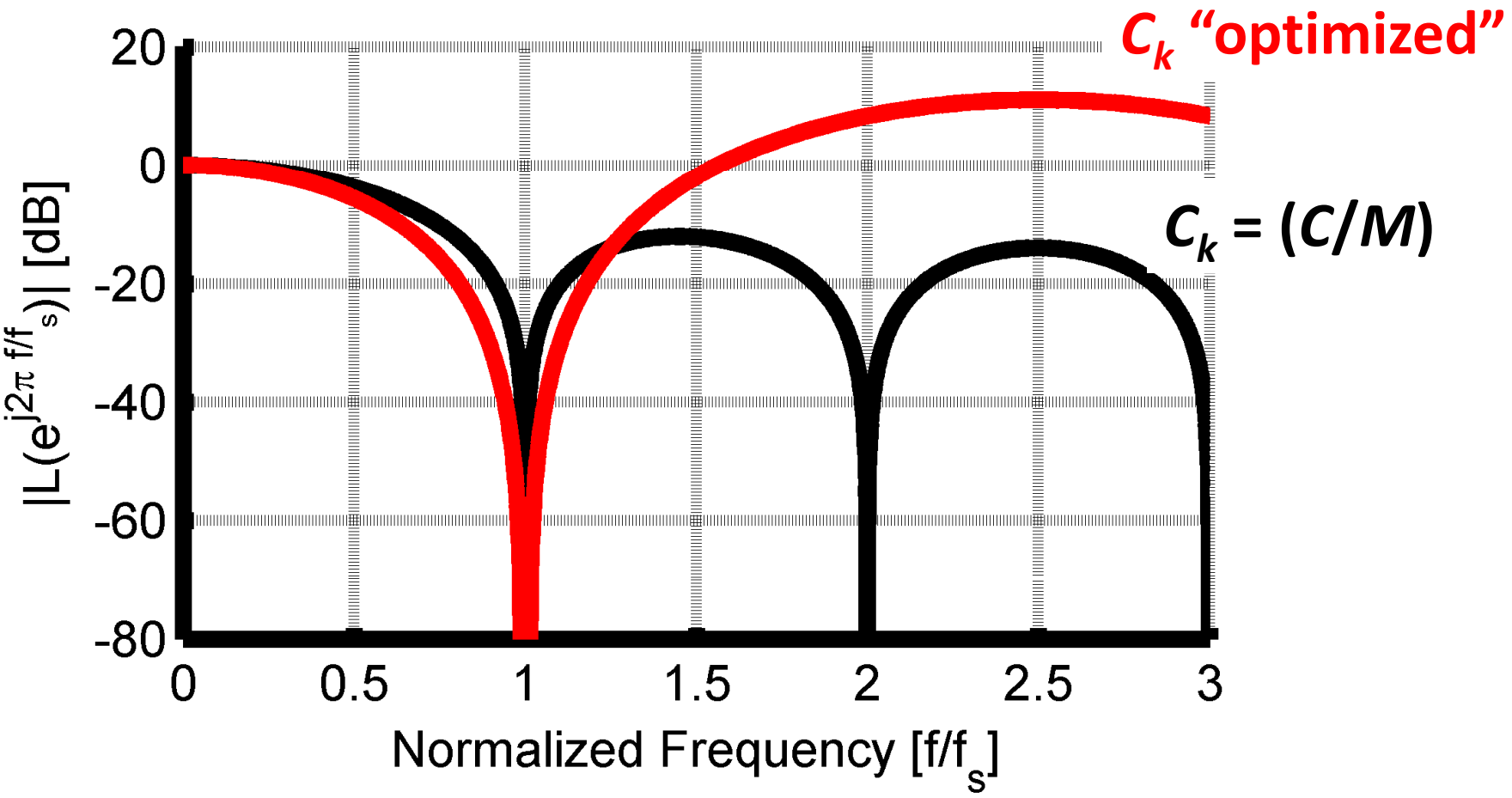


$C_k = (C/M)$



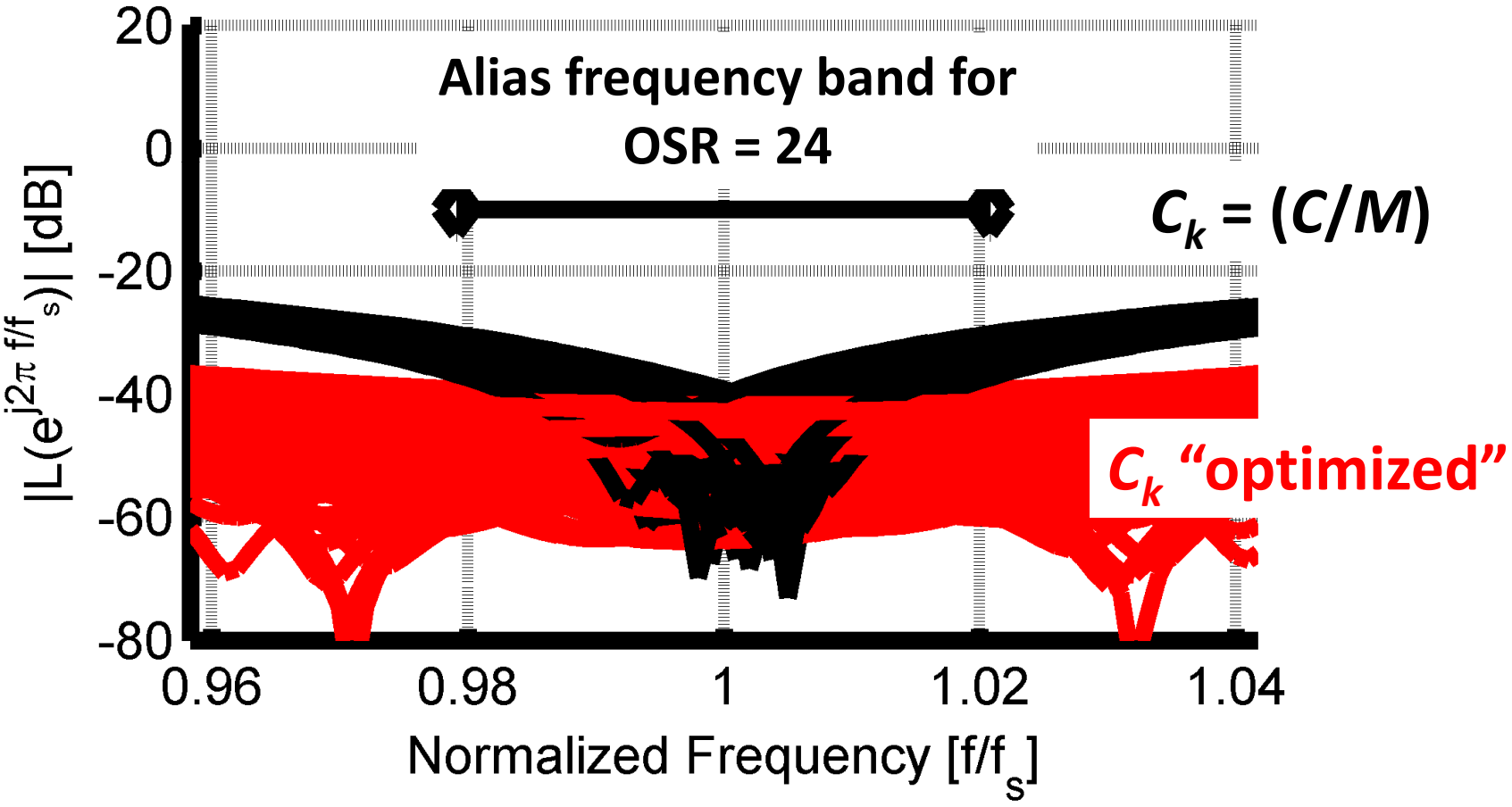
C_k chosen to maximize anti-aliasing around f_s

Choice of capacitor values, C_k



Increased width of the anti-aliasing notch is particularly important in low-OSR modulators

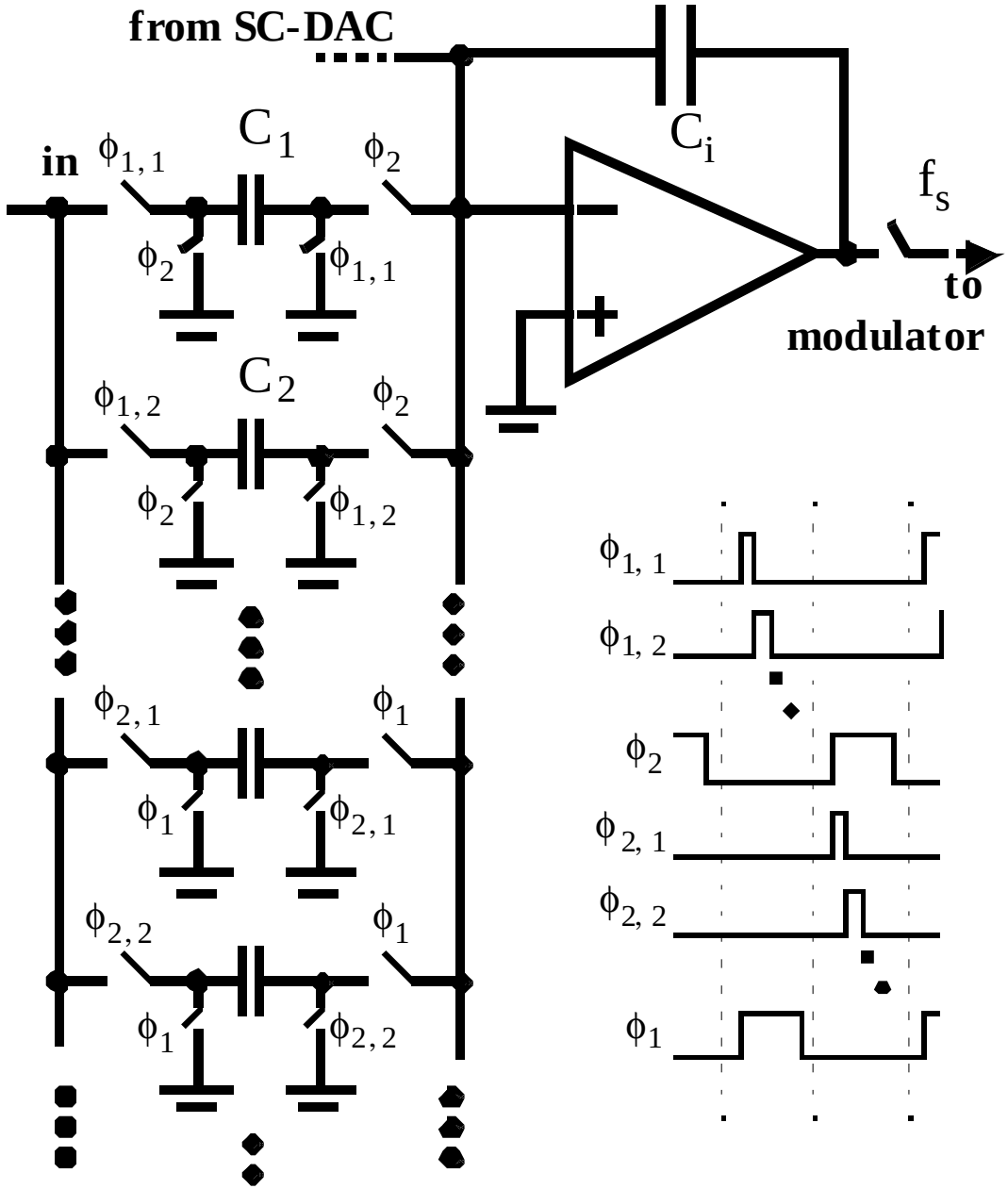
Capacitor Mismatch



100 Monte-Carlo frequency responses with capacitor value standard deviation of 0.2%

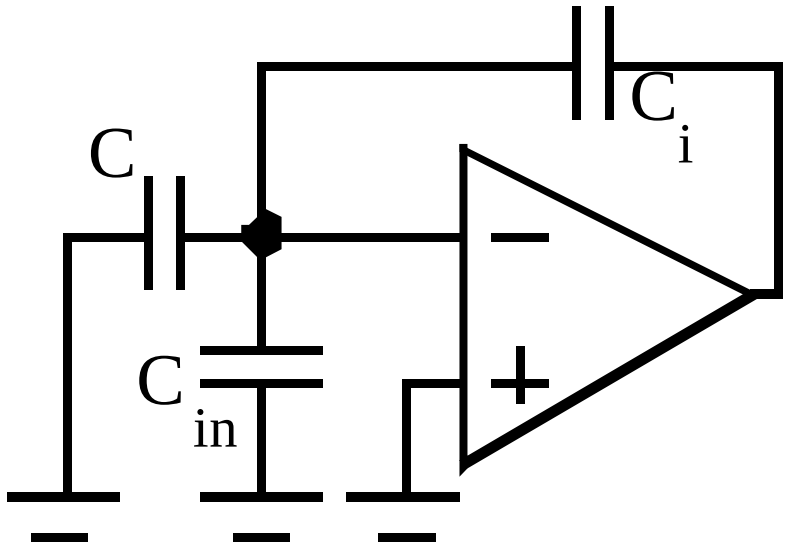
Clocking

- This scheme requires the generation of multiple clock phases [2]
- Faster settling of the sampling capacitors necessitates larger switches and, hence, some overhead in the clock distribution
- Skew between the clock phases results in harmonic at $f_s \pm f_{in}$, which will be filtered by the following digital decimation filter

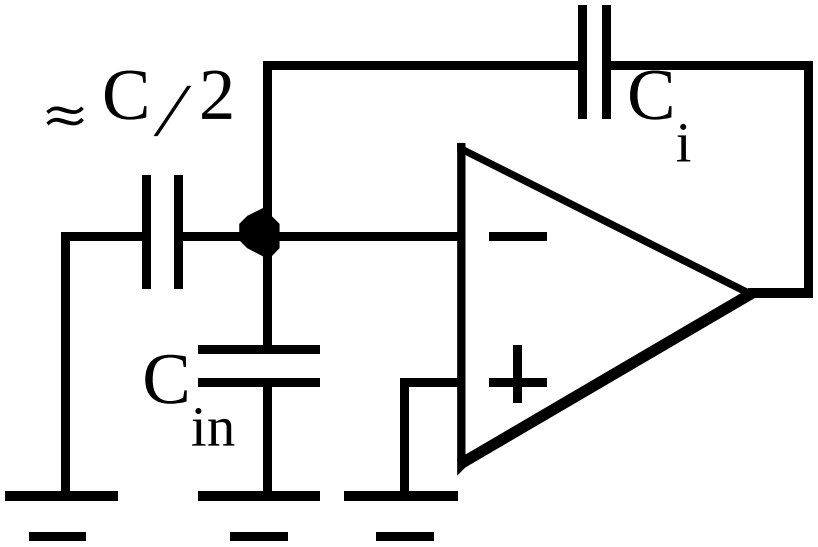


Opamp Settling Time

Conventional ΣΔ modulator front-end during the integration phase:



Anti-aliasing multi-rate ΣΔ modulator front-end during the integration phase:



Since only ½ of the total sampling capacitance is integrated at any time, the feedback factor in the integration phase is increased, thus permitting the use of an opamp with lower GBW.

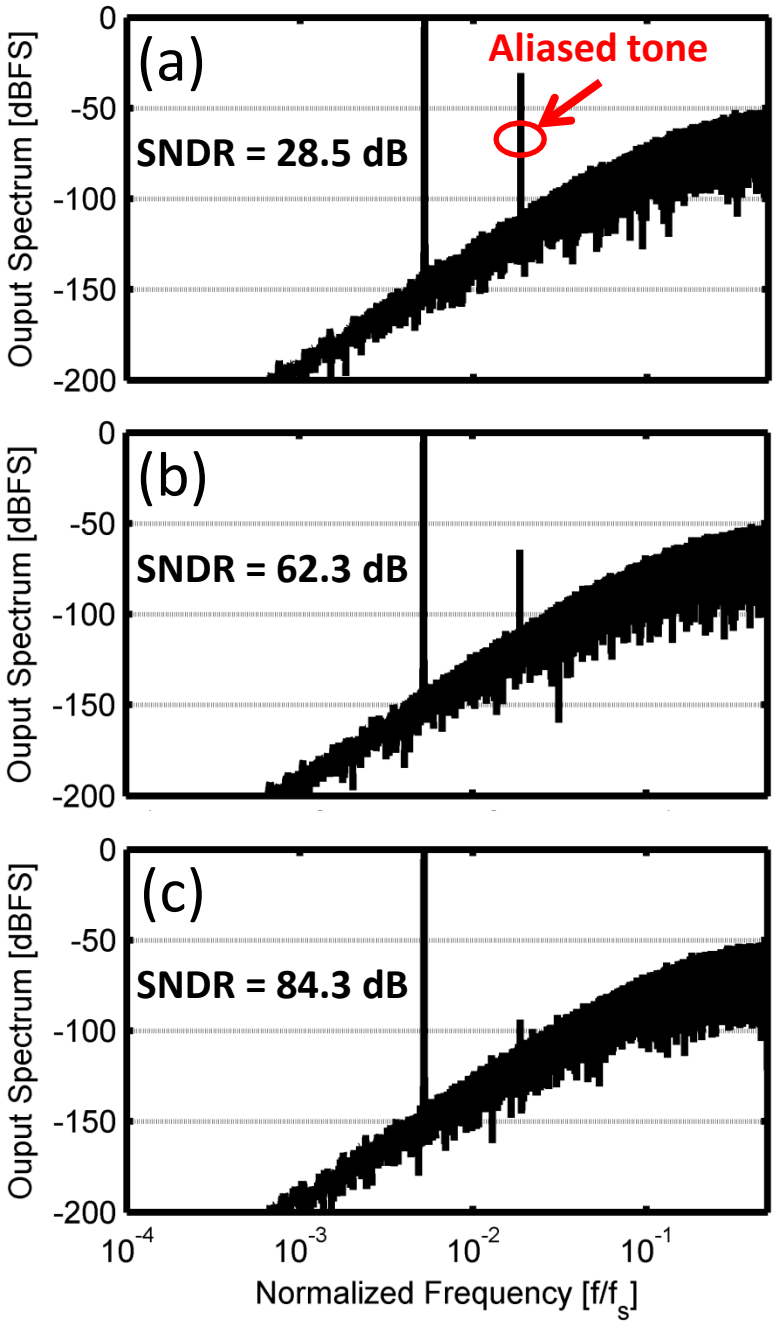
Simulation Results

- 3rd-oder modulator
- OSR = 24
- Two-tone input:
  - -2 dBFS in-band
  - -30 dBFS at 0.98f_s

a) Conventional front-end

b) Anti-aliasing multi-rate front-end with $M = 5$ and $C_k = C/M$

c) Anti-aliasing multi-rate front-end with $M = 5$ and optimized C_k



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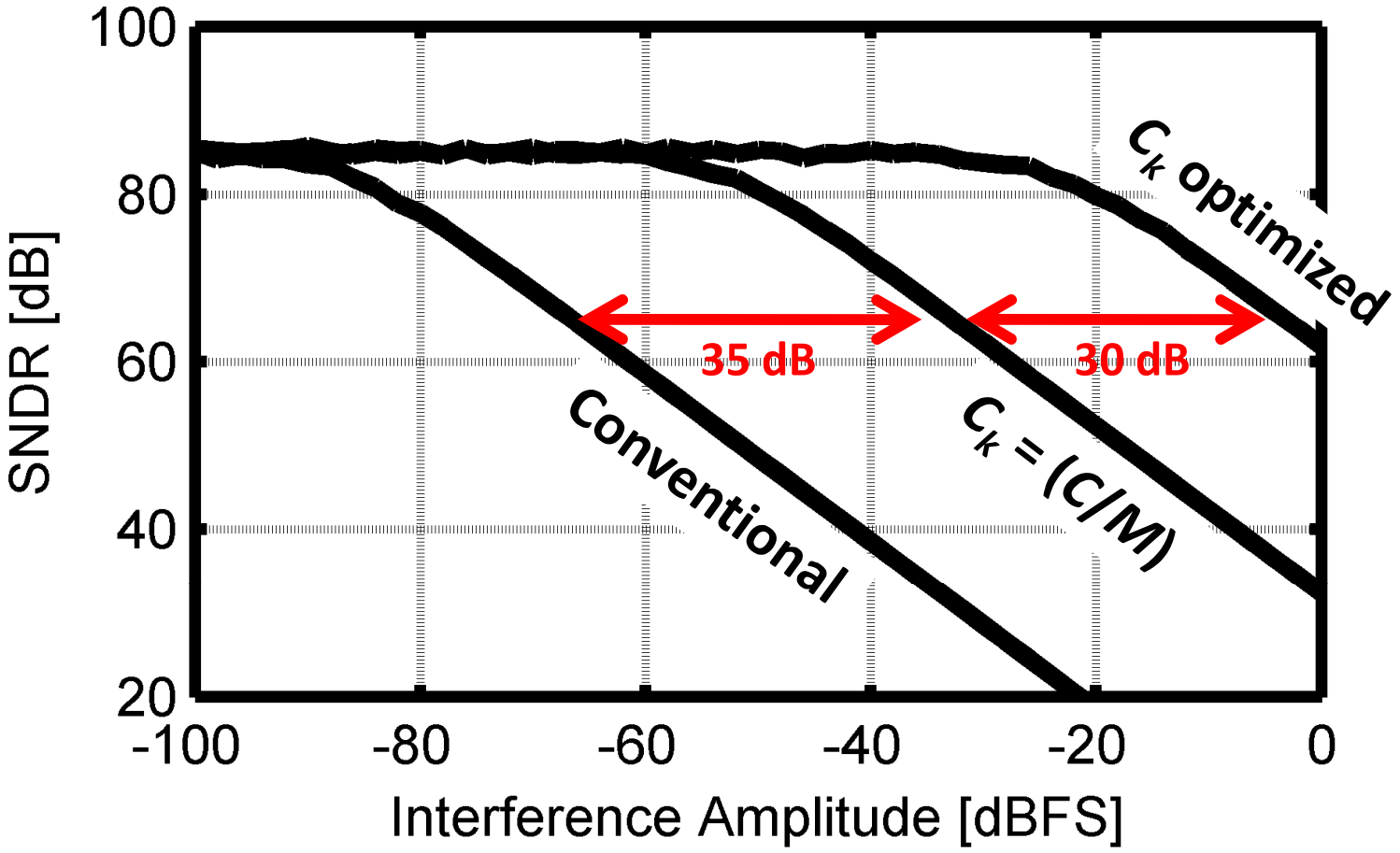

Conclusions

- Splitting the input sampling capacitor in a discrete-time $\Sigma\Delta$ modulator into multiple parallel branches sampled at increased rate enables the STF to be shaped by an FIR transfer function, here used for anti-aliasing
- Example 3rd-order modulator with OSR=24 and M=5 demonstrates:
  - 35 dB of anti-aliasing is provided by a uniformly segmented input sampling capacitor, $C_k = C/5$
  - An additional 30 dB of anti-aliasing is provided when the values of C_k are optimized for a total of 65 dB of anti-aliasing

EXTRAS

Simulation Model

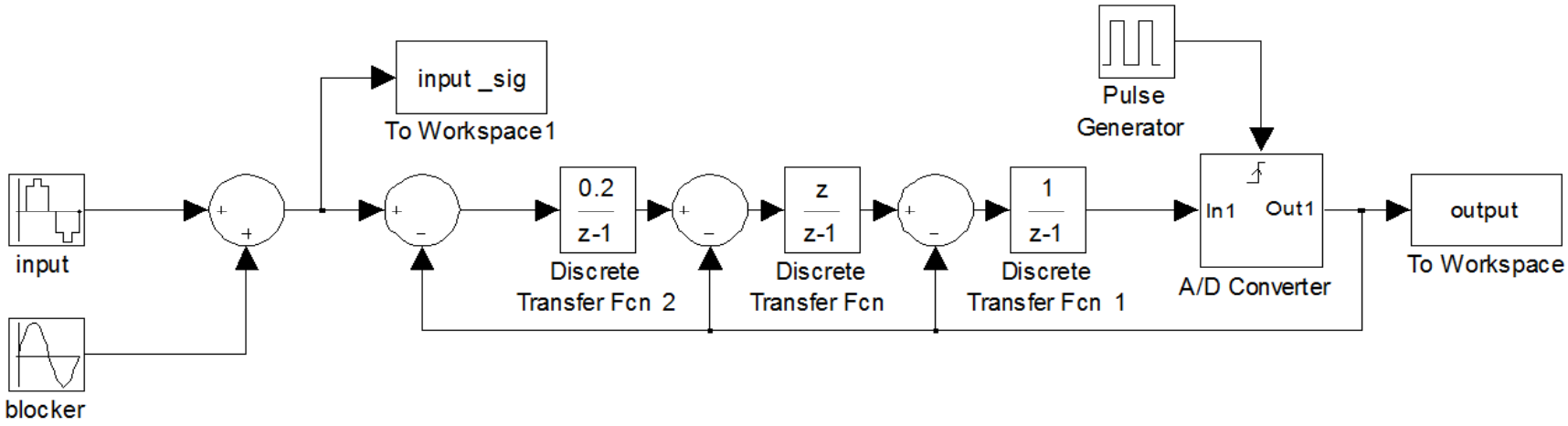

Table of optimized capacitor values

(C_1/C)	(C_2/C)	(C_3/C)	(C_4/C)	(C_5/C)
0.52	-0.64	1.24	-0.64	0.52