An Anti-Aliasing Multi-Rate ΣΔ Modulator

Anthony Chan Carusone
Department of Electrical and Computer Engineering
University of Toronto, Canada

Franco Maloberti
Department of Electronics
University of Pavia, Italy

***Abstract* ? By splitting the input sampling capacitor of a ΣΔ modulator into several time-interleaved branches, FIR filtering can be incorporated into the signal transfer function. Doing so imposes little or no overhead in the design of the opamps. Simulations of a 3rd-order modulator demonstrate that up to 65dB of anti-aliasing can be obtained with 5 time-interleaved switched capacitor branches.**

I. Introduction

There are many examples of mixed-signal systems that require analog filtering and analog-to-digital conversion. Typically the analog input comprises a bandlimited desired signal plus broadband interference and noise and as shown in Figure 1. A common arrangement of the analog-digital interface is shown in Figure 2 comprising an analog lowpass anti-aliasing filter and ΣΔ modulator followed by digital decimation and lowpass filtering.

Given a modulator sampling rate of f_s and oversampling ratio OSR, the signal of interest is bandlimited to $f_s/(2OSR)$. Sampling causes signal content around integer multiples of f_s to be aliased directly on top of the desired signal. Hence, the anti-aliasing filter (AAF) must attenuate these alias prior to sampling. The signal content labeled "Out-of-band interference" in Figure 1 can be eliminated by either the AAF, digital signal processing following the ΣΔ modulator, or any combination of the two.

Much work has been done exploring different combinations of analog continuous-time, analog discrete-time, and digital signal processing to perform the required filtering. Continuous-time filters introduce no aliasing and so are a natural choice for the AAF. Furthermore, it is well-known that continuous-time ΣΔ modulators can incorporate anti-alias and out-of-band interference filtering right inside the ΣΔ modulator. However, discrete-time switched capacitor modulators have better immunity to clock jitter and better accuracy in setting the modulator coefficients. Hence, some have tried to combine the advantages of both by realizing "hybrid" ΣΔ modulators where one or two continuous-time integrators are followed by one or more discrete-time integrators [1][2][3][4][5], but the continuous-time circuitry still requires jitter-suppression and tuning circuitry [1].

Alternatively, the ΣΔ modulation and much of the AAF may be performed in discrete-time. The first stage of the discrete-time AAF operates at a frequency greater than the Nyquist rate relaxing the requirements of the preceding AAF. Its output then is down-sampled by subsequent discrete-time filter stages or the analog-to-digital converter (ADC) itself. The result is a "multi-rate" discrete-time filter [6][7].

This work proposes multi-rate ΣΔ modulators that pre-filter the input by operating the switched-capacitor front-end at a sampling frequency Mf_s, M-times faster than the following stages. The resulting signal path is shown in Figure 3. There is no continuous-time circuitry in the modulator; all transfer functions are determined by capacitor ratios and no tuning is required. Furthermore, the modulator employs a switched-capacitor feedback digital-to-analog converter (DAC) making it relativley insensitive to jitter. The technique places little or no additional requirements on the opamps in the modulator, and unlike double-sampling techniques does not cause down-conversion of quantization noise.

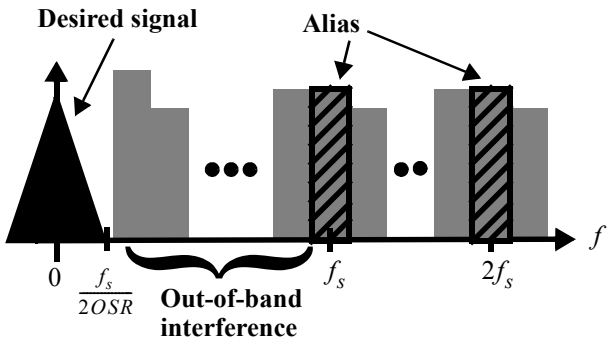

Figure 1. Typical broadband input spectrum comprising the desired baseband signal and interference at higher frequencies.

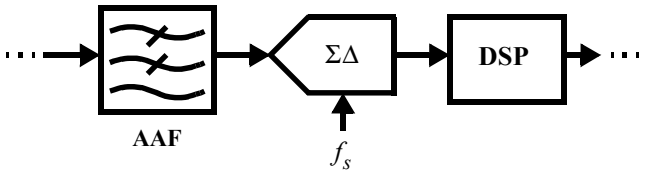

Figure 2. A typical mixed-signal processing system comprising an analog anti-aliasing filter (AAF) and ΣΔ modulator followed by digital decimation and lowpass filtering (DSP).

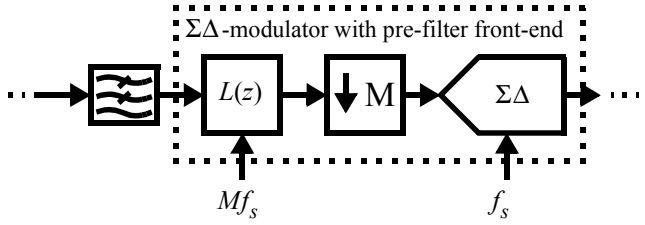

Figure 3. A multi-rate analog front-end incorporating a discrete-time FIR filter at a sample rate Mf_s into the ΣΔ modulator operating at f_s.

II. Multi-Rate Modulators

It is possible to perform a few taps of analog finite impulse response (FIR) filtering by interleaved sampling of a signal onto switched-capacitors. Such a circuit has been used for analog decimation [8][9] and a similar approach was applied at the input of a successive approximation ADC (SAR) in [10]. However, whereas the SAR can not begin conversion until after all samples have been collected [10], in this work a scheme for multi-rate sampling in a ΣΔ modulator is presented with little or no overhead.

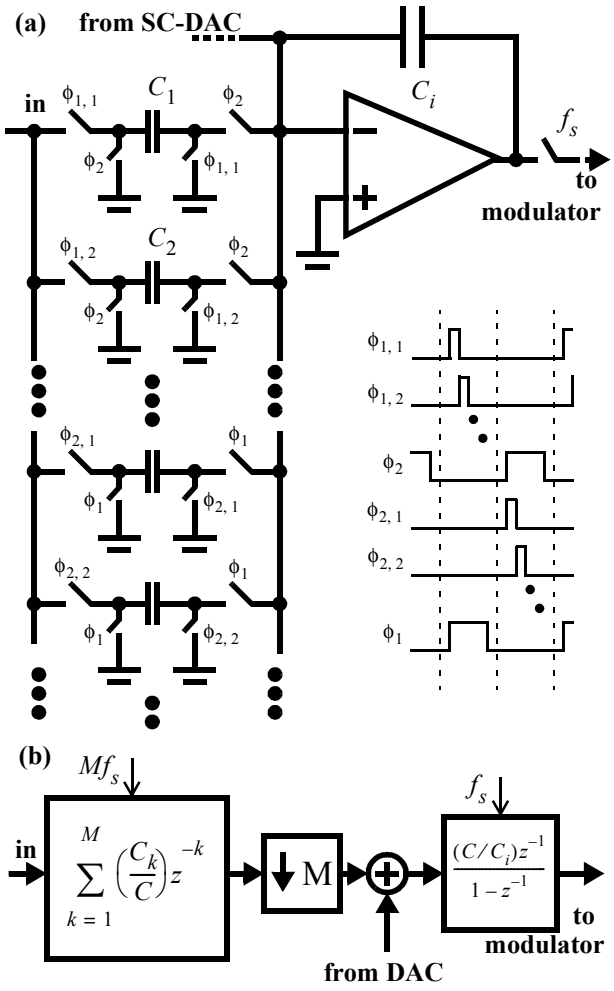

Figure 4. A possible implementation of a multi-rate $\Sigma\Delta$ modulator: (a) simplified schematic; (b) signal flow graph.

Shown in Figure 4a is a first stage where the input sampling capacitor, C, is split into M sampling capacitors $C_1, C_2, \ldots C_M$ so that

$$\sum_{k=1}^{M} C_k = C. \tag{1}$$

The input voltage is sampled onto each of the input capacitors by equally-spaced clocks, $\phi_{1,1}, \phi_{1,2}, \ldots \phi_{2,1}, \phi_{2,2} \ldots$, each operating at the modulator sampling frequency, f_s. These samples are summed and integrated onto C_i along with charge from the feedback DAC which is built from a separate switched-capacitor bank. Subsequent stages operate as usual at the sampling frequency f_s.

Since the input in Figure 4a is sampled at M times per period at equally-spaced intervals, it is effectively sampled at Mf_s. Different parts of the modulator in Figure 4 operate with different sampling frequencies, so it is referred to as a "multi-rate" modulator. However, unlike the multi-rate modulator in [11], all integration is performed at the same rate. The second stage of the modulator is a conventional switched-capacitor integrator operating at f_s and hence downsamples the first integrator's output by a factor M. This results in aliasing from all integer multiples of f_s just as in a coventional modulator, but these alias frequencies are already attenuated by the first-stage operating at Mf_s.

Specifically, the proposed front-end may be modeled as in Figure 4b. The higher sampling frequency front-end filters the input with a transfer function,

$$L(z) = \sum_{k=1}^{M} \left(\frac{C_k}{C}\right) z^{-k}. \tag{2}$$

The finite impulse response filter's M tap-weights are determined by the size of the input sampling capacitors, C_k. These can be chosen to provide the desired pre-filtering prior to downsampling.

A. Rectangular Pre-Filter

A special case is a rectangular FIR response where the total capacitance C is split into M equal-sized sampling capacitors,

$$C_k = C/M, \quad \forall\ 1 \le k \le M \tag{3}$$

This choice results in minimal circuit overhead. The total capacitor area is the same as in a conventional architecture. Furthermore, the total charge delivered to the integraing capacitor each period is the same as in a conventional architecture, so opamp slew rate requirements are unaffected. Note that letting M increase to a very large value would result in a practically continuous integration of the input, as is performed by hybrid modulators [1][2][3][4][5]. However, a multi-rate modulator does not require time-constant tuning or clock jitter reduction circuitry as in [1].

The front-end transfer function is,

$$L(z) = \sum_{k=1}^{M} \left(\frac{1}{M}\right) z^{-k} \tag{4}$$

which has $(M-1)$ zeros equally spaced around the unit circle,

$$z_z = e^{j\left(\frac{2\pi}{M}\right)m}, \quad \forall\ 1 \le m \le M-1 \tag{5}$$

thus providing notches at the first $(M-1)$ alias frequencies, $kf_s, k = 1, 2, \ldots (M-1)$. The frequency response is illustrated in Figure 5. For a low OSR, one problem with this choice is that the notches are very narrow so that signal content around the edge of the alias bands is attenuated much less than signal content very close to $kf_s, k = 1, 2, \ldots (M-1)$.

B. Optimized Pre-Filter

Instead, one may optimize the size of the capacitors for some other response. For example, one may wish to eliminate the input spectral content in the first alias frequency band around f_s. The results of a least-squares optimization are shown for the case $M = 5$ in Table I. With $M < 5$, the best possible anti-aliasing is provided by taking $C_k = (C/M)$.

These zero locations provide a broader stopband around the first alias frequency, as shown in Figure 5. However, the aliases around $2f_s$ and $3f_s$ are actually amplified. Of course, even trivial

TABLE I. FRONT-END CAPACITANCE VALUES OPTIMIZED USING A LEAST-SQUARES FIT FOR $M = 5$ AND $OSR = 24$.

(C_1/C)	(C_2/C)	(C_3/C)	(C_4/C)	(C_5/C)
0.52	-0.64	1.24	-0.64	0.52

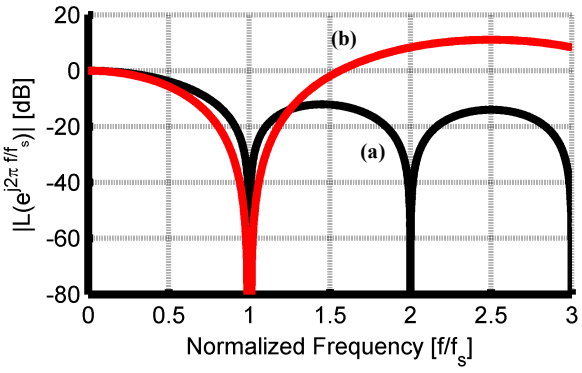

Figure 5. Frequency response of the front-end: (a) $M = 5$ with rectangular coefficients $C_k = (C/M)$; (b) coefficients optimized for maximum attenuation of the first alias and $OSR = 24$.

continuous-time anti-aliasing filter is likely to provide sufficient attenuation at those higher frequencies. Also note that two of the capacitor values in Table I are negative. This is, of course, easily realized in a fully-differential implementation, but does increase the total sampling capacitance at the input which may increase the demands placed on preceding stages and the opamps.

III. Practical Considerations

A. Opamp settling time

With a properly designed clocking scheme, the opamp gain-bandwidth requirements may actually be reduced by using a multi-rate front-end. The clock waveforms shown in Figure 4a provide a half-period for integration just as in a convetional front-end, but only half of the sampling capacitors are integrated in each half-period. For example, Figure 6 shows the equivalent circuits for both the conventional and multi-rate front-ends during the integration phase. With the sampling capacitor sizes chosen as in (3) for a rectangular pre-filter, the feedback gain is clearly greater in Figure 6b.

$$\beta_{\text{conv.}} = \frac{C_i}{C_i + C_{in} + C} < \frac{C_i}{C_i + C_{in} + \left(\frac{C}{2}\right)} = \beta_{\text{multi-rate}} \quad (6)$$

Hence, an opamp with lower gain-bandwidth can be used.

Faster settling is required during input sampling due to the short sampling phases, $\phi_{1,i}$ and $\phi_{2,i}$. However, this is more readily accomodated since the samplers are passive. Furthermore, this may be alleviated somewhat by extending the sampling phases to the beginning of each half-period, as in [2]. Circuitry to generate suitable clocks is described in [2].

B. Capacitor mismatch

For the special case $M = 2$ with $C_1 = C_2 = C/2$, the front-end becomes an example of the well-established double-sampling scheme (DSS) [12]. DSS are plagued by mismatch which causes quantization noise and blockers near f_s to be down-converted to low frequencies [13].

Here, only the input is sampled at Mf_s, and is immediate down-sampled to the normal sampling frequency, f_s, after the first stage. Therefore, mismatch in the size of the sampling capacitors

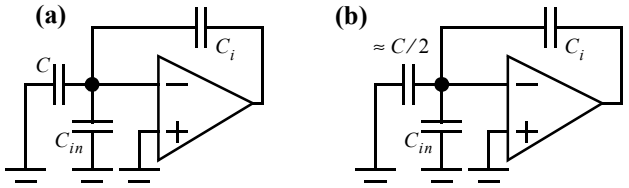

Figure 6. Opamp feedback during integration phase: (a) conventional front-end; (b) multi-rate front-end.

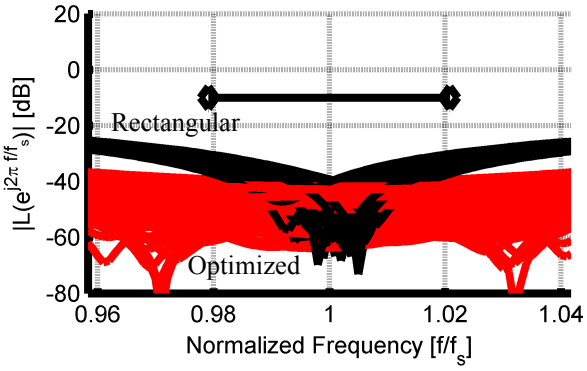

Figure 7. Ensemble of 100 frequency responses, $L(e^{j2\pi f/Mf_s})$, with 0.2% standard deviation capacitor mismatch. The alias frequency band is identified for $OSR = 24$.

C_k does not result in downconversion from f_s, only to some inaccuracy in the coefficients of the FIR transfer-function $L(z)$. The DAC operates at the normal sampling frequency, f_s, on its own switched-capacitor bank just as in a conventional $\Sigma\Delta$ modulator, so capacitor mismatch in the DAC may be corrected using conventional dynamic element matching techniques.

C. Clocking

Skew in the distribution of the clock signals ϕ_k results in harmonic distortion of the input. For an input at f_{in}, tones will appear at $f_s \pm f_{in}$ and also around higher integer multiples of f_s. The effect is quantified in [10] for the case $M = 2$. Fortunately, since the $\Sigma\Delta$ modulator is oversampled anyway, these harmonics are well outside of the band of interest and can be filtered digitally.

The clocking scheme for the multi-rate front end shown in Figure 4a requires the switched-capacitor samplers to settle up to $M\times$ faster than in a conventional front-end. This will necessitate larger sampling switches introducing some overhead into the clock generation circuitry. Clock generation is considered in detail in [2].

IV. Simulation Results

To quantify the potential advantages of a multi-rate $\Sigma\Delta$ converter, a 3rd-order modulator with an oversampling ratio of OSR=24 was behaviourally simulated. The input signal comprises a -2dBFS in-band tone and an "alias" tone at $(1 - 0.45/OSR)f_s$. In a conventional modulator, the alias appears in-band with no attenuation. An example output spectrum is shown in Figure 8a for a -30dBFS alias tone, resulting in a SNDR of only 28.5dB at the output of the modulator. Introducing a multi-rate front-end with $M = 5$ and $C_k = (C/5)$ improves the SNDR to 62.3 dB, still limited by the alias tone. Optimizing the capacitor values as in Table I results in a SNDR of 84.3dB limited by quantization noise.

Figure 9 shows the modulator's output SNDR versus the amplitude of the interfering alias tone. It indicates that over 30dB of anti-aliasing is provided by the simple "rectangular" FIR front-end filter, and an additional 35dB is provided when the coefficients are optimized to suppres the first alias at a frequency around f_s for a total of approximately 65dB of anti-aliasing. This, of course, may be translated into a significant savings in whatever continuous-time AAF preceeds the modulator.

V. Conclusions

Taking time-interleaved samples at the input of an oversampling converter can incorporate FIR filtering into the signal transfer function with little or no circuit overhead. The technique is robust with respect to capacitor mismatch. Up to 65dB of anti-aliasing was demonstrated in a 3rd-order modulator with a 5-tap filter.

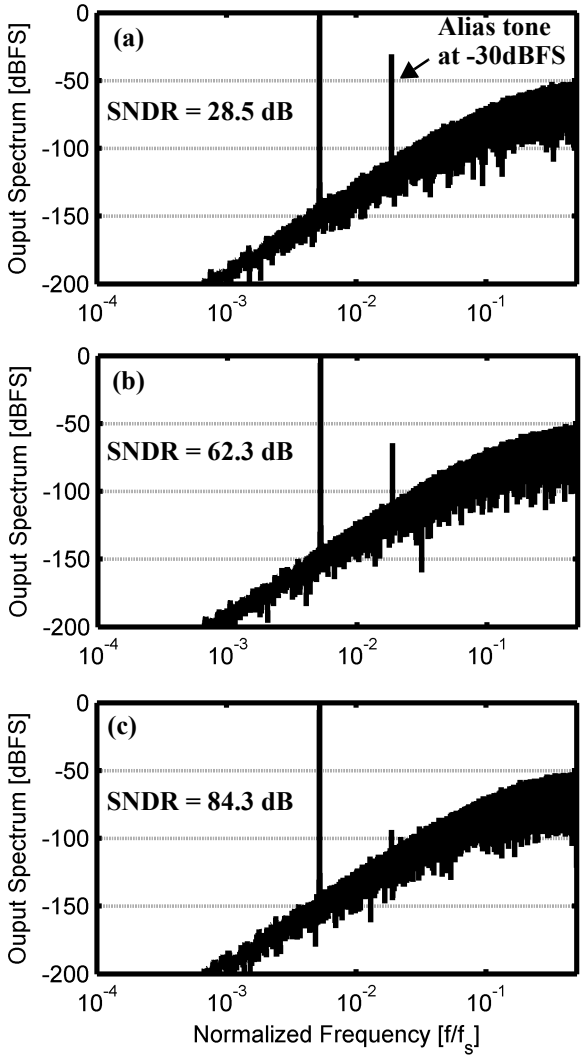

Figure 8. Modulator output spectra with a -30 dBFS alias tone at $(1 - 0.45/OSR)f_s$ and an input of -2dBFS 3rd-order modulators with $OSR = 24$: (a) conventional front-end; (b) front-end with $M = 5$ and $C_k = C/M$; (c) a front-end with capacitance values optimized as in Table I.

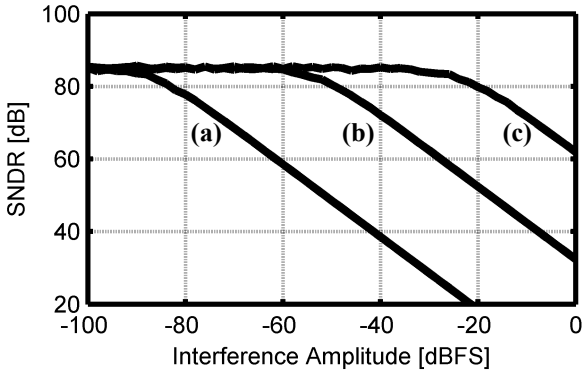

Figure 9. SNDR of 3rd-order modulators with $OSR = 24$ and an interfering signal at $(1 - 0.45/OSR)f_s$ versus the interfering signal amplitude: (a) conventional front-end; (b) multi-rate with $M = 5$ and $C_k = C/M$; (c) multi-rate front-end with capacitance values in Table I.

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