Modeling and Design of Multilevel Bang–Bang CDRs in the Presence of ISI and Noise

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***Abstract*—Multilevel clock-and-data recovery (CDR) systems are analyzed, modeled, and designed. A stochastic analysis provides probability density functions that are used to estimate the effect of intersymbol interference (ISI) and additive white noise on the characteristics of the phase detector (PD) in the CDR. A slope detector based novel multilevel bang–bang CDR architecture is proposed and modeled using the stochastic analysis and its performance compared with a typical multilevel Alexander PD-based CDR for equal-loop bandwidths. The rms jitter of the CDRs are predicted using a linear jitter model and a Markov chain and verified using behavioral simulations. Jitter tolerance simulations are also employed to compare the two CDRs. Both analytical calculations and behavioral simulations predict that at equal-loop bandwidths, the proposed architecture is superior to the Alexander type CDR at large ISI and low signal-to-noise ratios.**

***Index Terms*—Alexander phase detector (PD), bang–bang PDs, clock-and-data recovery (CDR), intersymbol interference (ISI), minimum mean squared error (MMSE) timing recovery, multilevel serial links.**

I. Introduction

SWITCHING and routing data via bandlimited channels have become the design bottleneck in high-speed serial links due to the dramatic increase in data traffic. As a result, the electrical path from one die to another is being plagued by severe levels of intersymbol interference (ISI) due to dispersion arising from frequency dependent channel characteristics such as skin effect, dielectric losses and reflections. Pulse amplitude modulation (PAM) has been proposed as a bandwidth-efficient alternative to nonreturn-to-zero (NRZ) signalling since it mitigates the undesirable characteristics of channels by lowering the symbol rate. Extensive work has been done on high-speed CMOS based clock-and-data recovery (CDR) circuits employing NRZ signalling [1]–[3]. However, CDR design for PAM signals is more challenging compared to its NRZ counterpart due to the presence of a multitude of different data transitions in the multilevel signal [4]–[7]. This work proposes a multilevel CDR scheme that does not use data transitions for phase detection and clock recovery.

At present, one of the most widely used CDR techniques is the bang–bang loop which updates the voltage-controlled oscillator (VCO) by a fixed amount of phase irrespective of the phase error. Analysis of bang–bang loops is complicated due to the inherent nonlinearity of the phase detector (PD). An attempt to linearize the loop in [8] by using an approximation to Gaussian input noise resulted in a square-root dependence of output jitter on input jitter for a 100% edge density. In [9], a piecewise-linear model of a bang–bang loop is introduced in which the effect of slewing is utilized to derive expressions for jitter transfer, jitter tolerance and jitter generation. In [10], the effect of ISI, transmitter noise and receiver noise on the performance of a bang–bang loop is analyzed leading to the conclusion that ISI errors dominate the low bit-error rate (BER) analysis. However, none of these references provide an analysis of how deterministic and random noise sources influence the gain of the bang–bang PD and how the CDR should be designed in the presence of these noise sources to meet given specs (such as loop bandwidth, jitter peaking, etc.). We address this by defining the PD gain as the slope of the PD output probability curves, which are found from the knowledge of the channel and noise statistics. The analysis is easily extended to multilevel PAM. Two multilevel CDRs are analyzed using the model: an Alexander PD based CDR and a novel technique based on minimum mean squared error (MMSE) timing recovery. Sinusoidal VCO noise and transmitter noise is introduced in behavioral simulations to verify the loop bandwidth predicted by the model and to estimate the jitter tolerance, respectively. Thus, the techniques developed in this work allow us to model the effects of noise and ISI on bang–bang PDs. This allows us to choose the PD with the best performance (lowest rms jitter, higher jitter tolerance) for a certain level of ISI and random noise.

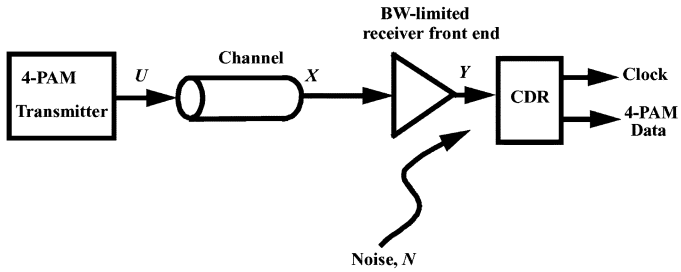

Fig. 1. 4-PAM system model.

Fig. 1 shows the system to be modeled. The 4-PAM signal is transmitted through a bandlimited channel which leads to ISI. At the receiver end, the signal is further corrupted by additive noise and then fed into the receiver front-end which may exacerbate the ISI. The CDR recovers the clock signal which is used to sample the received signal and recover the transmitted data. The paper is organized as follows. Section II discusses relevant background concepts and introduces a linear jitter model [8]. Section III derives a probability density function (PDF) using

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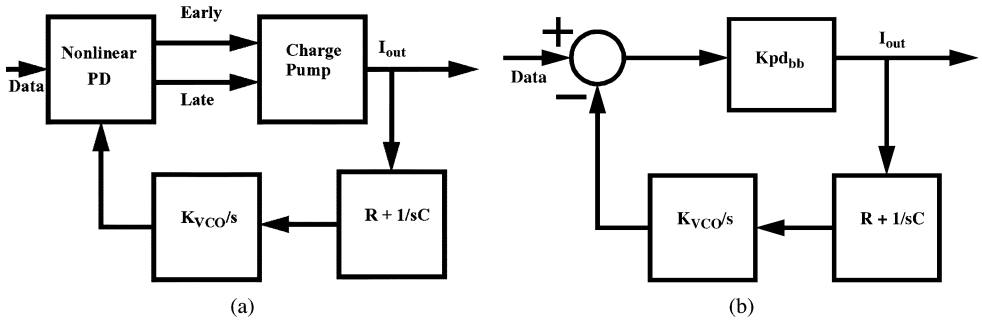


Fig. 2. Bang–bang PLL. (a) Block diagram. (b) Linearized model.

a stochastic analysis. The PDF is modified to model Alexander PDs and a novel multilevel PD based on MMSE timing recovery in Section IV. In Section V, the two CDRs are compared with respect to different non idealities such as ISI, random noise, sinusoidal VCO jitter and jitter tolerance. Finally, the paper concludes with comments on VLSI realizations of the two CDRs (Section VI).

II. Background

A block diagram of a nonlinear (bang–bang) CDR loop is shown in Fig. 2. From the analysis of bang–bang loops described in [8] the bang–bang phase update is defined as

$$\theta_{\rm bb} = \frac{IRK_{\rm VCO}}{f_{\rm clk}} \tag{1}$$

where I is the charge pump current in amps, $f_{\rm clk}$ is the clock frequency in hertz, $K_{\rm VCO}$ is the VCO gain in radians per voltage seconds, and R is the resistance of the loop filter in ohms. For large damping factor ($\zeta = (R/2)\sqrt{K_{\rm pd}CK_{\rm VCO}}$), the loop bandwidth of a second-order linear loop can be approximated as [11]

$$\omega_{-3\ {\rm dB}} \approx K_{\rm pd}K_{\rm VCO}R \tag{2}$$

where $K_{\rm pd}$ is the gain of the PD and charge pump in amps per radian ($K_{\rm pd} = I/2\pi$ for a linear phase-locked loop (PLL) [11]). Equation (2) is accurate within 1.6% for $\zeta > 4$. Substituting (1) in (2), the loop bandwidth of a bang–bang PLL can be expressed as

$$\omega_{-3\ {\rm dB_{bb}}} = 2\pi f_{-3\ {\rm dB_{bb}}} = \frac{\theta_{\rm bb}f_{\rm clk}}{I}K_{\rm pd_{bb}}. \tag{3}$$

Here, $K_{\rm pd_{bb}}$ is the gain of the bang–bang PD which has yet to be defined. Since the bang–bang PD drives a charge pump, the average output of the charge pump ($= E[I_{\rm out}]$) can be expressed in terms of the charge pump current I, and sampling phase τ

$$E\left[I_{\rm out}(\tau)\right] = -IP_{\rm early}(\tau) + IP_{\rm late}(\tau) = I - 2IP_{\rm early}(\tau) \tag{4}$$

where $P_{\rm early}$ denotes the probability of obtaining an early pulse at the output of the PD and $P_{\rm late} = 1 - P_{\rm early}$ is the probability of a late pulse. The gain or sensitivity of the bang–bang PD can be expressed as

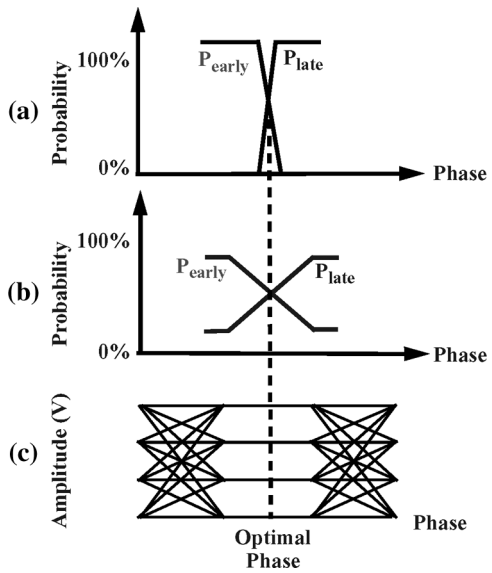


Fig. 3. Effect of ISI and noise on PD characteristics. (a) Ideal bang–bang PD. (b) Bang-bang PD in ISI and noise. (c) 4-PAM Received eye diagram.

$$K_{\rm pd_{bb}} = \frac{dE\left[I_{\rm out}(\tau)\right]}{d\tau}\Big|_{\tau=\tau_{\rm lock}} = -2I\frac{dP_{\rm early}}{d\tau}\Big|_{\tau=\tau_{\rm lock}}. \tag{5}$$

Substituting (5) in (3)

$$f_{-3\ {\rm dB_{bb}}} = -\left[\frac{\theta_{\rm bb}f_{\rm clk}}{\pi}\right]\left[\frac{dP_{\rm early}}{d\tau}\Big|_{\tau=\tau_{\rm lock}}\right]. \tag{6}$$

Equation (6) computes the loop bandwidth by linearizing the bang–bang PD and is valid as long as the bang–bang phase update, ($= \theta_{\rm bb}$) is small enough to keep the PD operating within the range of constant $K_{\rm pd_{bb}}$ or approximately constant slope of the $P_{\rm early}$ and $P_{\rm late}$ curves shown in Fig. 3. Note that ISI and noise effect the slope of the $P_{\rm early}$ and $P_{\rm late}$ curves shown in Fig. 3(a) and (b) and hence the gain of the PD. The statistical properties of the PD (i.e., the $P_{\rm early}$ and $P_{\rm late}$ curves) can be estimated if the PDF at the input to the CDR is known. This is dealt with in the next section. Furthermore, once the $P_{\rm early}$ and $P_{\rm late}$ versus sampling phase curves are known, the rms jitter in the recovered clock (neglecting sources of noise and jitter within the

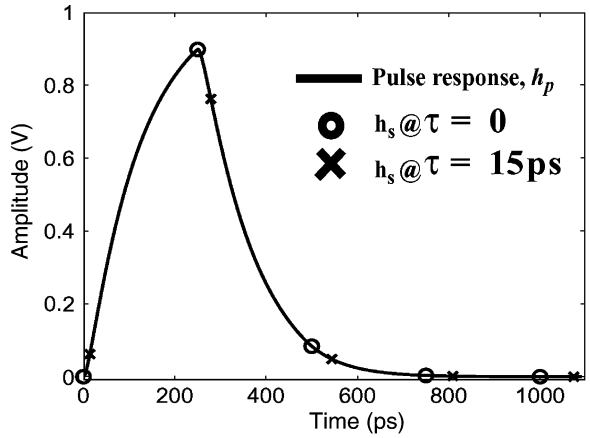


Fig. 4. Pulse response h_p of a typical serial link that consists of a coaxial cable channel model and first-order receive filter.

loop) can be estimated following the linearized analysis in [8]. The resulting rms jitter (in radians) can therefore be expressed as

$$\sigma_{\rm rms} = \sqrt{I\frac{\theta_{\rm bb}}{4K_{\rm pd_{bb}}}}. \tag{7}$$

Substituting (3) in (7) we get

$$\sigma_{\rm rms} = \frac{\sqrt{2\pi}}{-4\frac{dP_{\rm early}}{d\tau}|_{\tau=\tau_{\rm lock}}}\sqrt{\frac{f_{-3\ {\rm dB_{bb}}}}{f_{\rm clk}}}. \tag{8}$$

Equation (8) relates the loop bandwidth and the statistical properties of the PD to the rms jitter of the recovered clock. Note that for a fixed-loop bandwidth, a CDR's recovered clock jitter is inversely proportional to the slope of its $P_{\rm early}$ versus phase curves in the vicinity of the lock point. If the recovered clock jitter is high, the clock phase, τ will wander over a range for which the slope $dP_{\rm early}/d\tau$ is no longer constant making it difficult to apply (8). This variation in $dP_{\rm early}/d\tau$ can be taken into account by using a random walk model or Markov chain [12]. In this work, both the linear model in (8) and the Markov chain will be used to predict the rms jitter of the CDR.

III. Stochastic Modeling of CDR Input

The purpose of this section is to obtain an expression for the PDF of the input signal to the CDR (which is labelled as Y in Fig. 1) as a function of sampling phase, τ, from a knowledge of the channel response, the receiver front-end, and the additive noise. This expression can then be used to evaluate the $P_{\rm early}$ and $P_{\rm late}$ curves for the bang–bang CDR and eventually the gain of the PD.

A. Effect of Channel Response

The analysis assumes that the pulse response of the channel is known. Fig. 4 shows a typical pulse response, $h_p(t)$, of the entire path from transmitter to the CDR input. Included in $h_p(t)$ is a coaxial cable model used as the channel and a receiver front-end modeled as a first-order low-pass filter

$$H_{\rm LPF}(s) = \frac{1}{1+sT_c}. \tag{9}$$

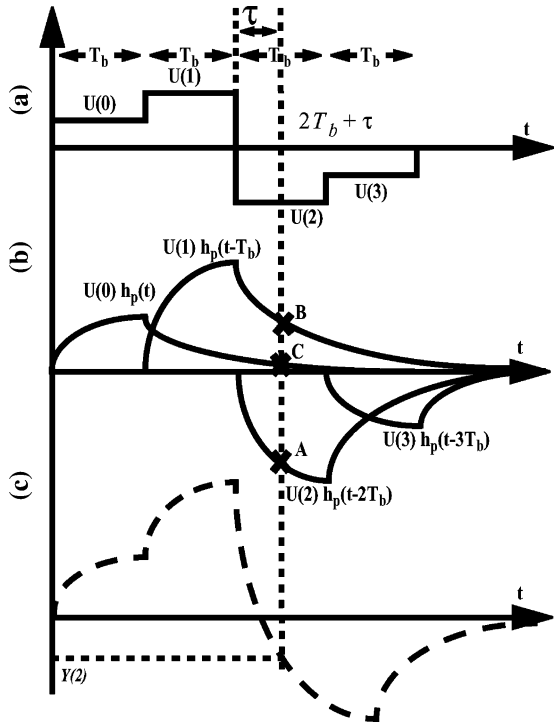


Fig. 5. Example of computing a sampled voltage at a particular sampling phase. (a) Transmitted symbols. (b) Received pulses (with ISI). (c) Received signal.

The input to the CDR can be expressed as

$$Y(t) = \sum_{k=-\infty}^{\infty} U(k)h_p(t-kT_b). \tag{10}$$

Here U is the random data input to the channel and Y is the receiver front-end output. Fig. 5 illustrates how previous symbols interfere with the current bit to produce the sampled voltage at any particular sampling phase. Fig. 5(a) shows a sequence of transmitted symbols. Neglecting the channel delay, the channel outputs a sequence of pulses, each pulse being weighted by the corresponding transmitted symbol. This is shown in Fig. 5(b). The received signal is a sum of these pulses. Thus, at time $t = 2T_b+\tau$ the receiver sampled voltage $Y(2)$ can be expressed as a sum of points A, B, and C in Fig. 5(b) where A is the sample of the current symbol and B, C are samples of previous symbols. Let h_s be the baud rate samples of h_p for a particular sampling phase τ. For instance, Fig. 4 plots h_s for two different sampling phases: $\tau = 0$ and $\tau = 15$ ps. Thus, h_s can be expressed as

$$h_s(k) = h_p(kT_b+\tau). \tag{11}$$

Substituting (11) in (10) we get

$$Y(lT_b+\tau) = \sum_{k=-\infty}^{\infty} U(k)h_s(l-k). \tag{12}$$

The infinite sum in (12) can be made finite by neglecting the negligible tails of $h_s(k)$ outside the range $0 \le k \le m$

$$Y(l) = \sum_{k=0}^{m} U(k)h_s(l-k). \tag{13}$$

For a finite h_s of length $m+1$, there are 4^{m+1} possible sequences of transmitted 4-PAM data: $U(0), U(1), \ldots\ldots U(m)$. Let $\mathbf{A}$ be a $4^{m+1} \times (m+1)$ matrix whose rows are all of the possible transmitted 4-PAM data patterns of length $m+1$ and $A(q,r)$ be the element of A in row q and column r. Hence, the channel output corresponding to the data pattern in row q of $\mathbf{A}$ is

$$c_Y(q) = \sum_{r=1}^{m+1} \mathbf{A}(q,r) h_s(m+1-r). \tag{14}$$

Thus, for a particular sampling phase there are 4^{m+1} possible values of the CDR input Y given by (14), each corresponding to a row of the data matrix $\mathbf{A}$. Assuming random uncorrelated data, each sequence will occur with probability $1/4^{m+1}$. Thus, the PDF for the signal Y (assuming no random noise) for a particular sampling phase can be expressed as

$$f_Y(x) = \frac{1}{4^{m+1}} \sum_{q=1}^{4^{m+1}} \delta\left(x - c_Y(q)\right). \tag{15}$$

Note that the data matrix $\mathbf{A}$ can be generalized for line coding by weighting each term of the summation in (15) by the probability of the corresponding data pattern. Some PDs are inactive for certain received data patterns, in which case the corresponding terms in (14) must be omitted.

B. Additive Noise

Noise in the channel and receiver front-end is modeled as an equivalent input referred noise source. If the PDF of the additive noise is $f_N(x)$, then the PDF of the signal Y (Fig. 1) at the input to the CDR for any sampling phase can be obtained by simply convolving f_N and f_Y in (15)

$$f_Y(x) = \frac{1}{4^{m+1}} \sum_{q=1}^{4^{m+1}} f_N\left(x - c_Y(q)\right). \tag{16}$$

For the special case of Gaussian noise

$$f_N(x) = \frac{e^{-x^2/2\sigma^2}}{\sqrt{2\pi\sigma^2}}. \tag{17}$$

Substituting (17) in (16)

$$f_Y(x) = \frac{1}{4^{m+1}\sqrt{2\pi\sigma^2}} \sum_{q=1}^{4^{m+1}} e^{-(x-c_Y(q))^2/(2\sigma^2)}. \tag{18}$$

In essence, the PDF is a sum of Gaussian distributions. The constants $c_Y(q)$ define the means of the Gaussians in terms of the sampled pulse response h_s (deterministic jitter). Each Gaussian has a variance of σ^2 (random jitter). Note that for evaluating c_Y in (18), the entire pulse response from transmitter to the CDR input has to be considered.

TABLE I
PARAMETERS FOR THE SYSTEM IN FIG. 1

Data rate	4 Gsymbol/s=8Gb/s
SNR	43 dB @ input to CDR
Channel	3m coaxial cable (-3dB BW=13.8 GHz)
Receiver front-end bandwidth	4 GHz

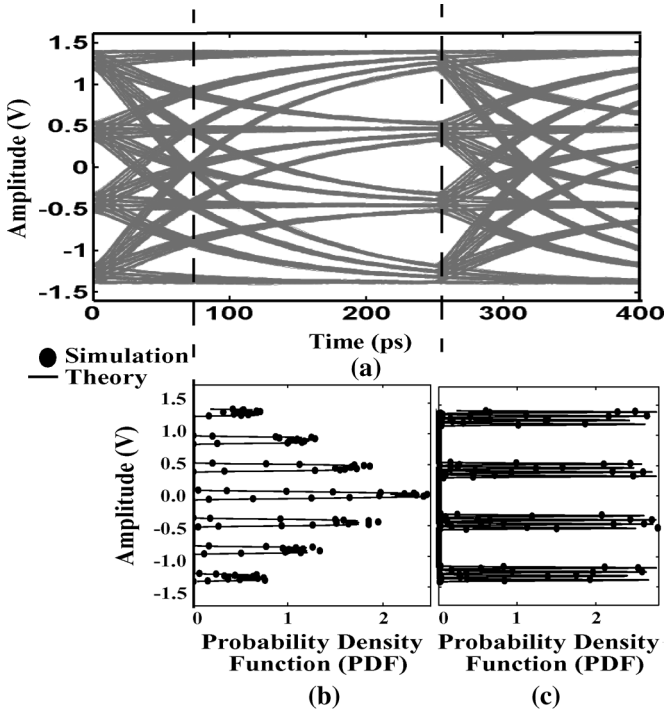


Fig. 6. PDF at two different sampling phases of a given data eye. (a) Eye diagram. (b) PDF at data transition. (c) PDF at maximum data eye opening.

C. System Level Parameters

System level parameters used for behavioral simulations are shown in Table I. The input random data sequence is assumed to be a 4-PAM system with equi-probable values at $+1.5$, 0.5, -0.5, and -1.5. The effect of baseline wander is neglected since the channel is assumed to be dc coupled. Using (18) and the parameters in Table I, the PDF at the input to the CDR is calculated for two different sampling phases (Fig. 6). Good agreement with time-domain simulations in Simulink is also observed. The SNR and the channel length will be varied in subsequent sections to observe the effect of these parameters on CDR performance.

IV. MULTILEVEL CDR ARCHITECTURES

This section attempts to model Alexander PD and MMSE PD-based CDR architectures for multilevel signals using the stochastic analysis in the previous section.

A. Alexander PD-Based CDR

In the presence of data transitions, the Alexander PD [14] generates an early or late pulse depending on whether the clock leads or lags the data. A possible implementation of an Alexander PD modified for 4-PAM signals is shown in Fig. 7 [4]–[7]. The input data is sampled at the rising and falling edges of a full-rate clock. The input being a 4-PAM signal, the sampled values are sent to a bank of clocked comparators

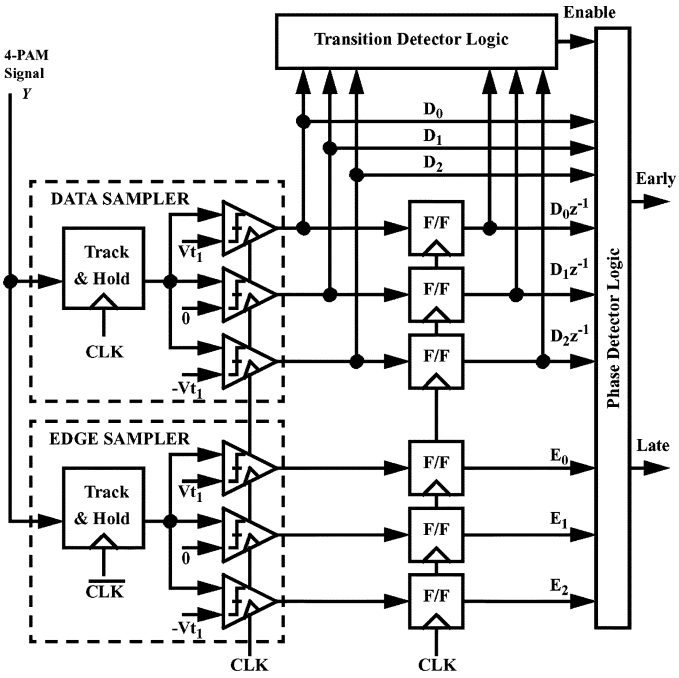


Fig. 7. Block diagram of 4-PAM Alexander PD [4]–[7].

to detect the correct signal level. The choice of the threshold V_{t_1} depends on the input data eye. The usual Alexander PD logic is authenticated by a transition detector which filters out undesired transitions such as $+1.5$ to -0.5 and vice versa. The desired transition types are [7]: 1) Symmetric crossings i.e., transitions from $+1.5$ to -1.5 and vice versa; 0.5 to -0.5 and vice versa; 2) 1.5 to 0.5 and vice versa; 3) -1.5 to -0.5 and vice versa. The PD logic is enabled through a control signal whenever any one of these transitions are detected. For example, if a transition from -1.5 to $+1.5$ is detected then the early/late pulses can be generated through logic gates as

$$\text{Early} = D_1 \oplus E_1; \quad \text{Late} = D_1 z^{-1} \oplus E_1 \tag{19}$$

where D_1 is the current data sample output of the zero threshold clocked comparator (Fig. 7), E_1 is the corresponding edge sample and $D_1 z^{-1}$ is the data sample from the previous period. To determine the P_{early} and P_{late} versus sampling phase curves for this PD, the statistics of the received waveform at data transitions are required. Hence, to model the CDR in lock, the PDF of the transition edge samples is needed.

Fig. 8 shows one of the data transitions of a 4-PAM signal and two PDFs corresponding to different transition edge sampling phases A and B. Sampling phase A leads the zero crossing while sampling phase B lags. For a leading sampling phase, we expect $P_{\text{early}} > P_{\text{late}}$ and *vice versa* for a lagging sampling phase. Note that an early pulse will be generated by the PD whenever the sampled value at the rising data transition edge is below the threshold. Thus, for sampling phase A or B, the probability of an early pulse when the data transitions from -1.5 to $+1.5$ $(= P_{\text{early},Y_{[-1.5\Rightarrow+1.5]}})$ can be expressed as

$$P_{\text{early},Y_{[-1.5\Rightarrow+1.5]}} = \int_{-\infty}^{0} f_{Y_{[-1.5\Rightarrow+1.5]}}(x)dx \tag{20}$$

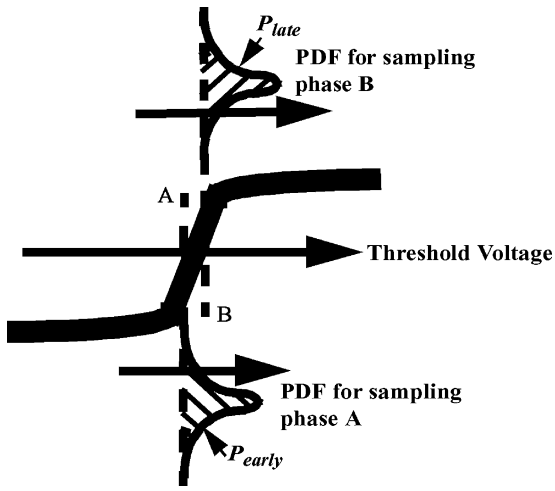


Fig. 8. Example of calculating P_{early} and P_{late} for two different transition edge samples using PDFs.

where $f_{Y_{[-1.5\Rightarrow+1.5]}}(x)$ denotes the PDF corresponding to a transition from -1.5 to $+1.5$ in the 4-PAM signal Y. This PDF can be derived from the PDF in (18) by modifying the data matrix $\mathbf{A}$ to include only rows whose mth and $(m+1)$th columns are -1.5 and $+1.5$, respectively. Consequently, the modified 4-PAM data matrix will have dimensions $4^{m-1} \times (m+1)$. For example, if $m = 2$ the modified data matrix $\mathbf{A}$ can be expressed as[1]

$$\mathbf{A}_{[-1.5\Rightarrow+1.5]} = \begin{bmatrix} -1.5 & -1.5 & 1.5 \\ -0.5 & -1.5 & 1.5 \\ 0.5 & -1.5 & 1.5 \\ 1.5 & -1.5 & 1.5 \end{bmatrix}. \tag{21}$$

Thus, $f_{Y_{[-1.5\Rightarrow+1.5]}}(x)$ can be expressed as

$$f_{Y_{[-1.5\Rightarrow+1.5]}}(x) = \frac{1}{4^{m+1}\sqrt{2\pi\sigma^2}} \sum_{q=1}^{4^{m-1}} e^{-\frac{\left(x - c_{Y_{[-1.5\Rightarrow+1.5]}}(q)\right)^2}{2\sigma^2}} \tag{22}$$

and

$$c_{Y_{[-1.5\Rightarrow+1.5]}}(q) = \sum_{r=1}^{m+1} \mathbf{A}_{[-1.5\Rightarrow+1.5]}(q,r) h_s(m+1-r). \tag{23}$$

Evaluating (22)

$$P_{\text{early},Y_{[-1.5\Rightarrow+1.5]}} = \frac{0.5}{4^{m+1}} \sum_{q=1}^{4^{m-1}} \text{erfc}\left(\frac{c_{Y_{[-1.5\Rightarrow+1.5]}}(q)}{\sqrt{2\sigma^2}}\right) \tag{24}$$

[1]Practically m is much larger than 2. $m = 2$ is chosen here to illustrate the data transition matrix.

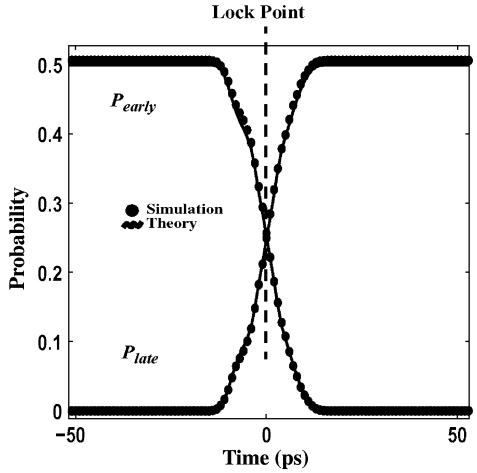


Fig. 9. Plots of $P_{\rm early}$ and $P_{\rm late}$ values for Alexander PD for 13.8-GHz coaxial cable channel model, $\rm SNR = 43$ dB, 4 Gsymbol/s 4-PAM data, and 4-GHz receiver front-end.

where erfc is the complementary error function. Similarly, the probability of a late pulse when the data transitions from -1.5 to $+1.5$ $(= P_{{\rm late},Y_{[-1.5\Rightarrow+1.5]}})$ can be expressed as

$$P_{{\rm late},Y_{[-1.5\Rightarrow+1.5]}} = \frac{0.5}{4^{m+1}} \sum_{q=1}^{4^m-1} {\rm erfc}\left(\frac{-c_{Y_{[-1.5\Rightarrow+1.5]}}(q)}{\sqrt{2\sigma^2}}\right) \tag{25}$$

Similar equations for $P_{\rm early}$ and $P_{\rm late}$ can be derived for other data transition types. Using this method the $P_{\rm early}$ and $P_{\rm late}$ for any sampling phase can be determined for the system shown in Fig. 1 with an Alexander PD in the CDR. Fig. 9 shows plots of $P_{\rm early}$ and $P_{\rm late}$ for different sampling phases. Note that the recovered clock will lock to the sampling phase corresponding to $P_{\rm early} = P_{\rm late}$ if the CDR is stable. After lock is achieved, the behavior of the clock phase can be modeled as a random walk. The bang–bang nature of the CDR will cause the clock sampling phase to be updated by a fixed amount denoted by $\theta_{\rm bb}$. Using (6) the bang–bang phase update $\theta_{\rm bb}$ can be calculated for a particular loop bandwidth once the slope, $dP_{\rm early}/d\tau$ is approximated in the vicinity of the lock point from Fig. 9. Then a random walk model or Markov chain [12] can be utilized to predict the rms jitter corresponding to a particular $\theta_{\rm bb}$. The jitter buildup in the recovered clock versus the number of clock cycles is depicted in Fig. 10(a) for phase updates corresponding to a 10-MHz loop bandwidth. The rms jitter can also be predicted using the linear model in (8).

Once $\theta_{\rm bb}$ is known, the rest of the loop can be designed as in [11] to provide $\zeta > 5$ for jitter peaking $<$0.1 dB. Note that this also satisfies the condition of large stability factor which ensures a dominant proportional path in the bang–bang loop [8]. Thus, the design methodology for the CDR is described as follows (assuming the VCO gain, $K_{\rm VCO}$ is known).

1) The probability curves are estimated for a particular channel, receiver front-end bandwidth and input noise level.
2) The average slope of these curves near the lock point can be used to estimate the charge pump current using (5) for a target PD gain, $K_{\rm pd_{bb}}$. In this work, the target $K_{\rm pd_{bb}}$ is set to 100 μA/rad for all CDRs.
3) The bang–bang phase update, $\theta_{\rm bb}$ can be determined using (6) for a particular loop bandwidth, $f_{-3\ {\rm dBbb}}$. In this work, the target loop bandwidth is set to 10 MHz for all CDRs.
4) The loop resistor can be calculated using (2). In this work $R = 500\ \Omega$.
5) The loop damping factor can be expressed as

$$\zeta = \frac{1}{2}\sqrt{RC\omega_{-3\ {\rm dB}}}. \tag{26}$$

To achieve jitter peaking $<$0.1 dB, ζ needs to be larger than 5 [11]. Thus, (26) places a lower limit on the loop filter capacitance. In this work, $C = 5$ nF and $\zeta = 6.26$.

In summary, the CDR loop parameters are chosen to meet a certain loop bandwidth, PD gain and jitter peaking. Table II shows the parameters for a 10-MHz Alexander CDR. Simulated excess phase of the recovered clock is shown in Fig. 10(b).

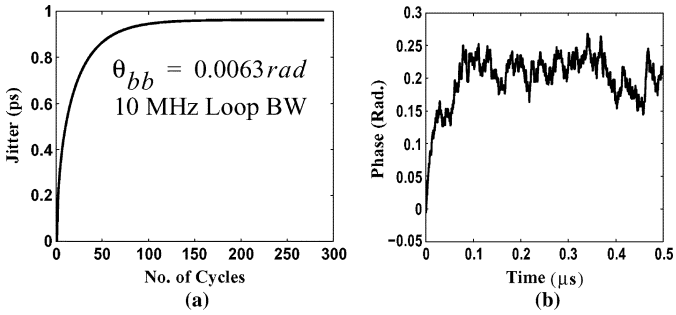


Fig. 10. 10-MHz Alexander CDR characteristics for 13.8-GHz coaxial cable channel, $\rm SNR = 43$ dB and 4 Gsymbol/s 4-PAM data. (a) rms jitter buildup predicted by Markov model. (b) Simulated excess phase variation of 4-GHz clock recovered by Alexander PD-based CDR.

TABLE II
PARAMETERS FOR 10-MHz ALEXANDER PD-BASED CDR

Loop bandwidth (MHz)	10
Charge Pump Current, (μA)	40
VCO gain (MHz/V)	200
θ_{bb}=Bang-bang phase update (rad.)	0.0063
Average PD slope near lock $=-2\frac{dP_{early}}{d\tau}\|_{\tau=\tau_{lock}}$ (/rad)	2.5
PD gain=$K_{pd\,BB}$ (μA/rad)	100
R (Ω)	500
C (nF)	5
RMS jitter using linearized model i.e. Eq. (8) (ps)	0.9939
RMS jitter using Markov model (ps)	0.9627
RMS jitter from simulation (ps)	0.9962
Peak-to-peak jitter from simulation (ps)	6

B. MMSE PD-Based CDR

MMSE timing recovery [12] optimizes the sampling phase in a digital receiver by minimizing the expected value of the squared error

$$E_k = E\left[e_k^2\right] = E\left[\left(U_k - y(kT+\tau_k)\right)^2\right]. \tag{27}$$

Here U_k represents the kth transmitted bit, $y(t)$ the received waveform, T the symbol period, and τ_k the sampling phase for the kth received bit. Note that the optimal sampling phase corresponds to the maximum vertical data eye opening. MMSE re-

quires that the sampling phase, τ_k be adjusted in the direction opposite the gradient, $\delta E_k/\delta\tau_k$

$$\tau_{k+1} = \tau_k - \mu\left(\frac{\delta E_k}{\delta\tau_k}\right). \tag{28}$$

Here μ is a parameter that is chosen to trade-off acquisition time with jitter and determines how quickly τ_k is adjusted. Substituting (27) into (28) and dropping the expectation operator results in the following stochastic gradient update rule:

$$\tau_{k+1} = \tau_k + 2\mu e_k\left(\frac{\delta y(kT+\tau_k)}{\delta\tau_k}\right). \tag{29}$$

Practical high-speed implementations of the LMS algorithm often use only 1-bit representations of the sign of the error and the slope [15]. Applying this idea to MMSE TR results in the following sign–sign MMSE (SSMMSE) rule [16] :

$$\tau_{k+1} = \tau_k + 2\theta_{\rm bb}\,\mathrm{sgn}(e_k)\,\mathrm{sgn}\left(\frac{\delta y(kT+\tau_k)}{\delta\tau_k}\right). \tag{30}$$

Here, $\theta_{\rm bb}$ (the bang–bang phase update) replaces μ. In a practical bang–bang CDR, a small integral term is added to the right side of (30). Thus, to summarize, this method requires the following two quantities: 1) the sign of the slope of the received signal at the sampling instant; 2) the sign of the error between the sampled value and a particular signal level. Once these signals are available in binary form, early/late pulses can be generated using logic gates [16]

$$\text{Early} = D(e \oplus s); \quad \text{Late} = D(e \odot s) \tag{31}$$

where D is the data sample corresponding to a particular signal level. The error with respect to a particular signal level can be generated by a comparator. This will often be required for other purposes as well such as adaptive equalization [17], hence no extra hardware will be necessary.

The algorithm may be simplified by eliminating the error signal altogether. Suppose the PD is monitoring a $+1.5$ level. Thus, the error signal $e = \mathrm{sgn}[y(t) - 1.5]$ where $y(t)$ is the received signal. Note that e will be 0 most of the time since it is highly unlikely that the signal will rise above 1.5. This can be easily seen in the 4-PAM eye diagram of Fig. 6(a). Setting e to zero in (31) results in the following logic:

$$\text{Early} = Ds; \quad \text{Late} = D\bar{s}. \tag{32}$$

A similar modification can be made when monitoring the -1.5 level. The only difference will be that the error signal in this case will be $e = \mathrm{sgn}[y(t) + 1.5]$. Therefore, the error will be 1 most of the time. Besides hardware reduction, another advantage of monitoring the max. and min. signal levels is the lower jitter in the recovered clock [16]. The main challenge in the design is implementing a high-frequency slope detector. One possibility is to use passive RC-CR sections as shown in Fig. 11. The relative phase shift between the data and slope outputs will be 90° over a broad bandwidth. The low-pass and high-pass filters

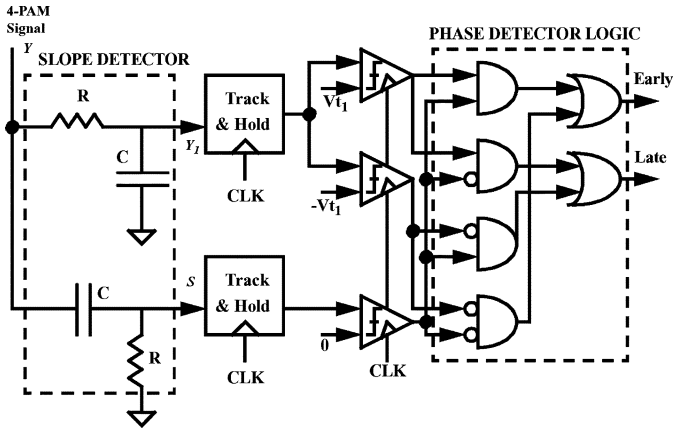


Fig. 11. Multilevel PAM timing recovery using an SSMMSE PD with a full rate clock ($+1.5$ and -1.5 levels are being monitored).

can be realized using on chip passive components. The choice of the filter time constant is a tradeoff between bandwidth of receiver front-end and sensitivity of the slope detector. For this work, $(R_sC_s)^{-1} = 2\pi 10$ Grad/s. As proposed in [18], an active filter may also be used.

Note that in Fig. 11, the early/late decisions of the PD depend on both the signal (Y_1) and the derivative (S) of the signal. Hence, for each sampling phase a PDF can be computed for the signal (Y_1) and a corresponding PDF for the slope (S) by using (18) provided that the slope detector bandwidth is included in the pulse response of the channel. Each of these PDFs will have their own c vectors (i.e., c_{Y_1} and c_S) corresponding to each possible combination of data. Since the phase update depends on both of these two signals, a joint PDF of these two signals needs to be constructed for each sampling phase. A joint PDF requires the calculation of the correlation-coefficient function ρ which is given as [13]

$$\rho_{Y_1S} = \frac{E[Y_1S] - E[Y_1]E[S]}{\sigma_S\sigma_{Y_1}}. \tag{33}$$

However, it can be shown that this function is zero for a signal and its slope at a particular sampling phase (Appendix). The joint PDF of the signal Y_1 and its slope S for a particular sampling phase can be expressed as

$$f_{Y_1S}(x,z) = K_o\sum_{q=1}^{4^{m+1}} e^{-\frac{1}{2}\left[\left(\frac{x-c_{Y_1}(q)}{\sigma_{Y_1}}\right)^2+\left(\frac{z-c_S(q)}{\sigma_S}\right)^2\right]} \tag{34}$$

where $K_o = [4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)]^{-1}$. Note that the noise variance of the slope signal (σ_S^2), is influenced by the derivative and hence is different from the noise variance of the data signal $(\sigma_{Y_1}^2)$. When the SSMMSE PD is monitoring $+1.5$ level, the probability that an early pulse will be generated for a particular sampling phase can be expressed as

$$P_{\text{early},[Y_1\Rightarrow+1.5]} = \int_{V_{t_1}}^{1.5}\int_{0}^{\infty} f_{Y_1S}(x,z)\,dx\,dz \tag{35}$$

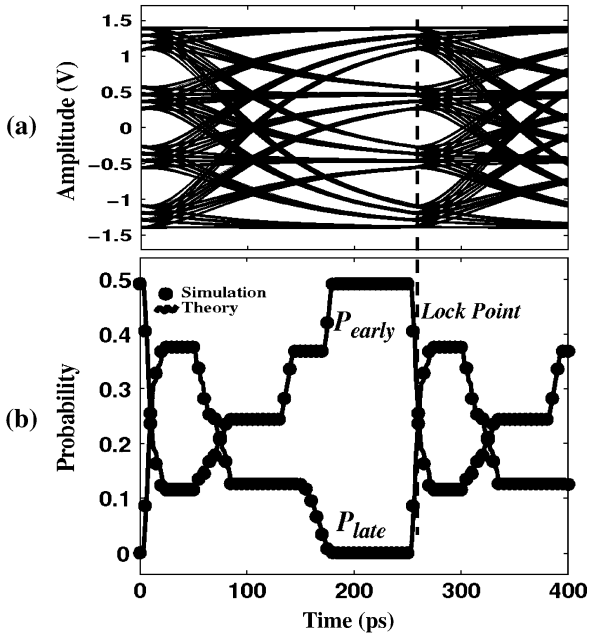


Fig. 12. SSMMSEPD characteristics for 13.8-GHz coaxial cable channel model, $\mathrm{SNR} = 43$ dB, 4 Gsymbol/s 4-PAM data and passive slope detector with 10-GHz cutoff frequency. (a) Eye diagram of CDR input (i.e., signal Y_1 in Fig. 11. (b) Simulated and theoretical P_{early} and P_{late} for SSMMSEPD.

where V_{t_1} represents the threshold voltage of the data comparator [Fig. 11]. Evaluating the integrals in (35)

$$P_{\mathrm{early},[Y_1 \Rightarrow +1.5]} = K_1 \sum_{q=1}^{4^{m+1}} \mathrm{erfc}\left(\frac{-c_S(q)}{\sigma_S\sqrt{2}}\right) \times \mathrm{erf}\left[\frac{1.5 - c_{Y_1}(q)}{\sigma_{Y_1}\sqrt{2}}\right] - K_1 \sum_{q=1}^{4^{m+1}} \mathrm{erfc}\left(\frac{-c_S(q)}{\sigma_S\sqrt{2}}\right) \times \mathrm{erf}\left[\frac{V_{t_1} - c_{Y_1}(q)}{\sigma_{Y_1}\sqrt{2}}\right] \quad (36)$$

where $\mathrm{erf}(.)$ and $\mathrm{erfc}(.)$ denote the error and complementary error function, respectively and $K_1 = 0.25/4^{m+1}$. The probability of obtaining a late pulse (when monitoring $+1.5$ level) can be expressed as

$$P_{\mathrm{late},[Y_1 \Rightarrow +1.5]} = \int_{V_{t_1}}^{1.5} \int_{-\infty}^{0} f_{Y_1 S}(x,z)\,dx\,dz. \quad (37)$$

Similar equations can be derived for early and late pulses when monitoring -1.5 level. Using these equations, the P_{early} and P_{late} for each sampling phase can be determined for the system shown in Fig. 1 with an SSMMSE PD in the CDR. Fig. 12 shows plots of P_{early} and P_{late} for all sampling phases along with the eye diagram of the received data. The rms jitter can now be determined using (8) and a random walk model (Markov chain) for a particular loop bandwidth. Using the design methodology described for the Alexander PD-based CDR, the SSMMSE CDR is designed for 10-MHz loop bandwidth. Table III shows the parameter values of the designed CDR. The jitter buildup predicted by a Markov model is depicted in Fig. 13(a) for phase updates corresponding to a 10-MHz loop bandwidth. Simulated excess phase of the recovered clock is shown in Fig. 13(b). Fig. 14 depicts simulated eye diagrams of the data input to the CDR and the recovered clocks for Alexander PD and SSMMSE PD at 10-MHz loop bandwidth. Note that the lock point for the SSMMSE CDR corresponds to the maximum data eye opening, not the midpoint between data transitions as in the Alexander PD.

TABLE III
PARAMETERS FOR 10-MHz SSMMSE PD-BASED CDR

Loop bandwidth (MHz)	10
Charge Pump Current, (μA)	46
VCO gain (MHz/V)	200
θ_{bb}=Bang-bang phase update (rad.)	0.0072
Average PD slope near lock $=-2\frac{dP_{early}}{d\tau}\|_{\tau=\tau_{lock}}$ (/rad)	2.175
PD gain=$K_{pd\,BB}$ (μA/rad)	100
R (Ω)	500
C (nF)	5
RMS jitter using linearized model i.e. Eq. (8) (ps)	1.146
RMS jitter using Markov model (ps)	1.187
RMS jitter from simulation (ps)	1.186
Peak-to-peak jitter from simulation (ps)	6.02

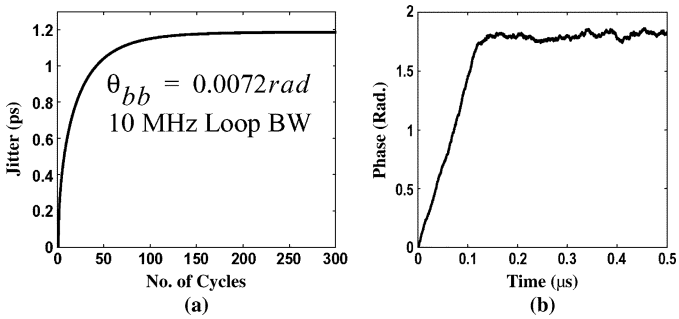


Fig. 13. 10-MHz SSMMSE PD-based CDR characteristics for 13.8-GHz coaxial cable channel model, $\mathrm{SNR} = 43$ dB, 4 Gsymbol/s 4-PAM data and passive slope detector with 10-GHz cutoff frequency. (a) Jitter buildup predicted by Markov model. (b) Simulated excess phase variation of 4-GHz clock recovered by SSMMSE PD-based CDR.

V. EFFECT OF SYSTEM NONIDEALITIES

In this section, the effect of different nonidealities on the CDR performance will be investigated.

A. Effect of Channel Bandwidth

Increasing the channel length reduces the bandwidth of the channel and leads to greater ISI. This degrades the slope of the probability curves (Fig. 3) and results in a larger rms jitter for a fixed-loop bandwidth (8). Fig. 15 plots the slope of the probability curves and rms jitter of Alexander and SSMMSE PD-based CDR as a function of channel bandwidth. All Table I parameters for the 4-PAM system depicted in Fig. 1 were kept intact except the channel length. Both simulations and calculations predict that at large channel bandwidths, Alexander performs better than SSMMSE. However, at lower channel bandwidths, SSMMSE is superior to Alexander PD-based CDR.

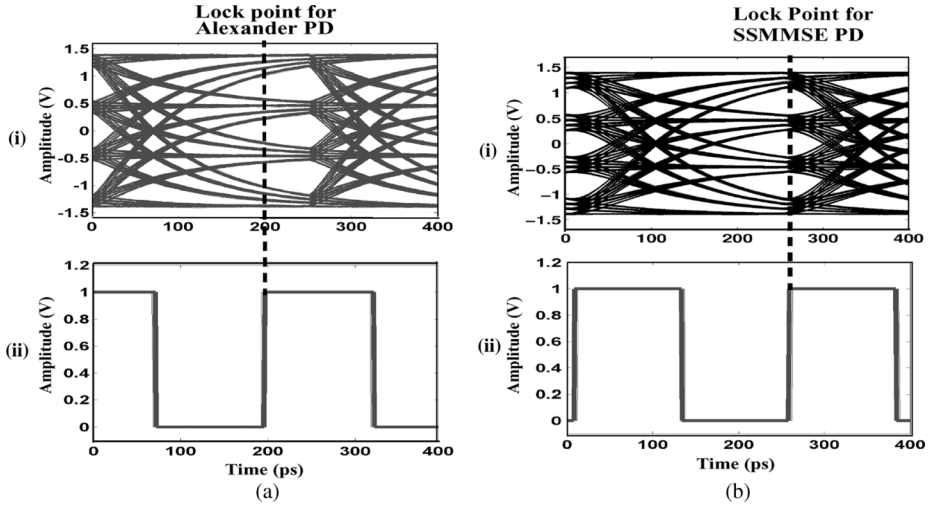
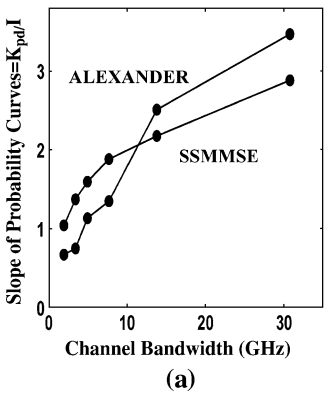


Fig. 14. Eye diagrams for 10-MHz CDRs. (a) Alexander PD-based CDR. (i) 4-PAM input to CDR with 13.8-GHz bandwidth channel, 4-GHz receiver front-end, and $\mathrm{SNR} = 43$ dB. (ii) Alexander PD-based CDR clock. (b) SSMMSE PD-based CDR. (i) 4-PAM input to CDR with 13.8-GHz bandwidth channel, 4-GHz receiver front-end, $\mathrm{SNR} = 43$ dB, and 10-GHz bandwidth passive slope detector. (ii) SSMMSE PD-based CDR clock.



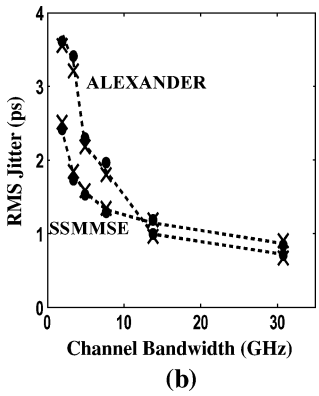
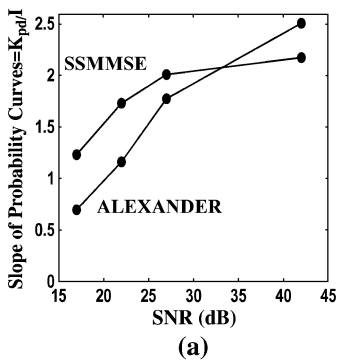


Fig. 15. Effect of channel bandwidth on the slope of probability curves and rms jitter of Alexander and SSMMSE PD-based CDR. For all CDRs, the $\mathrm{loop\ bandwidth} = 10$ MHz, $R = 0.5$ kΩ, $C = 5$ nF, $\mathrm{VCO\ gain} = 200$ MHz/V, $K_{\mathrm{pd_{bb}}} = 100\ \mu$A/rad. A coaxial cable channel model was used in all simulations. The SNR, 4-PAM data rate and receiver front-end bandwidth were set to 43 dB, 4 Gsymbol/s and 4 GHz, respectively. (a) Slope of probability curves versus channel bandwidth. (b) RMS jitter versus channel bandwidth ($\mathrm{dashed\ line} = \mathrm{linear\ jitter\ model}$ (8); $\mathrm{cross} = \mathrm{Markov\ jitter\ model}$; $\mathrm{dots} = \mathrm{simulation}$).



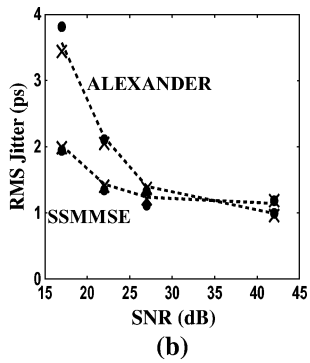


Fig. 16. Effect of SNR on the slope of probability curves and rms jitter of Alexander and SSMMSE PD-based CDR. For all CDRs, the $\mathrm{loop\ bandwidth} = 10$ MHz, $R = 0.5$ kΩ, $C = 5$ nF, $\mathrm{VCO\ gain} = 200$ MHz/V, $K_{\mathrm{pd_{bb}}} = 100\ \mu$A/rad. A coaxial cable channel model was used in all simulations. The channel bandwidth, 4-PAM data rate and receiver front-end bandwidth were set to 13.8 GHz, 4 Gsymbol/s and 4 GHz, respectively. (a) Slope of probability curves versus channel bandwidth. (b) rms jitter versus channel bandwidth ($\mathrm{dashed\ line} = \mathrm{linear\ jitter\ model}$(8); $\mathrm{cross} = \mathrm{Markov\ jitter\ model}$; $\mathrm{dots} = \mathrm{simulation}$).

B. Effect of SNR

As the noise power at the input to the CDR is increased, the signal-to-noise ratio (SNR) degrades and this lowers the slope of the probability curves and rms jitter of Alexander and SSMMSE PD-based CDR. Fig. 16 plots the slope of the probability curves and rms jitter of Alexander and SSMMSE PD-based CDR as a function of SNR. All Table I parameters for the 4-PAM system depicted in Fig. 1 were kept intact except the SNR. Both simulations and calculations predict that at large SNRs, Alexander performs better than SSMMSE. However, at lower SNRs, SSMMSE is superior to Alexander PD-based CDR.

C. Effect of VCO Jitter

To simulate the effect of VCO jitter and verfiy the loop bandwidth, sinusoidal noise was introduced at the input to the VCO and the phase transfer functions from the VCO input to the output of the VCO were plotted along with analytical transfer functions in Fig. 17. Note that the peak-to-peak VCO input phase has to be kept small to keep the CDR within the linear region of operation [9]. In these simulations, the peak-to-peak VCO input jitter was set to 10 ps.

D. Effect of Transmitter Jitter

Sinusoidal jitter with varying amplitude was introduced at frequencies from 50 kHz to 100 MHz at the transmitter. At each jitter frequency, the jitter amplitude was gradually increased until bit errors occurred. Fig. 18 plots the jitter tolerance for the two CDRs at two different SNRs. At large SNRs (i.e., $\mathrm{SNR} = 43$ dB) Alexander is more jitter tolerant than SSMMSE CDR. However, at low SNRs (i.e., $\mathrm{SNR} = 28$ dB) Alexander PD fails the jitter tolerance test even with no transmitter jitter. At low SNRs, the SSMMSE method has the potential to tolerate more jitter compared to the Alexander PD-based CDR for the given channel and noise conditions. This effect can be explained from

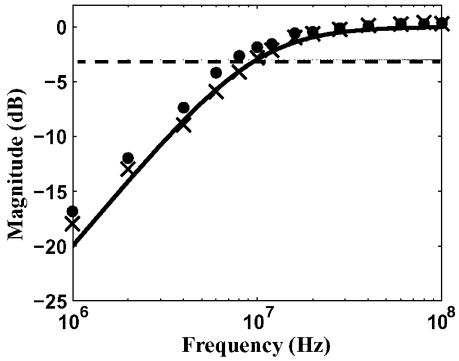


Fig. 17. CDR transfer characteristics with 13.8-GHz coaxial cable channel, SNR = 43 dB, 4 Gsymbol/s 4-PAM data and 4-GHz receiver front-end (solid line, linearized analysis; dots, simulation results for SSMMSE PD-based CDR; cross, simulation results for Alexander PD-based CDR. For all CDRs, the loop bandwidth = 10 MHz, $R = 0.5$ kΩ, $C = 5$ nF, VCO gain = 200 MHz/V, $K_{\mathrm{pd_{bb}}} = 100\ \mu$A/rad.

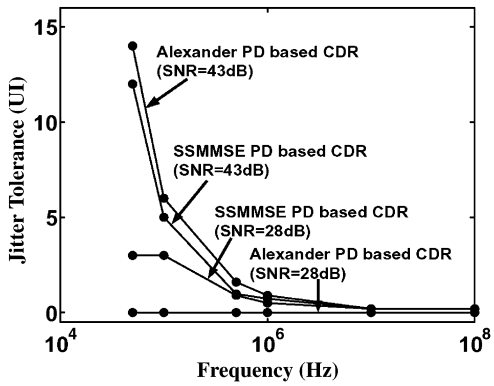


Fig. 18. CDR jitter tolerance simulation results with 13.8-GHz bandwidth coaxial cable channel, 4 Gsymbol/s and 4-GHz receiver front-end. For all CDRs, the loop bandwidth = 10 MHz, $R = 0.5$ kΩ, $C = 5$ nF, VCO gain = 200 MHz/V, $K_{\mathrm{pd_{bb}}} = 100\ \mu$A/rad.

the input eye diagrams shown in Fig. 19 for two different SNRs. At low SNRs, the data transitions are more effected by noise, than the peak in the eye opening. Since the SSMMSE technique tracks the maximum data eye opening instead of the data transitions, it has better jitter tolerance compared to the Alexander PD-based CDR at low SNRs.

VI. Conclusion

Analysis and design of multilevel bang–bang CDRs were presented. A sampling-phase-dependent PDF is derived and utilized to model two different bang–bang CDRs: Alexander and SSMMSE. The CDRs are modeled by calculating the slope of the P_{early} and P_{late} versus sampling phase curves in the vicinity of the lock point. The loop bandwidth of the CDR is directly proportional to the slope of the P_{early} and P_{late} curves in the vicinity of the lock point. A CDR with a lower slope will require a larger charge pump current and a larger bang–bang phase step to meet a target loop bandwidth. Therefore, the slope of the P_{early} and P_{late} curves is an important performance metric of any bang–bang CDR. A steeper slope implies lower rms jitter and higher jitter tolerance. Since the CDR input statistics effect the PD gain the choice of the best PD will in general depend on the channel ISI and noise. The analysis presented here is particularly well suited to multilevel systems where ISI and noise become important due to the degradation in voltage margin as a result of the increased number of levels.

Analysis showed that for the coaxial cable channel and Gaussian noise conditions assumed, the SSMMSE PD performed better compared to the Alexander PD at large ISI and low SNRs since the SSMMSE PD maintained a higher slope of the P_{early} and P_{late} curves. At large ISI and low SNRs, the noise in the data transitions is effectively worse than in the maximum data eye opening; thus causing the SSMMSE PD to perform better than the Alexander PD-based CDR under these conditions.

Comparison of the hardware requirements of the two CDRs is given in Table IV. The SSMMSE method presented in this work is hardware efficient compared to an Alexander PD-based CDR. A particularly important feature of the SSMMSE method is that it requires half the number of clock sampling phases as that of the Alexander PD. For example, to retime the data with a quarter rate clock, an Alexander PD would require eight clock phases separated in phase by 45° but the SSMMSE method requires only four clock phases separated in phase by 90°. Thus, the SSMMSE method would require a simpler and lower power VCO.

Appendix
Correlation-Coefficient Function for SSMMSE PD

The purpose of this section is to prove that the correlation-coefficient function for a random signal (Y_1) and its slope, $(S = dY_1/dt)$ is equal to zero. From (33)

$$\rho_{Y_1S} = \frac{E[Y_1S] - E[Y_1]E[S]}{\sigma_S\sigma_{Y_1}}. \tag{38}$$

For uncorrelated random data, $E[Y_1] = 0$. Also $E[Y_1S] = R_{Y_1S}(0)$, where $R_{Y_1S}(0)$ denotes the cross correlation between Y_1 and S for a lag (or delay) of zero. Therefore

$$\rho_{Y_1S} = \frac{E[Y_1S]}{\sigma_S\sigma_{Y_1}} = \frac{R_{Y_1S}(0)}{\sigma_S\sigma_{Y_1}}. \tag{39}$$

If Y_1 is a wide-sense stationary process, then its cross-correlation with its slope S can be expressed as [13]

$$R_{Y_1S}(t_d) = -\frac{dR_{Y_1}(t_d)}{dt_d} \tag{40}$$

where t_d is the delay (or lag) between the signal Y_1 and its slope, S and $R_{Y_1S}(t_d)$ is the auto-correlation function for the signal Y_1 for a delay of t_d. Substituting (40) in (39)

$$\rho_{Y_1S} = \frac{R_{Y_1S}(0)}{\sigma_S\sigma_{Y_1}} = \frac{-1}{\sigma_S\sigma_{Y_1}}\frac{dR_{Y_1}(t_d)}{dt_d}\Big|_{t_d=0} \tag{41}$$

$R_{Y_1}(t_d)$ is expressed as [13]

$$R_{Y_1}(t_d) = \int_{-\infty}^{\infty} [\mathrm{PSD}_{Y_1}(f)]\, e^{j2\pi f t_d} df \tag{42}$$

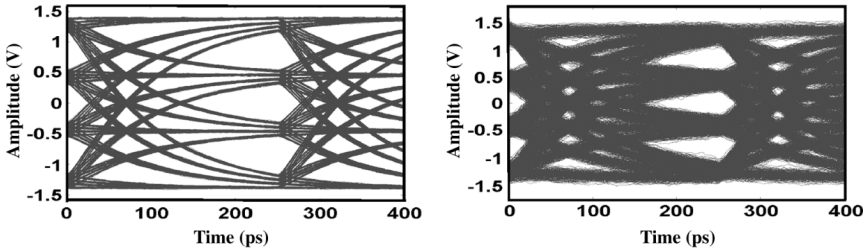


Fig. 19. Eye diagram of 4 Gsymbol/s, 4-PAM data with 13.8-GHz channel. (a) $\mathrm{SNR} = 43$ dB. (b) $\mathrm{SNR} = 28$ dB.

TABLE IV
COMPARISON OF THE HARDWARE REQUIREMENTS OF ALEXANDER PD AND SSMMSE PD

Phase Detector	High-speed clocked comparators	Clock phases (per symbol period)	PD Logic	Other hardware
SSMMSE	3	1	4 ANDs; 2 ORs.	Slope detector.
Alexander	6	2	6 XORs; 6 ANDs; 2 ORs	Transition detector.

where $\mathrm{PSD}_{Y_1}(f)$ denotes the power-spectral density of Y_1. Substituting (42) in (41) and simplifying

$$\begin{aligned}\rho_{Y_1S} &= -\frac{1}{\sigma_S\sigma_{Y_1}}\int_{-\infty}^{\infty} j2\pi f\,[\mathrm{PSD}_{Y_1}(f)]df \\ &= \frac{\int_{-\infty}^{0} j2\pi f\,[\mathrm{PSD}_{Y_1}(f)]df + \int_{0}^{\infty} j2\pi f\,[\mathrm{PSD}_{Y_1}(f)]df}{-\sigma_S\sigma_{Y_1}} \\ &= \frac{-\int_{0}^{\infty} j2\pi f\,[\mathrm{PSD}_{Y_1}(f)]df + \int_{0}^{\infty} j2\pi f\,[\mathrm{PSD}_{Y_1}(f)]df}{-\sigma_S\sigma_{Y_1}} \\ &= 0. \end{aligned} \tag{43}$$

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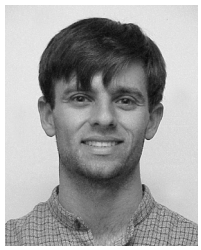

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