A Passive Filter Aided Timing Recovery Scheme

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***Abstract*— This paper presents a passive filter for the front end of a high speed serial link receiver to aid timing recovery. The filter provides simultaneous lowpass and highpass transfer characteristics to generate the data and its slope respectively. Slope detection is demonstrated at 10-Gb/s. As a proof of concept, the filter was used to extract a 2-GHz clock from a 2-Gb/s 2^{31}-1 random data sequence based on a modified minimum mean squared error (MMSE) criterion. The circuit is fabricated in a 0.18 μm CMOS process and consumes 21.6 mW from a 1.8V supply.**

***Index Terms*— Baud-rate timing recovery, MMSE, CMOS, passive filter.**

I. Introduction

This paper introduces a high speed passive filter that aids an external timing recovery loop by generating the slope of an incoming random data waveform.

Typically, timing recovery (TR) is achieved by tracking the edges of the incoming random bit stream [1]. This approach requires an extra clock phase for sampling the edges of the input data. TR without edge sampling (also called baud-rate TR) requires only data samples and thus is more hardware-efficient than edge-sampled TR [2]. Baud-rate techniques reported in the literature either rely on specific 4-bit patterns [2] or uncorrelated random data [3],[4]. Recently, an active filter aided baud-rate TR scheme has ben reported that is based on a modified minimum mean squared error (MMSE) criterion [5]. Unlike other baud-rate schemes, this scheme is not constrained by the properties of the input random data. However, continuous-time slope detection is the major challenge in implementing this scheme. Although the active filter reported in [5] provides the slope information of the input data and performs linear equalization as well, it suffers from low speed and increased power consumption. This work demonstrates the use of a low-power passive filter that provides slope information at a higher speed for baud-rate TR.

II. Modified MMSE TR

Although this scheme has been described in detail in [5], it is briefly described here for completeness. MMSE TR is based on the following stochastic gradient update rule:

$$\tau_{k+1} = \tau_k + 2\mu e_k \left(\frac{\delta y(kT+\tau_k)}{\delta \tau_k} \right) \tag{1}$$

Here $y(t)$ represents the received waveform, T the symbol period, τ_k the sampling phase for the kth received bit R_k, $e_k = R_k - y(kT+\tau_k)$ and μ is a parameter that is chosen to tradeoff acquisition time with jitter and determines how quickly τ_k is adjusted. Practical high speed implementations of the LMS algorithm often use only 1-bit representations of the sign of the error and the slope [6]. Applying this idea to MMSE TR results in the following Sign-Sign (SSMMSE) rule [7]:

$$\tau_{k+1} = \tau_k + 2\mu \text{sgn}(e_k) \text{sgn} \left(\frac{\delta y(kT+\tau_k)}{\delta \tau_k} \right) \tag{2}$$

For NRZ data, the TR equation can be simplified to exclude the error signal e_k [5]:

$$\tau_{k+1} = \tau_k + 2\mu \text{sgn} \left(y(kT+\tau_k) \frac{\delta y(kT+\tau_k)}{\delta \tau_k} \right) \tag{3}$$

The main point here is that this scheme requires a continuous time slope detector. Although a two-tap slope detector has been reported in [8], this leads to large jitter in the recovered clock [9].

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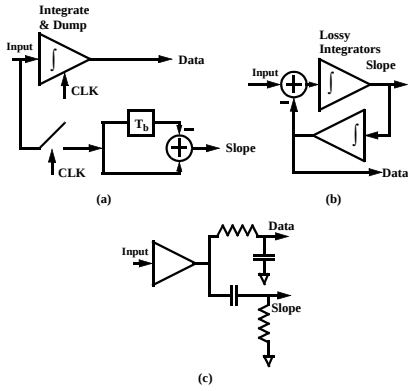


Fig. 1. Slope detection techniques. (a) Integrate and Dump [7]. (b) Active Filter [5]. (c) Passive filter comprised of RC-CR section [This work].

III. High Speed Slope Detection

As shown in Fig. 1 (a) slope detection can be simplified by an integrate and dump circuit, which has the following input-output relationship [7]:

$$y(kT+\tau) = \int_{(k-1)T+\tau}^{kT+\tau} u(t)\, dt \tag{4}$$

where $u(t)$ is the input and $y(t)$ is the output. Taking the derivative on both sides,

$$\left(\frac{\delta y(kT+\tau_k)}{\delta \tau_k} \right) = u(kT+\tau) - u((k-1)T+\tau) \tag{5}$$

This approach is simple and provides a low power solution to slope detection. However, the low-pass characteristics of integrating front-ends make them prone to intersymbol interference (ISI) thus limiting the maximum allowable data rate

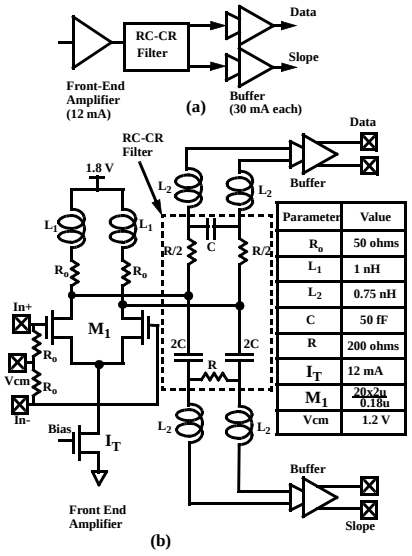


Fig. 2. Passive Filter. (a) Block diagram. (b) Schematic.

for this scheme. An active filter can be utilized to provide data and slope information simultaneously as shown in Fig. 1(b). The active filter can be designed to include linear equalization as well [5]. Fabricated in a 0.18 μm CMOS process, the active filter in [5] consumed 39.6mW from a 1.8V power supply and operated upto 2.7-Gb/s. A lower power and higher speed solution is a passive filter comprised of an RC-CR section, as shown in Fig. 1(c). Here the data is passed simultaneously through a low-pass and a high-pass first order filter section. This aligns the slope signal with the data signal over a broad bandwidth.

IV. Passive Filter

Fig. 2 shows the complete schematic of the passive filter. It consists of a front-end amplifier, an RC-CR section and two sets of output buffers. The lowpass RC section is called the "data path" and the high pass CR section is the "slope path". To ensure a 90 degree relative phase shift between the data and slope paths, identical elements were used in both paths. The cut-off frequency of the passive filter is a critical parameter in the design. Decreasing the RC time constant ensures wide bandwidth in the data path, but reduces the gain in the slope path proportionately. To ensure that the bandwidth was not limited by the passive filter, the RC time constant was chosen to be 10ps. The input impedance of the filter per side as a function of frequency is given as:

$$Z_{in} = \frac{R}{4} + \frac{1}{4j\omega C} \tag{6}$$

Since R was set to 200 ohms, the input impedance of the filter was 50 ohms only at high frequecncies. Therefore, in order to provide a broadband input match to the external 50 ohm characteristic impedance a front-end amplifier was needed as shown in Fig. 2. Inductors L_1 and L_2 were used to improve the amplifier's bandwidth. Note that the presence of these inductors do not effect the slope detection action of the passive filter. This can be derived as follows:

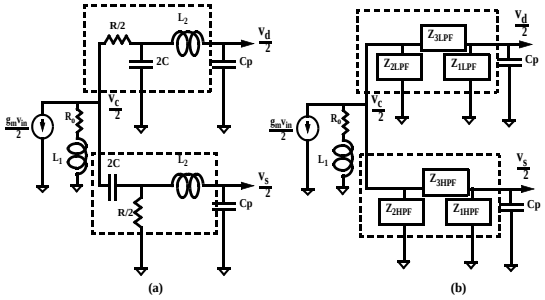


Fig. 3. Small signal model of passive filter. (a) Small signal half-circuit. (b) Small signal half-circuit with RCL-CRL sections replaced by equivalent Δ sections.

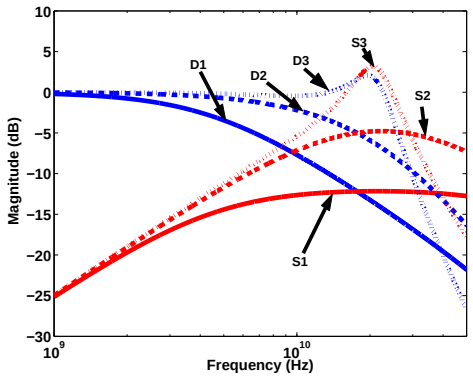


Fig. 4. Data and slope path frequency responses. D1 and S1 respectively denote the data and slope path transfer functions without inductors L_1, L_2; D2 and S2 respectively denote the data and slope path transfer functions with inductor L_1 only and D3 and S3 respectively denote the data and slope path transfer functions without both inductors L_1, L_2. For these simulations, $g_m = 20mA/V, C_p = 110fF$ and all other parameters were taken from the table in Fig. 2.

Fig. 3 (a) shows the small signal circuit of the passive filter. C_p denotes the parasitic capacitance at the input to the buffer. To simplify the analysis, the RCL-CRL sections are replaced by their equivalent Δ network by using a Y-Δ transformation (Fig. 3 (b)). The impedances in the Δ network can be expressed as,

$$Z_{1LPF}(j\omega) = Z_{3HPF}(j\omega) = j\omega(L_2 - \frac{1}{2\omega^2 C}) + \frac{L_2}{RC} \tag{7}$$

$$Z_{2LPF}(j\omega) = Z_{2HPF}(j\omega) = \frac{j\omega\frac{R}{2}(L_2 - \frac{1}{2\omega^2 C}) + \frac{L_2}{2C}}{j\omega L_2} \tag{8}$$

$$Z_{3LPF}(j\omega) = Z_{1HPF}(j\omega) = -\omega^2 RC(L_2 - \frac{1}{2\omega^2 C}) + j\omega L_2 \tag{9}$$

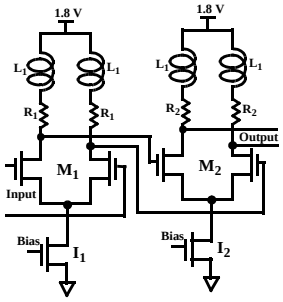
The gain in the data path can be expressed as:

$$\frac{v_d}{v_{in}}(j\omega) = A_1(j\omega)K_L(j\omega) = A_1(j\omega)\frac{Z_{1LPF}(j\omega)}{Z_T(j\omega)} \tag{10}$$

where $Z_T(j\omega) = Z_{1LPF} + Z_{3LPF} + j\omega C_p Z_{1LPF} Z_{3LPF}$ and $A_1(j\omega)$ is the gain from $v_c/2$ to $v_{in}/2$[1]. The gain in the slope path can be expressed as:

$$\frac{v_s}{v_{in}}(s) = A_1(j\omega)K_H(j\omega) = A_1(j\omega)\frac{Z_{3LPF}(j\omega)}{Z_T(j\omega)} \tag{11}$$

[1] $A_1(j\omega) = \frac{-g_m}{Y_o + 2Y_{2LPF} + (1-K_L(j\omega))Y_{3LPF} + (1-K_H(j\omega))Y_{1LPF}}$



Parameter	Value
R_1	100 ohms
R_2	50 ohms
L_1	1 nH
I_1	10 mA
I_2	20 mA
M_1	20x2u / 0.18u
M_2	40x2u / 0.18u

Fig. 5. Schematic of two-stage buffer.

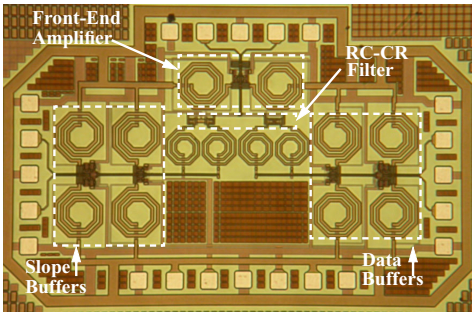


Fig. 6. Die Photo of Passive Filter

Thus the ratio of the gains in the data and slope paths can be expressed as:

$$\frac{v_d}{v_s}(s) = \frac{Z_{1LPF}}{Z_{3LPF}} = \frac{1}{j\omega RC} \tag{12}$$

Eq. (12) shows that inductors L_1 and L_2 do not hamper the slope detection action of the passive filter. Fig. 4 plots the transfer functions in the data and slope paths with and without inductors L_1 and L_2. The plots reveal that inductors L_1 and L_2 improve the bandwidth and gain in both paths.

Output buffers were provided in both the data and slope paths, each comprising of two inductively peaked differential pairs (Fig. 5). The total current consumption was 72mA from a 1.8V power supply. Of this total, 12mA was consumed in the front-end amplifier and 30mA in each of the output buffers. Excluding the output buffers, the power consumption was 21.6 mW.

V. Measurement Results

The passive filter was fabricated in a 0.18-μm CMOS technology and occupied an area of 1.1 mm^2. The die photo is shown in Fig. 6. A network analyzer was used to measure the frequency response (Fig. 7) of the filter on wafer. The measured -3dB bandwidth in the data path was 6 GHz. In the slope path, the magnitude of S_{21} increased at a rate of 20dB/dec. The relative phase shift between the data and slope paths is plotted in Fig. 8(a). The phase shift is near 90 degrees over a broad bandwidth. The input impedance of the filter is shown in Fig. 8(b). A Centellax PRBS board was connected to the passive filter to test its functionality. Eye diagrams of data and slope outputs captured by an Agilent 86100B scope for a 10-Gb/s 2^{31}-1 PRBS sequence are shown in Fig. 9. Note that the slope output exhibits peaks aligned with transitions

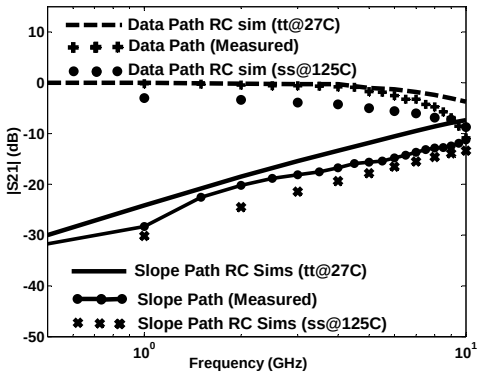
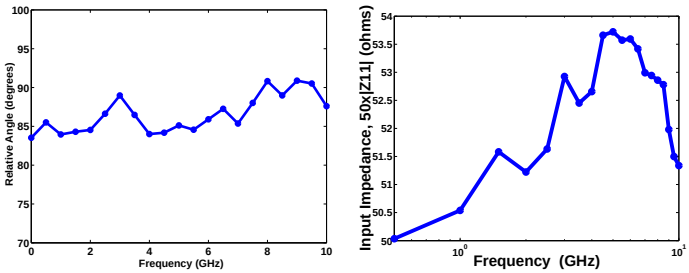


Fig. 7. Measured and simulated S21 in the data and slope paths.



(a) (b)

Fig. 8. Network analyzer measurements. (a) Relative angle between the data and slope paths.(b) Input impedance of the passive filter.

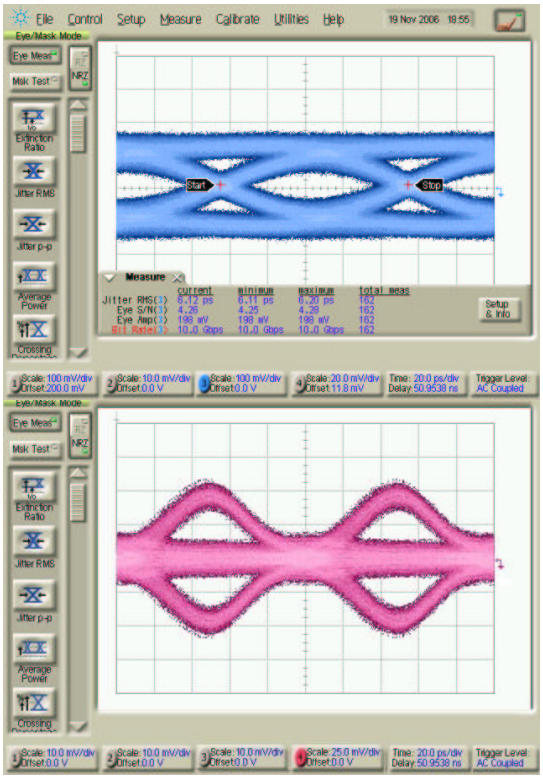


Fig. 9. Data (top eye) and slope (bottom eye) outputs of passive filter at 10-Gb/s (Vertical scale (top eye)=100mV/div; Vertical scale (bottom eye)=25mV/div ; Horizontal scale=20ps/div).

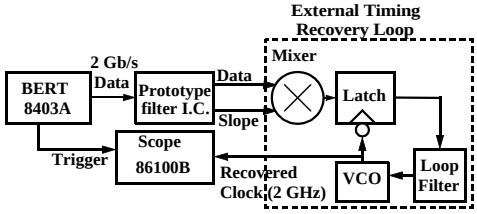


Fig. 10. Test set up for external TR loop using the passive filter.

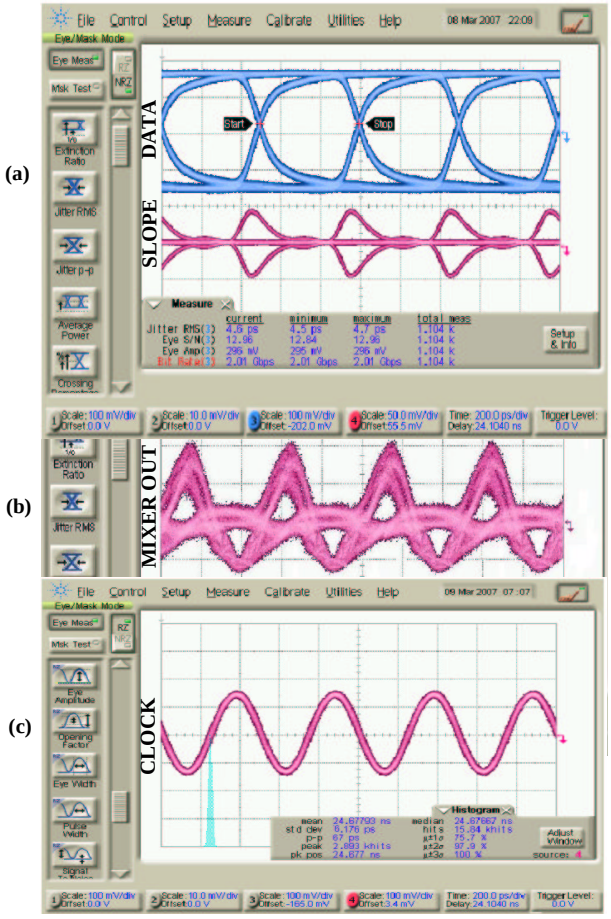


Fig. 11. Waveforms at different points of the TR loop. (a) Data (top eye) and slope (bottom eye) outputs of passive filter at 2-Gb/s.(Vertical scale (top eye)=100mV/div; Vertical scale (bottom eye)=50mV/div ; Horizontal scale=200ps/div) (b) Mixer output corresponding to a 2-Gb/s random data sequence (Vertical scale= 50mV/div; Horizontal scale=200ps/div). (c) Recovered 2-GHz clock (Vertical scale= 100mV/div; Horizontal scale=200ps/div).

in the data waveform. At high speeds, capturing the data and slope signal that are precisely aligned is challenging due to the mismatches in cables. To offset this issue, the data signal was captured first and then the same cable was connected to the slope path to capture the slope. The scope time delay settings were kept fixed during this measurement as shown in the time delay slots of the eye diagrams in Fig. 9.

The passive filter was combined with external components to demonstrate the proposed TR scheme as shown in (Fig. 10). The mixer, latch, VCO and loop filter were implemented on a separate board using commercial components. The loop was tested with a 2-Gb/s 2^{31}-1 PRBS data pattern generated from a BERT. The data rate for this test was limited by the external components. The mixer takes the product of the slope and data signals, as required by Eq. (3), and the latch performs the sgn operation. Fig. 11 shows the waveforms at different points of the test setup. As expected, a baud-rate timing tone is visible at the output of the mixer. The resulting RMS clock jitter was 6.1 ps. Table I summarizes the performance of the TR scheme and compares it to other published timing recovery schemes.

TABLE I

PERFORMANCE SUMMARY & COMPARISON TABLE

Reference	Data Rate	Clock Freq.	Conditions	RMS Jitter
This work (Baud-rate)	2 Gb/s	2 GHz	2^{31}-1 PRBS;	6.1 ps
[5] (Baud-rate)	2 Gb/s	2 GHz	2^{31}-1 PRBS;	6.5 ps
[2] (Baud-rate)	5 Gb/s	1 GHz	Random data;	4.8 ps
[10] (Edge-sampled)	2.5 Gb/s	2.5 GHz	2^{23}-1 PRBS;	17.4 ps

VI. CONCLUSION

This paper presented a passive filter that is used to generate timing information from a random data waveform. This filter provides simultaneous lowpass and highpass transfer characteristics over a broad bandwitdh. The highpass transfer characteristic is utilized to provide the slope information upto 10-Gb/s. The data and slope signals can be used to recover a clock based on the modified MMSE criterion. To demonstrate the timing recovery concept, the prototype passive filter was used with external components to recover a 2-GHz clock from a 2-Gb/s 2^{31}-1 random data sequence.

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