A 20-Gb/s Coaxial Cable Receiver Analog Front-End in 90-nm CMOS Technology

Peter Park and Anthony Chan Carusone
Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto
Toronto, ON M5S 3G4 Canada

***Abstract*—A binary receiver analog front-end (AFE) targeting 20 Gb/s for use with coaxial cable channels is presented. To accommodate links of varying lengths, the AFE includes an analog peaking equalizer followed by a post-amplifier. The input preamplifier is important for achieving the required input sensitivity. A DC bias current is introduced through the feedback resistor in a conventional shunt-shunt feedback nMOS transimpedance amplifier (TIA) to level-shift the output, obviating a following level-shifting stage. The fabricated AFE occupies 0.89 mm^2 in a 90-nm CMOS process and dissipates 138 mW from a 1.3-V supply. The AFE amplifies and opens the eye pattern of a 20-Gb/s data stream transmitted over coaxial cable with 7.5-dB loss at 10 GHz.**

I. Introduction

Multi-Gb/s transceivers including equalization is an area of ongoing research. A basic transceiver link is shown in Fig. 1, where the channel is typically a backplane trace or coaxial cable. Due to frequency-dependent channel impairments such as skin-effect and dielectric loss, transmitter and/or receiver equalization becomes necessary. This work addresses the design of the analog front-end (AFE) of a binary 20-Gb/s coaxial cable receiver in a 90-nm CMOS technology. As part of this work, a broadband preamplifier topology was used that (to the authors' knowledge) had not previously been implemented in CMOS. Analog peaking equalization was also implemented. Adaptation and clock recovery were beyond the scope of this work.

The following sections describe the circuit design and present measurement results of the AFE.

II. Architecture

A block diagram of the receiver AFE is shown in Fig. 2. The single-ended input signal is amplified by the broadband preamplifier. The preamplifier output is single-ended, so a single-ended to differential (S2D) block is used. The signal is then applied to an analog equalizer, and buffered by the post-amplifier and output driver to provide appropriate swing and termination to the 50-Ω testing environment. The output driver is required solely for testing.

III. Circuit Design

This section details the circuit design of the 20-Gb/s receiver AFE blocks.

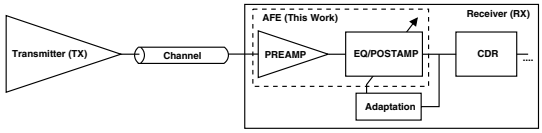


Fig. 1. Basic transceiver link.

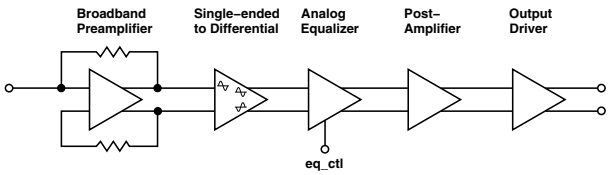


Fig. 2. AFE block diagram.

A. Broadband Preamplifier

The first stage of the receiver AFE is the broadband preamplifier (Fig. 2). To maximize sensitivity, it is generally desirable for the first stage to provide high gain and low noise. While widely used in conjunction with photodiodes, the shunt-feedback transimpedance amplifier (TIA) has also been used as a low-noise broadband preamplifier [1]. MOS differential pairs preceded by on-chip termination resistors have also been used for this purpose, but it has been shown that the shunt-feedback topology is preferred in terms of noise, power and bandwidth [2]. This section compares two possible TIA topologies for use as a broadband preamplifier in the receiver front-end. It is assumed throughout that the preamplifier is followed by an nMOS-input differential pair, so the preamplifier output common-mode (CM) level must be compatible with this.

The first topology is the nMOS TIA with common-source (CS) in Fig. 3(a), which uses a CS amplifier with active load for the main voltage-gain stage, followed by another CS stage to provide more gain and level-shifting. This topology has recently been used as a broadband preamplifier [1], [2]. One possible issue with this topology is the output swing being limited on the low side due to M_1 being diode-connected at DC. The second topology is the nMOS TIA with active bias in Fig. 3(b), which uses a current source (M_3) to raise the output CM, obviating the second level-shifting CS stage. Note that a similar topology is common in discrete realizations [3, pp. 395-406], where passive biasing with resistors is used to raise the output CM. However, if these resistors are not

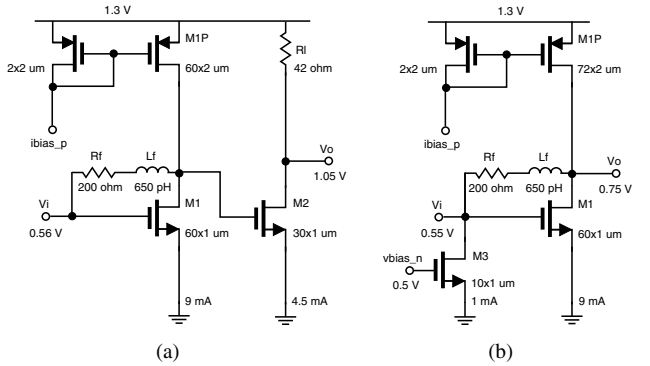


Fig. 3. Broadband preamplifiers used for simulation comparison: (a) nMOS TIA with CS, (b) nMOS TIA with active bias.

sufficiently large, the input match (and therefore the gain of the TIA when driven with a non-zero source impedance) is degraded [3]. Therefore a topology using active devices for biasing was considered. One disadvantage is the noise contributed by the current source M_3 appearing directly at the input, which could be mitigated as follows. The noise due to M_3 referred to an input voltage source V_s in series with a source resistance R_s is approximately

$$v_{n,s}^2(f) = [4kT\gamma g_{m3} + \frac{K_N}{C_{ox}W_3L_3f}g_{m3}^2]R_s^2 \qquad (1)$$

indicating that to reduce the noise contribution of M_3, g_{m3} should be minimized while the product W_3L_3 should be maximized. To the authors' knowledge, the nMOS TIA with active bias topology has not previously been implemented in CMOS, either as a broadband preamplifier or photodiode TIA.

The design procedure given in [2] for the nMOS TIA with CS topology was followed, resulting in the device sizes shown in Fig. 3(a). The value of R_f was chosen to set the TIA input impedance to the targeted 75-Ω cable impedance. Inductor L_f extends bandwidth and reduces the input-referred noise of R_f [4]. The CS transistor M_2 and load resistor R_l were sized to make the CS stage gain near 0 dB so that the gains of both TIAs under consideration would be the same.

The design of the nMOS TIA with active bias in Fig. 3(b) is very similar to the nMOS TIA with CS, apart from the addition of M_3 and the removal of the CS stage. In order to source the extra DC current flowing through R_f and M_3 while maintaining the same current density of M_1, W_{1P} was increased by 20%.

For both topologies, the simulated AC gain, $|S_{11}|$, NF and gain compression at 10 GHz are shown in Fig. 4. The simulations included 30 fF of capacitance at the input and output nodes. The AC response and input match were essentially the same for both topologies (A_{DC}/BW = 8.4 dB/13.4 GHz). However, the 10-GHz NF and P_{1dB} of the nMOS TIA with active bias were 0.5 dB lower (5.7 dB vs. 6.2 dB) and 50% higher (0.42 V_{pp} vs. 0.28 V_{pp}), respectively, indicating slightly lower noise and greater output swing. The NF increases at low frequency mainly due to the $1/f$-noise of the TIA transistors.

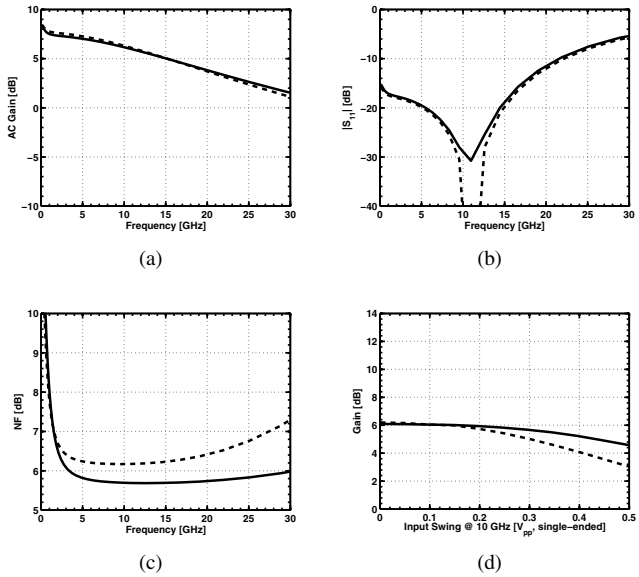


Fig. 4. Simulation comparison between nMOS TIA with active bias (solid) and nMOS TIA with CS (dashed): (a) AC gain, (b) $|S_{11}|$, (c) NF and (d) gain compression at 10 GHz.

Note that by increasing the value of R_l, the nMOS TIA with CS can have significantly larger gain than the nMOS TIA with active bias and would, therefore, tend to lower the NF. This makes the nMOS TIA with CS preferable in applications where a large voltage gain is desired, such as when the input signal is very small or when it is acceptable for the output to saturate (e.g. the output is a digital signal or is passed to a limiting amplifier). In this work, however, the output must be linearly processed by the remainder of the front-end up to the post-amplifier. The desired CS stage gain would have been approximately 0 dB if the nMOS TIA with CS had been used, and so the nMOS TIA with active bias was chosen for this application. The schematic of the implemented nMOS TIA with active bias is shown in Fig. 5. Approximately 1 mA of bias current drawn by M_3 flows through R_f at DC. By using M_3 instead of a resistor, the current source output resistance was increased ($\approx$ 1 kΩ versus 0.5 kΩ). Inductors L_p and L_g were added to improve matching and provide bandwidth extension [5]. Although the input is single-ended, a dummy stage was used to provide power supply rejection at the expense of higher power and noise.

B. Single-ended to Differential Stage (S2D)

As the coaxial cable output is single-ended and the broadband preamplifier does not provide any CM rejection, a separate S2D stage is used. Three cascaded differential pairs were used to ensure sufficient rejection of the large effective CM input, with the unused side of the first pair biased by the dummy preamplifier stage.

C. Analog Equalizer

Peaking equalizers have commonly been used to compensate notch-free, low-pass channels. The schematic of the

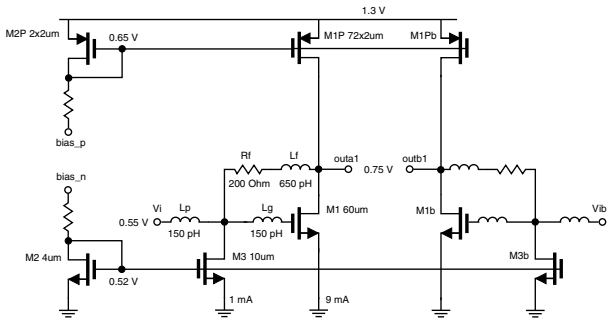


Fig. 5. Schematic of the broadband preamplifier.

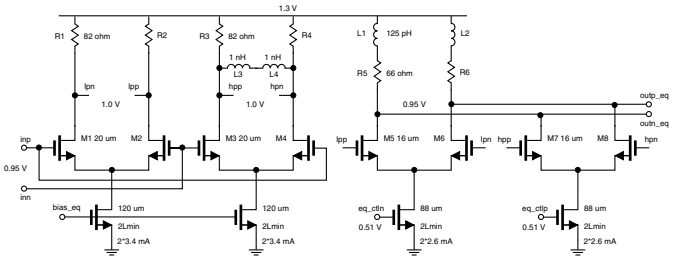


Fig. 6. Schematic of the equalizer.

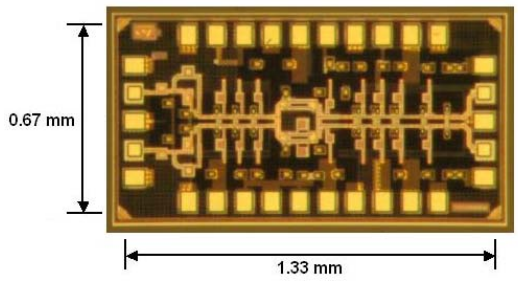
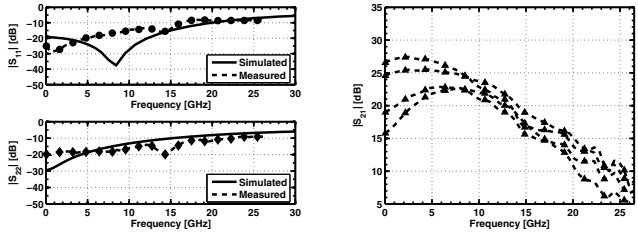


Fig. 7. AFE die photo.



(a) (b)

Fig. 8. Measured S parameters: (a) $|S_{11}|$ and $|S_{22}|$ and (b) $|S_{21}|$ for various equalizer settings.

equalizer is shown in Fig. 6, and is based on the 10-Gb/s BiCMOS cable equalizer in [6]. The low-pass and high-pass paths formed by transistors $M_{1,2}$ and $M_{3,4}$, respectively, are summed by M_{5-8} with the weighting set by eq_ctlp and eq_ctln. In [7], this topology was analyzed and used to achieve 40-Gb/s equalization in a 90-nm CMOS technology. The 1 nH inductors $L_{3,4}$ were implemented on-chip as stacked spirals, with self-resonance frequency (SRF) $>$ 50 GHz, well above the targeted peaking frequency. The equalizer has a simulated DC gain range of -8.6 to 0.3 dB, and maximum peaking of 8.6 dB.

D. Post-Amplifier and Output Driver

A post-amplifier follows the equalizer, and compensates for the low-frequency equalizer losses that increase with the amount of peaking applied. This block was implemented with three cascaded differential pairs. The 50-Ω output driver required for testing consisted of two cascaded differential pairs.

IV. Measurements

The die photo of the AFE is shown in Fig. 7, which occupies 1.33 mm x 0.67 mm = 0.89 mm^2 and dissipates 138 mW from a 1.3-V supply. All signals were applied and measured single-endedly by wafer probing. As the broadband preamplifier was integrated on-chip, measurements of the TIA alone were not possible.

A. S parameters

S parameters were measured using a HP 8510C 26.5-GHz VNA. Since the target cable channel is 75-Ω, all S parameters were converted from a 50-Ω to 75-Ω/50-Ω input/output port environment using the expressions in [8]. The single-ended $|S_{11}|$ and $|S_{22}|$ are shown in Fig. 8(a), with $|S_{11}|$ and $|S_{22}|$ below -10 dB up to 16 GHz and 20 GHz, respectively. The single-ended $|S_{21}|$ for various equalizer settings is shown in Fig. 8(b), displaying maximum peaking of 6.5 dB at 8 GHz. The measured gains were significantly larger than expected. Measurements of on-chip test structures indicated that the polysilicon resistors were $\approx$ 20% high, likely causing the excess gain.

B. Transients

An Agilent 86100C Infiniium DCA-J oscilloscope was used to capture single-ended eye diagrams. An input pattern for transient testing was generated by multiplexing four PRBS sequences (each of length $2^7 - 1$) to generate a 508-bit sequence. The AFE was tested with a 9-ft SMA cable (three 3-ft sections) having the frequency response shown in Fig. 9. For the 16.25-Gb/s input, the 9-ft SMA cable has 5.7 dB of loss at 8.125 GHz, with the corresponding eye diagram shown in Fig. 10(a). The equalized AFE output eye diagram is shown in Fig. 10(b). The input swing was 40 mV$_{pp}$, while the output swing was 225 mV$_{pp}$ per side with RMS jitter of 2.5 ps. The oscilloscope indicated timing margin of 0.58 UI for a BER of 10^{-12}. Similarly for the 20.4-Gb/s input, the cable has 7.5 dB of loss at 10.2 GHz, with the corresponding eye diagram shown in Fig. 11(a). The equalized AFE output eye diagram is shown in Fig. 11(b). The input swing was 40 mV$_{pp}$, while the output swing was 225 mV$_{pp}$ per side with RMS jitter of 2.7 ps. The oscilloscope indicated timing margin of 0.32 UI for a BER of 10^{-12}. This eye is less open than in the 16.25-Gb/s case due to reduced bandwidth caused by the larger-than-expected polysilicon resistors. There also appears

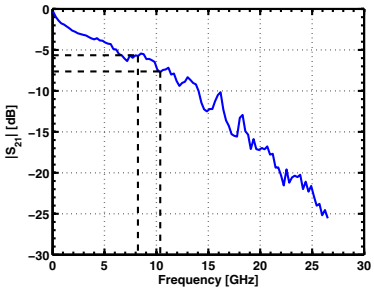
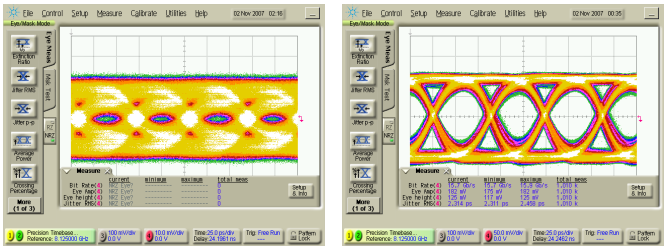
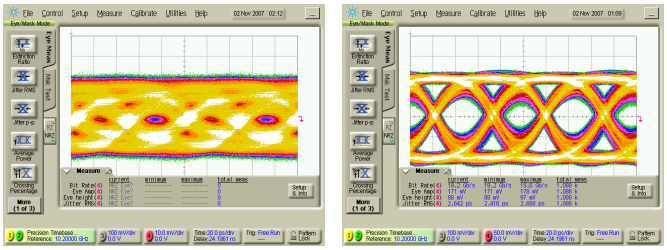


Fig. 9. Measured $|S_{21}|$ of a 9-ft SMA cable.



(a) (b)

Fig. 10. Single-ended eye diagrams for a 16.25-Gb/s 508-bit $(4 \times (2^7 - 1))$ input pattern: (a) through a 9-ft SMA cable (5.7-dB loss at 8.125 GHz); (b) equalized AFE output.



(a) (b)

Fig. 11. Single-ended eye diagrams for a 20.4-Gb/s 508-bit $(4 \times (2^7 - 1))$ input pattern: (a) through a 9-ft SMA cable (7.5-dB loss at 10.2 GHz); (b) equalized AFE output.

to be additional eye closure occurring every other bit. This is likely due to the test setup, as the corresponding input eye in Fig. 11(a) displays the same behaviour with only the input pattern generator and oscilloscope connected.

V. Conclusion

The design of a binary receiver AFE targeting 20 Gb/s in 90-nm CMOS has been investigated. The main functional blocks were the broadband preamplifier, peaking equalizer and post-amplifier. To the authors' knowledge, the nMOS TIA with active bias used as the broadband preamplifier had not previously been implemented in CMOS. The AFE provided a broadband match with $|S_{11}| <$ -10 dB up to 16 GHz, and maximum peaking of 6.5 dB at 8 GHz. A 9-ft SMA cable was equalized at 16.25 Gb/s (5.7 dB loss at 8.125 GHz) and 20.4 Gb/s (7.5 dB loss at 10.2 GHz). The design is 0.89 mm^2 and dissipates 138 mW from a 1.3-V supply. The receiver AFE is compared with other reported equalizers in Table I.

TABLE I
Comparison with other equalizers.

Reference	[7]	[9]	[10]	[11]	[12]	**This Work**
Bit Rate (Gb/s)	40	10	20	10	30	20.4
Loss[a] (dB)	10	19	9.5	20	14.5	7.5
Supply (V)	–	1.2	1.5	1.2	1	1.3
EQ Power (mW)	58	25	60	13.2	25	31
Total Power (mW)	115	–	60	133	25	138
Adaptive	YES	YES	YES	YES	NO	NO
Type[b]	SP+CD	CD	CD	CH	3-FIR	SP
Process	90-nm CMOS	0.13-um CMOS	0.13-um CMOS	0.11-um CMOS	90-nm CMOS	90-nm CMOS
Area (mm^2)	0.539	0.162 (CORE)	0.2 (CORE)	0.004 (EQ)	0.3	0.891

[a]Channel loss compensated at one-half the bit rate.
[b]SP, CD and CH refer to split-path, capacitive-degeneration and Cherry-Hooper topologies, respectively.

Acknowledgment

The authors would like to thank graduate student S. Shahramian for his help with testing, Gennum Corporation for financial support, and the Canadian Microelectronics Corporation (CMC) for technology and fabrication access.

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