A 20-Gb/s Coaxial Cable Receiver Analog Front-End in 90-nm CMOS Technology

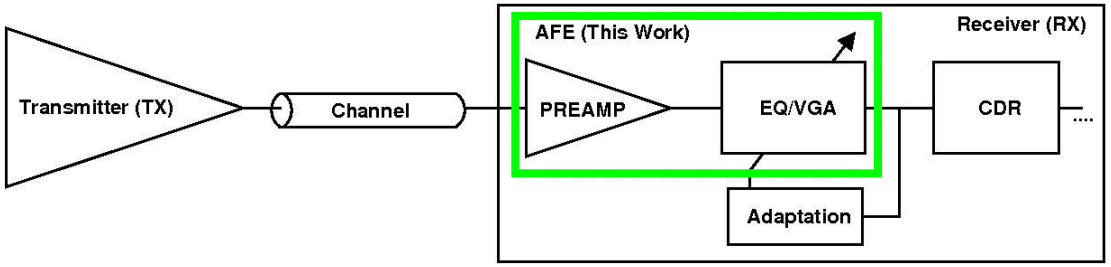
Peter Park[1] and Anthony Chan Carusone

University of Toronto, Canada

[1]now with Synopsys, Inc.

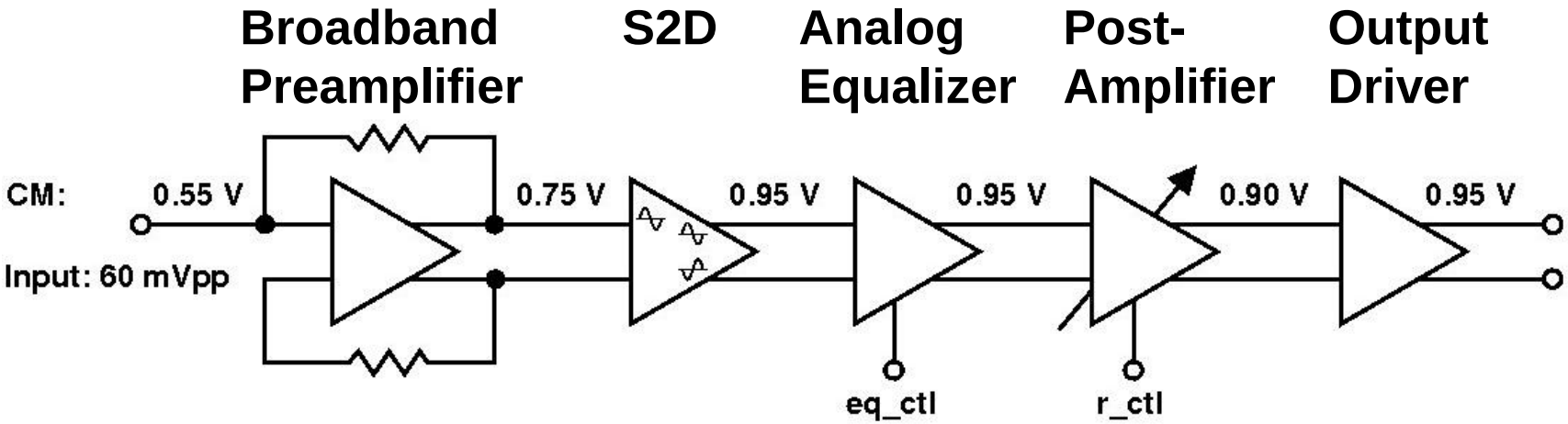
Receiver AFE Specifications

- 20-Gb/s operation
- 75-ohm input (cable impedance)
- 50-ohm output (testing)
- External gain and equalization control (non-adaptive)
- < 0.5 mV_{rms} input-referred noise
- 90-nm CMOS, 1.3-V supply



Basic transceiver link.

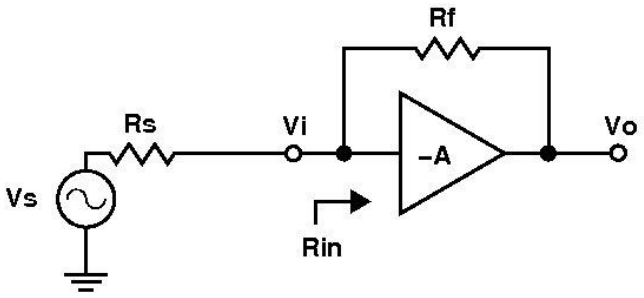
AFE Block Diagram



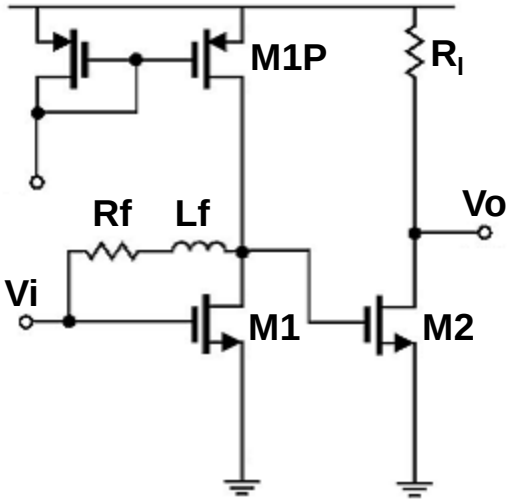
	Broadband Preamplifier	S2D	Analog Equalizer	Post-Amplifier	Output Driver
Gain (DIFF):	7.5 dB (SE)	8.3 dB	–8.6 – 0 dB	0 – 6.5 dB	0.4 dB
Bandwidth:	11.6 GHz	19 GHz	Variable	> 19.6 GHz	25.6 GHz
Swing/side:	140 mVpp	185 mVpp	70–185 mVpp	145–190 mVpp	150–200 mVpp
Power:	26 mW	42 mW	31 mW	23 mW	32 mW

Design - Broadband Preamplifier

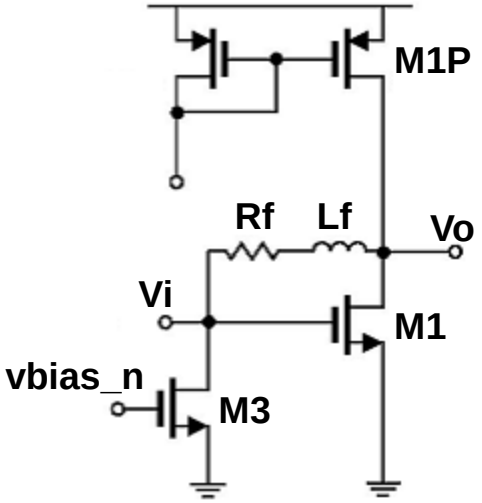
- **Shunt-feedback TIA stages have recently been used as low-noise broadband preamplifiers.**
- **TIA topologies were narrowed down to 1) nMOS TIA with common source (CS) and 2) nMOS TIA with active bias, and compared in simulation.**



Shunt-feedback TIA topology. Rin = Rf/(1+|A|).



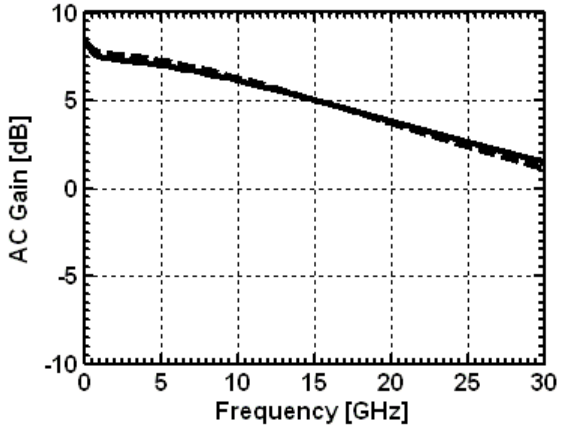
Topology: nMOS TIA with CS. The CS stage provides gain and level-shifting.

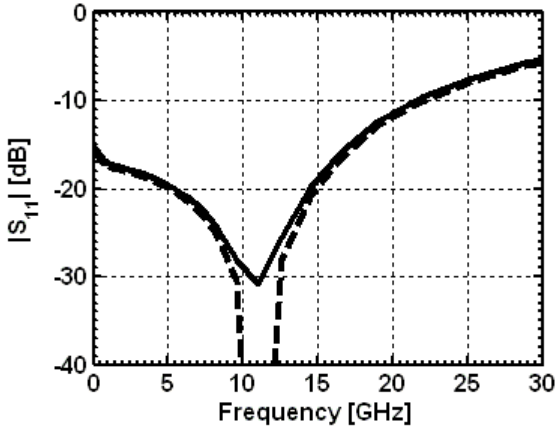


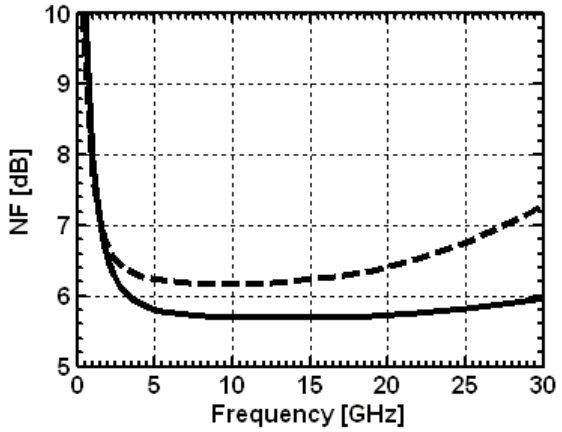
Topology: nMOS TIA with active bias. The CS stage is removed, M_3 added to raise the output CM.

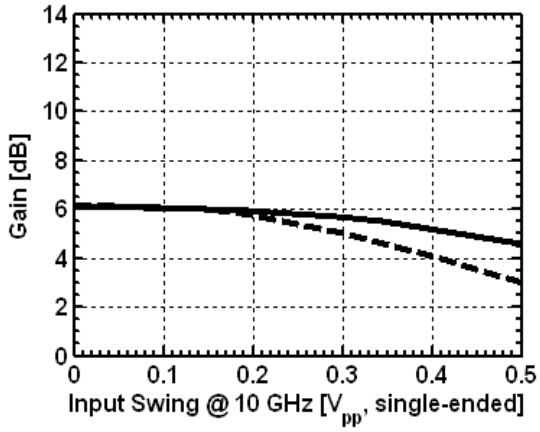
Design - Broadband Preamplifier

- **Simulation comparison results:**





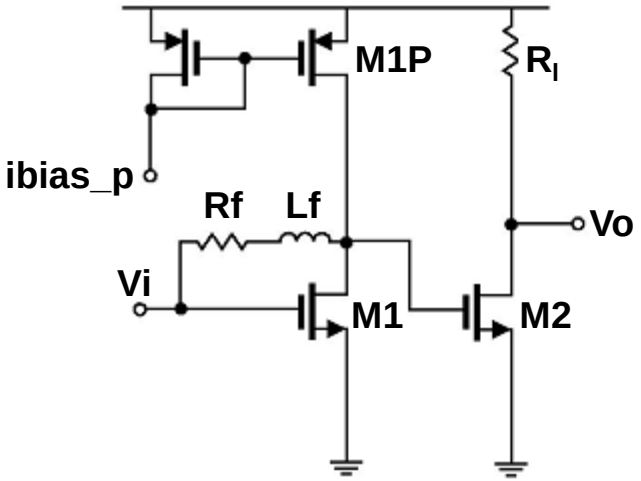




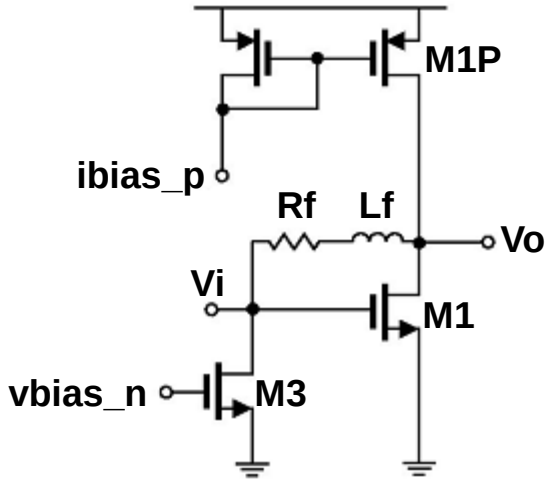
nMOS TIA with active bias (solid) and nMOS TIA with CS (dashed). Both topologies were designed to have the same A_{DC} and BW. At 10 GHz, active-bias topology has 0.5-dB lower NF and 50% higher input P_{1dB}.

Design - Broadband Preamplifier

- By increasing R_I, the nMOS TIA with CS can have significantly larger gain, and so is preferable where large voltage gain is desired.
- In this work, the output is linearly processed by the rest of the AFE. Based on the previous simulation comparison, the nMOS TIA with active bias was used.



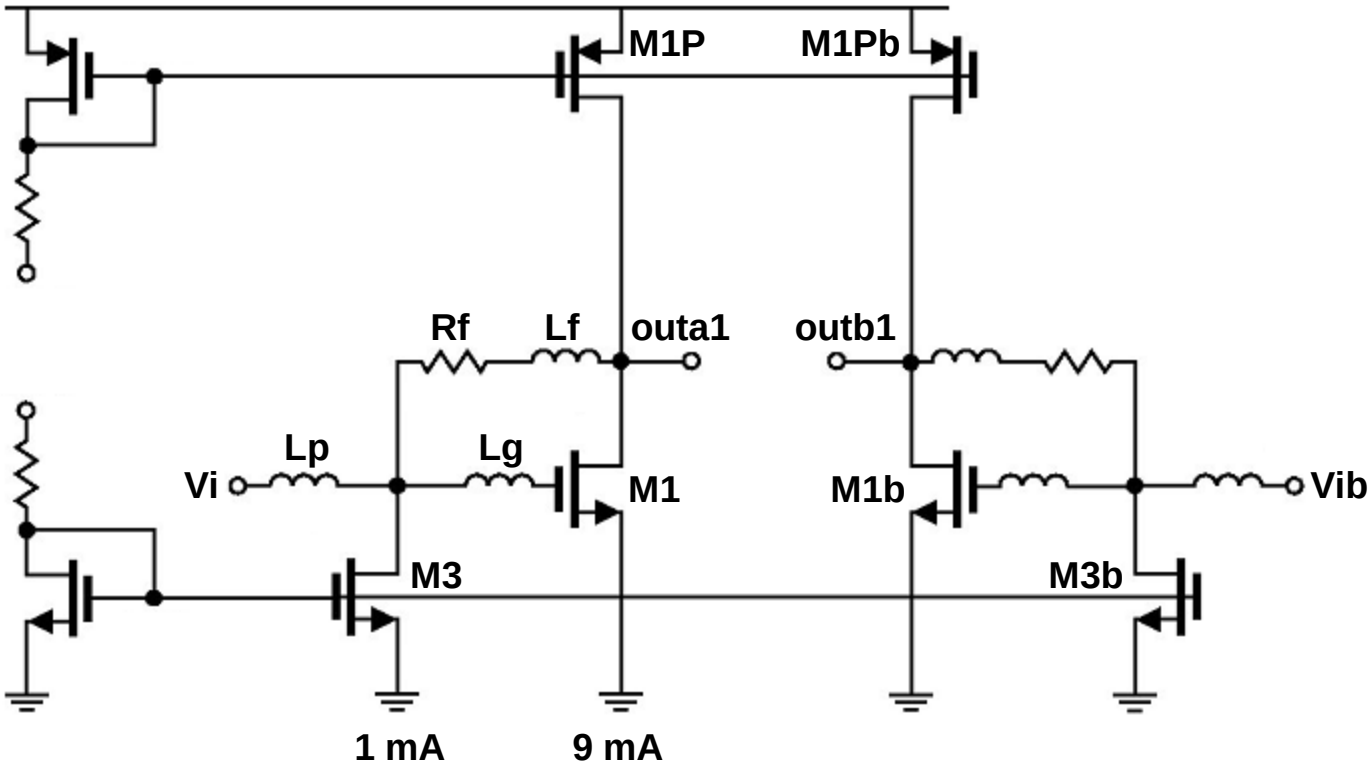
nMOS TIA with CS.



nMOS TIA with active bias.

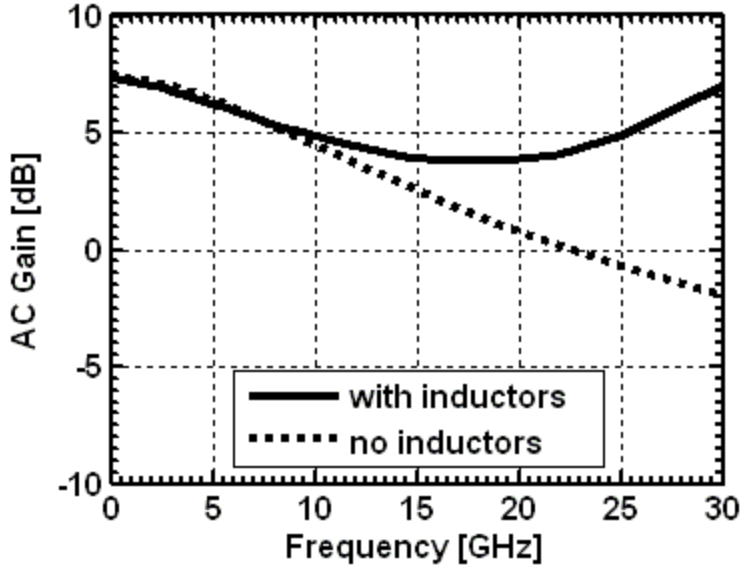
Design - Broadband Preamplifier

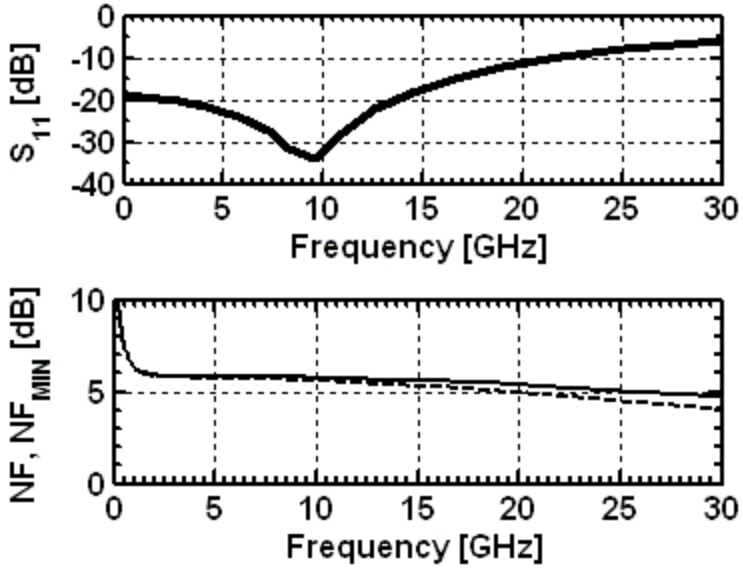
- **Implemented nMOS TIA with active bias.**
- **Dummy stage used for power supply rejection.**



Design - Broadband Preamplifier

- **Simulation results:**





AC gain (single-ended input).
A_{DC} = 7.5 dB, BW = 11.6 GHz.

$|S_{11}|$, NF and NF_{MIN}.
$|S_{11}|$ < -15 dB up to 16.6 GHz,
NF @ 10 GHz = 5.8 dB.

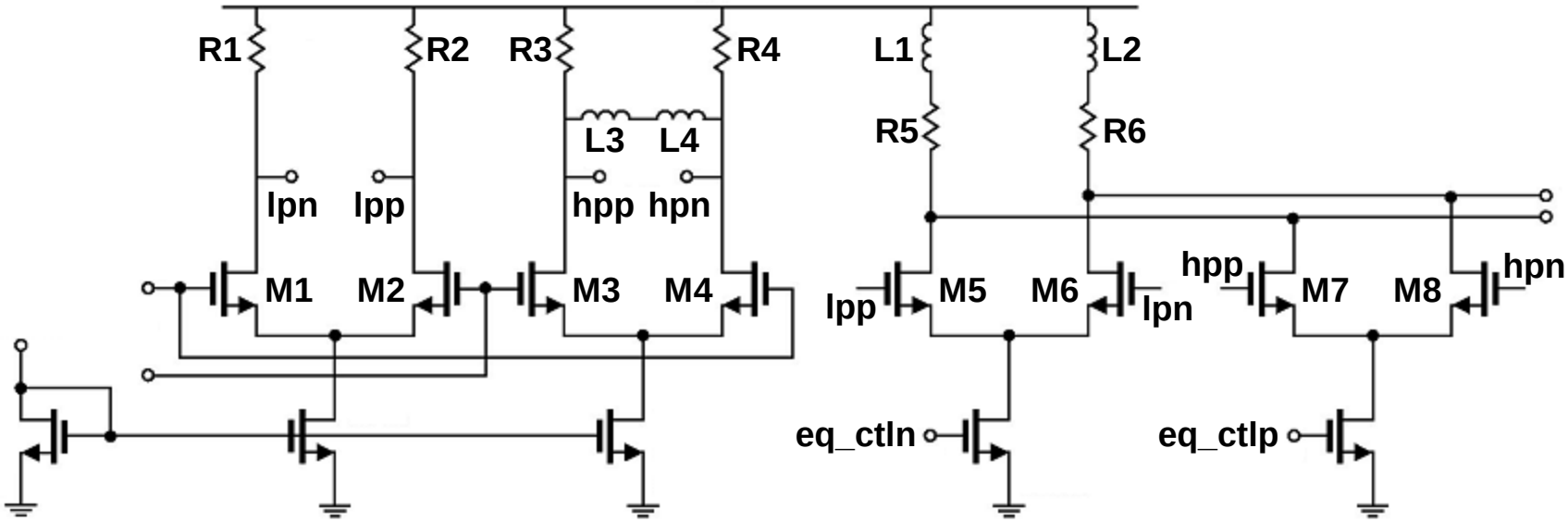
Design – Equalizer

- **Implemented split-path equalizer.**

$$A_{EQ}(s) = A_{DC}(1 + s/\omega_{z1})/(1 + s/\omega_{p1}),$$

$$A_{DC} = g_{m1,2}g_{m5,6}R_{1,2}R_{5,6}$$

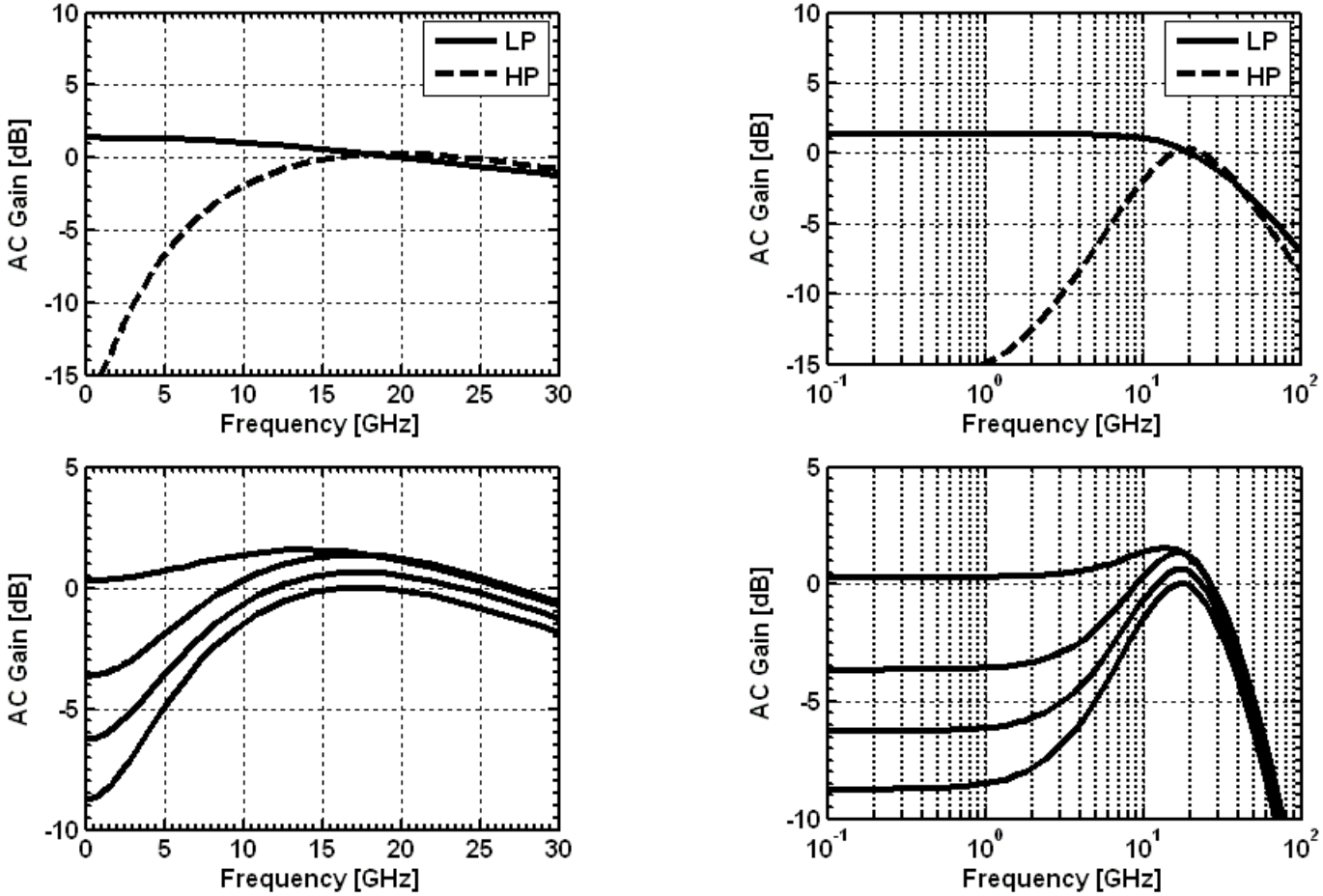
$$\omega_{z1} = \frac{R_{3,4}}{L_{3,4}(1+g_{m7,8}g_{m3,4}R_{3,4}/g_{m5,6}g_{m1,2}R_{1,2})} \qquad \omega_{p1} = \frac{R_{3,4}}{L_{3,4}}$$



LP Path **HP Path** **Weighted Sum**

Design – Equalizer

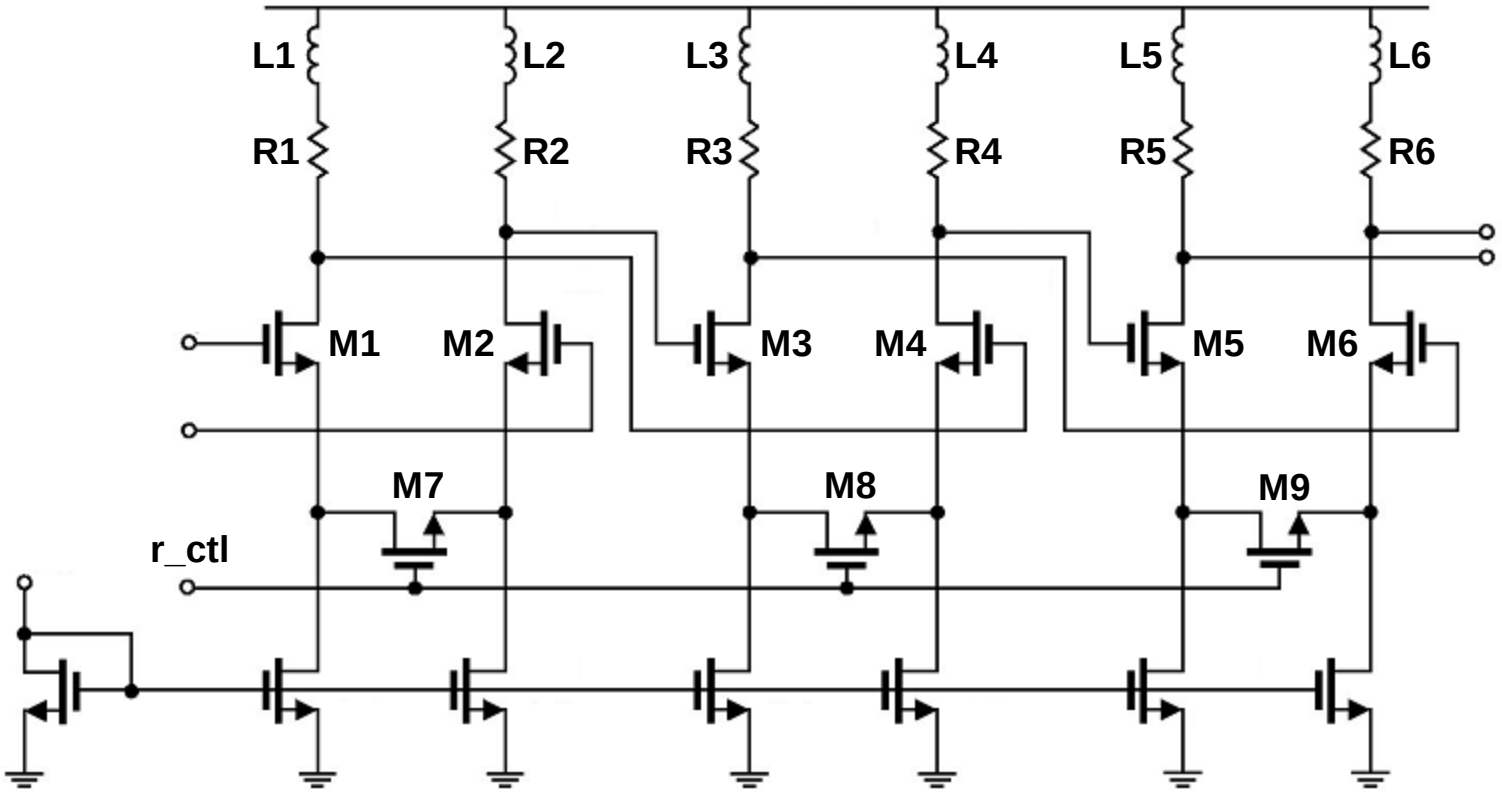
- **Low-pass and high-pass paths are combined:**



AC gains for various equalizer settings on linear and log scales.
A_{DC} = -8.6 - 0.3 dB, maximum peaking = 8.6 dB.

Design – Post-Amplifier

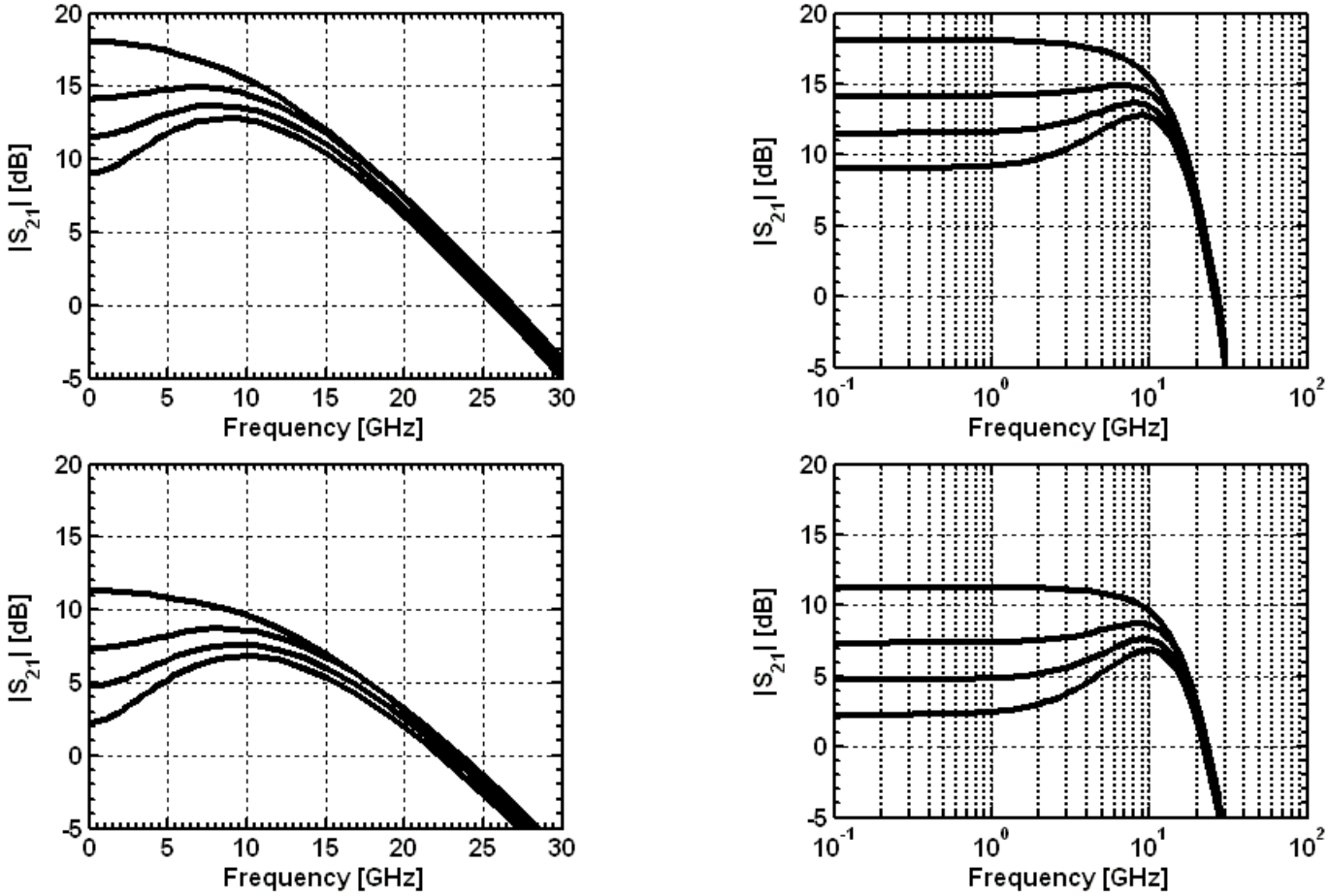
- **Post-amplifier uses three cascaded source-degenerated stages, providing some gain-control.**



A_{DC} = 0 - 6.5 dB, BW ≥ 19.6 GHz

Design – AFE

- **Simulation results - $|S_{21}|$:**



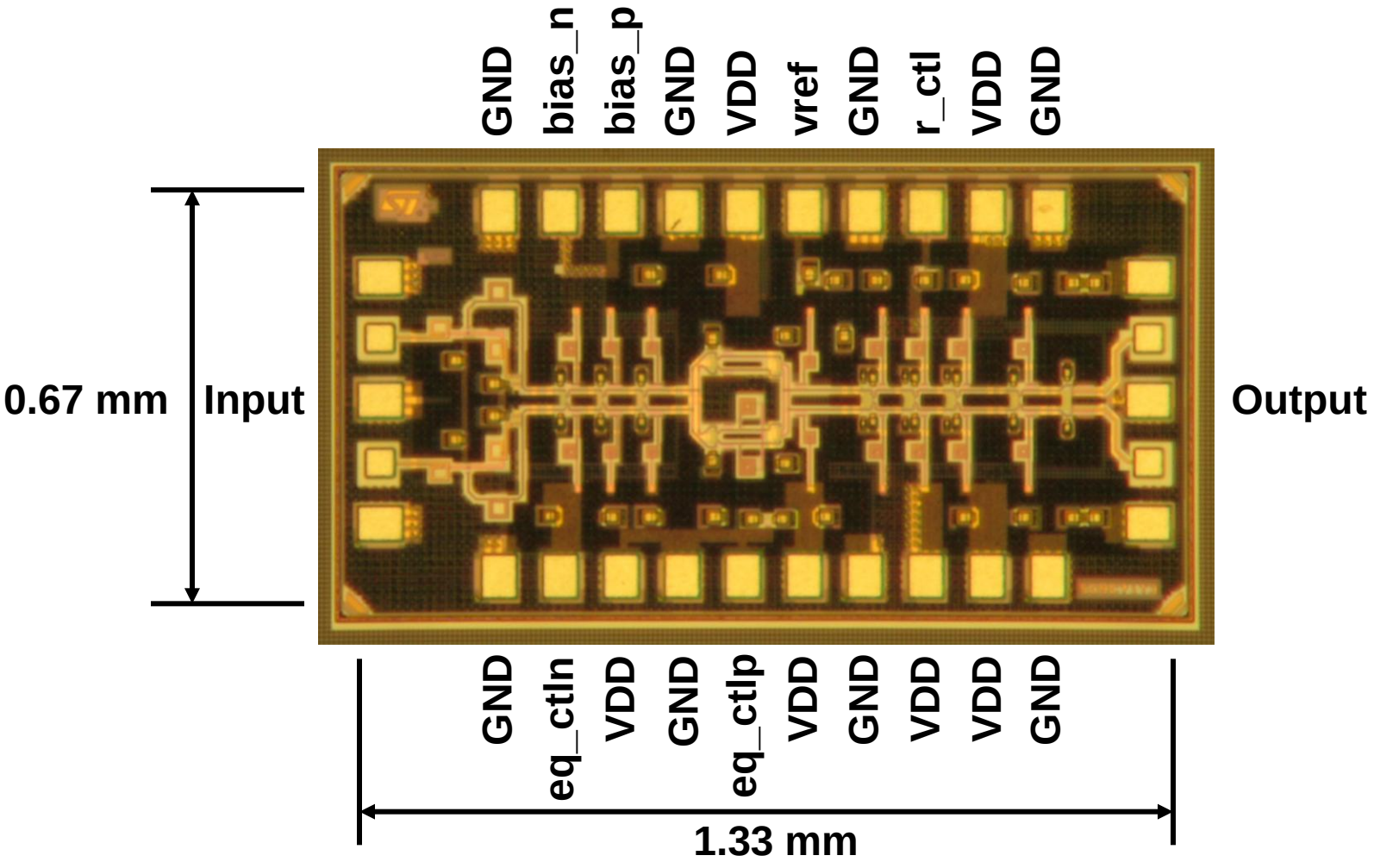
AFE: Simulated single-ended $|S_{21}|$ for maximum (top) and minimum (bottom) post-amplifier gains across equalizer setting.

Design – AFE

- **Simulation results - summary:**

$\|S_{11}\|$ < -15 dB up to:	14.9 GHz
Peaking @ 10 GHz	4.6 dB
Gain control range	6.8 dB
P_{1dB} @ 10 GHz (Excluding output driver) min EQ, min post-amp. gain max EQ, max post-amp. gain	 105 mV_{pp} 98 mV_{pp}
NF @ 10 GHz	12.9 dB
Differential output noise (max EQ, max post-amp. gain)	2.0 mV_{rms}
Input-referred noise (max EQ, max post-amp. gain)	0.36 mV_{rms}
Input sensitivity @ BER = 10^{-15}	5.7 mV_{pp}

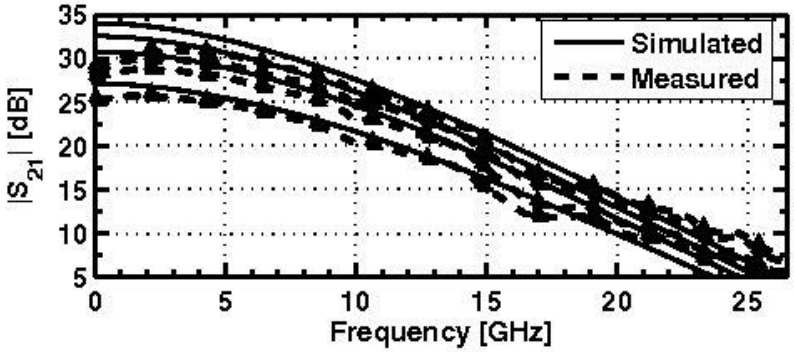
Measurements

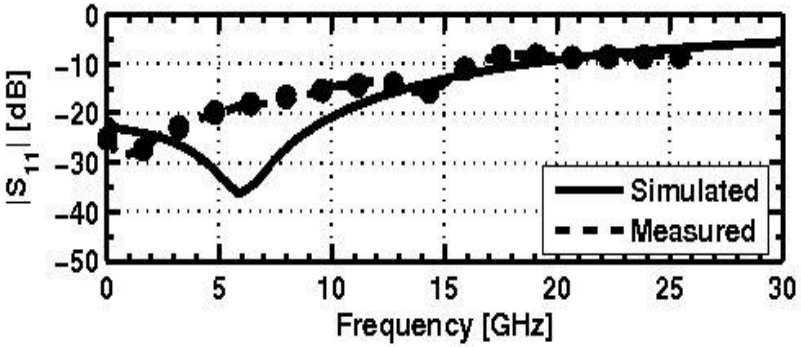


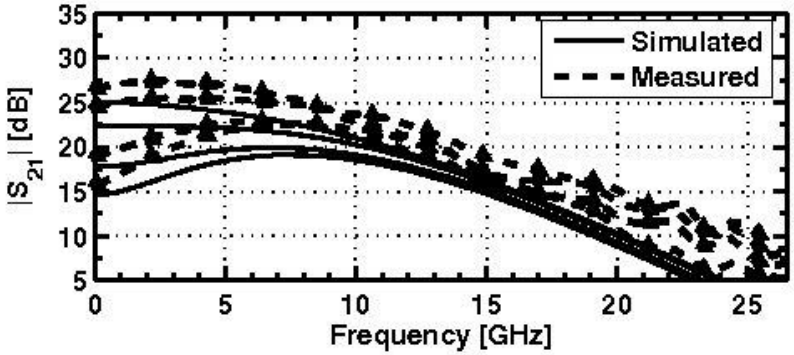
- **Power/Area: 138 mW/0.89 mm^2**

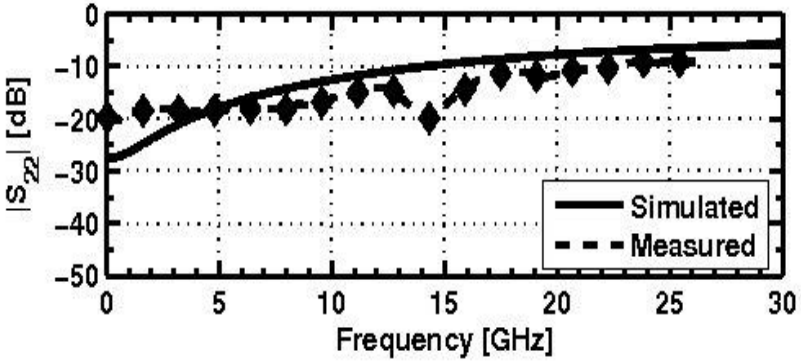
S Parameter Measurements

- **$|S_{11}|$, $|S_{22}|$ < -10 dB up to 16, 20 GHz, respectively (converted from 50-ohm to 75/50-ohm input/output environment)**





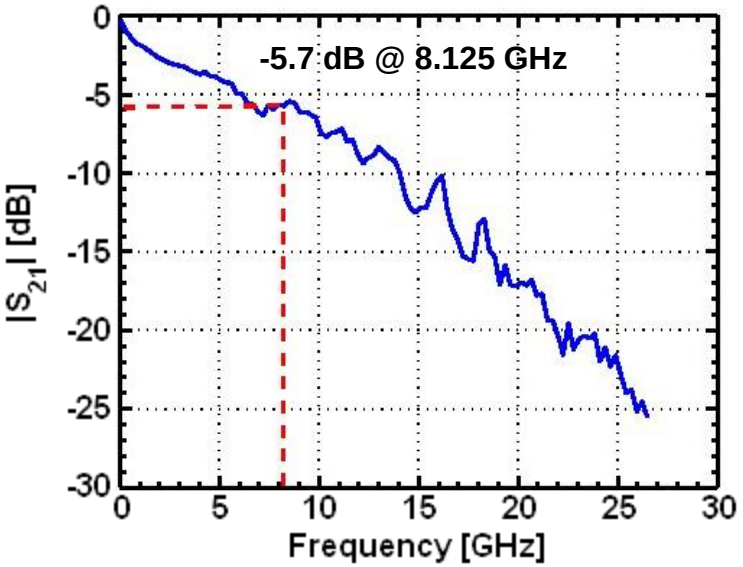


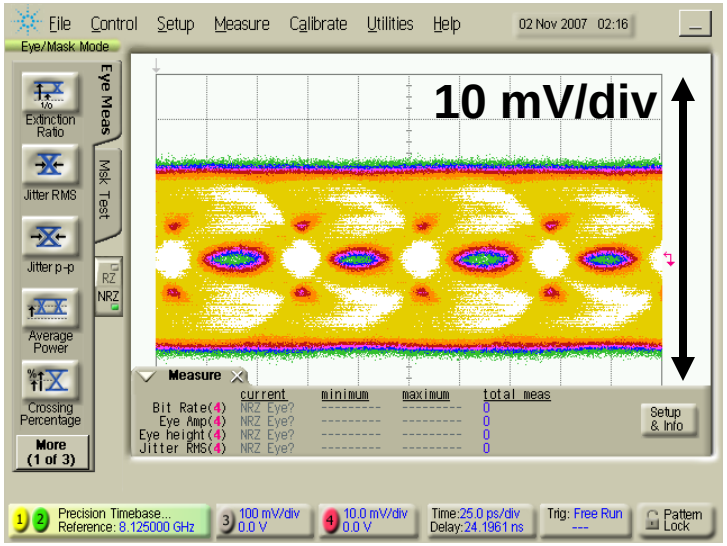


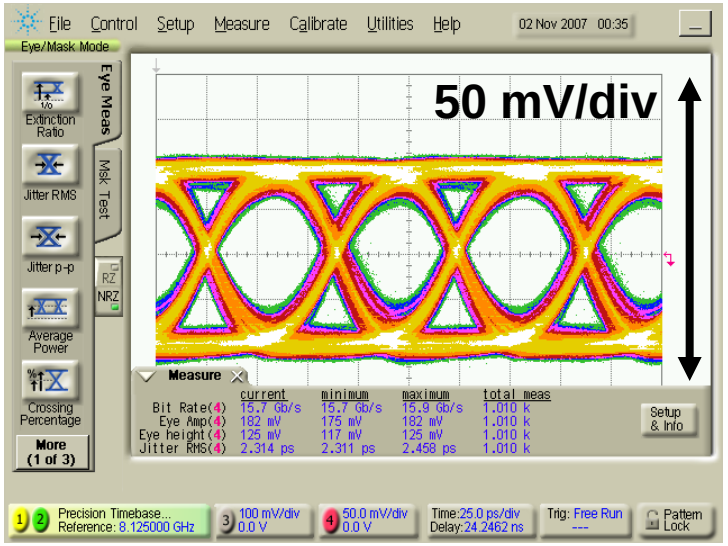
Transient Measurements

- **16.25 Gb/s, 9-ft SMA cable**
- **Launch amplitude ~ 47 mV**

Potential TX power savings



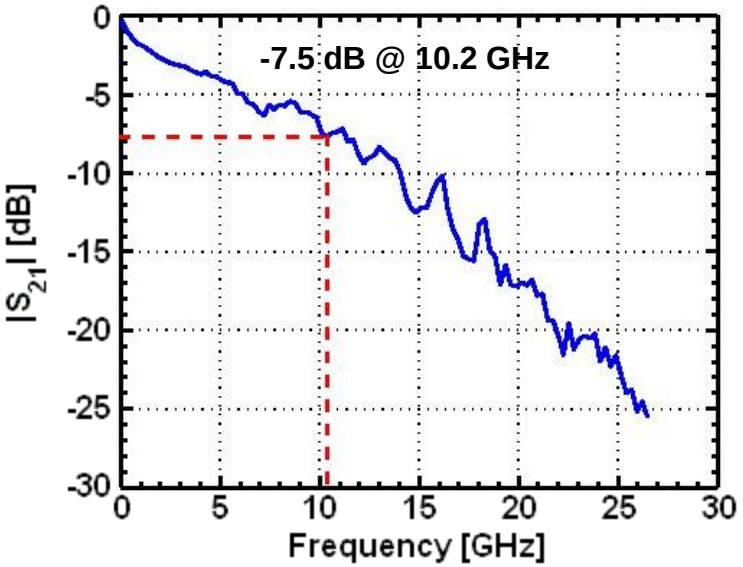


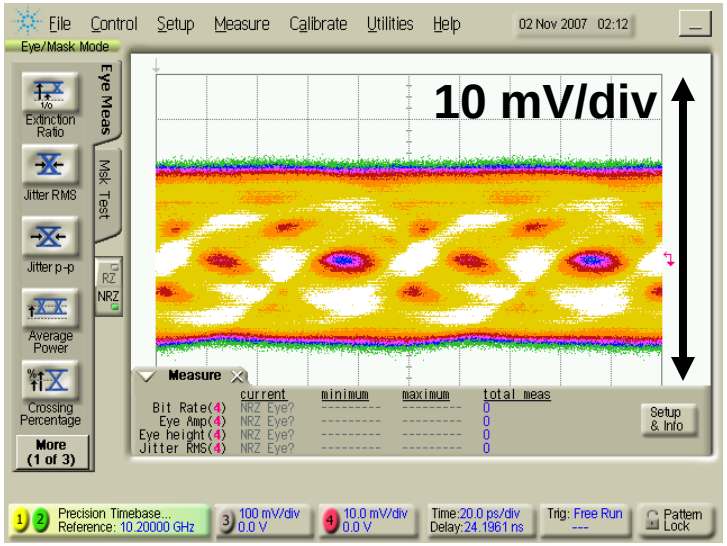


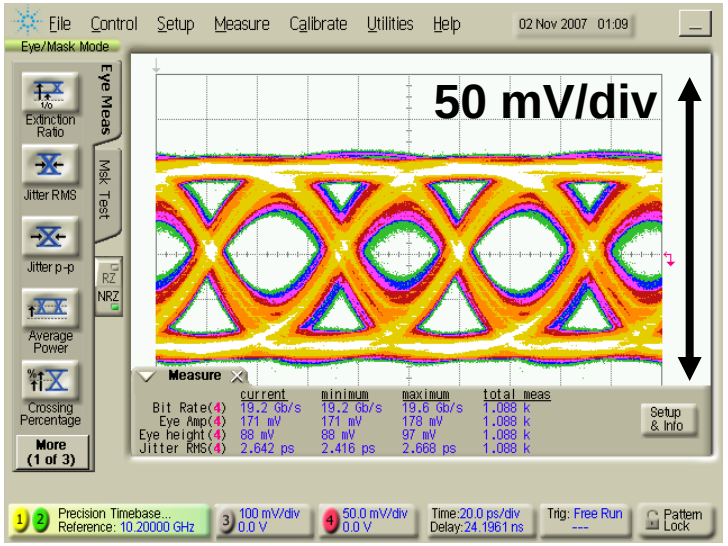
Transient Measurements

- **20.4 Gb/s, 9-ft SMA cable**
- **Launch amplitude ~ 47 mV**

Potential TX power savings







Measurement Summary

Technology/Supply	90-nm CMOS/1.3 V	
Power/Area	138 mW/0.89 mm^2	
$\|S_{11}\|$, $\|S_{22}\|$	< -10 dB up to 16, 20 GHz	
Maximum Peaking	6.5 dB @ 8 GHz	
Gain Control Range	6.0 dB	
GBW Product (differential)	≥ 294 GHz	
P_{1dB}	1 GHz	7 GHz
(no EQ, min gain)	-30.75 dBm	-31.6 dBm
(no EQ, max gain)	-39.75 dBm	-38.6 dBm
(max EQ, max gain)	-36.75 dBm	-35.6 dBm
Bit Rate	16.25 Gb/s	20.4 Gb/s
9-ft SMA Cable Loss	5.7 dB @ 8.125 GHz	7.5 dB @ 10.2 GHz
Input Swing (single-ended)	40 mV_{pp}	40 mV_{pp}
Output Swing (single-ended)	225 mV_{pp}	225 mV_{pp}
RMS Jitter	2.5 ps	2.7 ps
Timing Margin (BER = 10^{-12})	0.58 UI	0.32 UI

Comparison - Equalizers

Reference	[ZG05]	[HMC+05]	[GLTR05]	[Lee06]	[TKO+05]	[SC06]	[LL08b]	This Work
Bit Rate (Gb/s)	10	10	10	20	10	30	40	20. 4
Loss[1] (dB)	13	18	19	9.5	20	14.5	10	7.5
Supply (V)	3.3	1.8	1.2	1.5	1.2	1	–	1.3
EQ Power (mW)	155	7.3	25	60	13.2	25	58	31 (sim.)
Adaptive	YES	NO	YES	YES	YES	NO	YES	NO
Type[2]	SP	4-FIR	CD	CD	CH	3-FIR	SP+CD	SP
Process	0.18-um BiCMOS	0.18-um CMOS	0.13-um CMOS	0.13-um CMOS	0.11-um CMOS	90-nm CMOS	90-nm CMOS	90-nm CMOS
Area (mm^2)	0.705	–	0.162 (CORE)	0.2 (CORE)	0.004 (EQ)	0.3	0.539	0.891

[1] Loss compensated at one-half the symbol rate.
[2] SP: split-path; CD: capacitive-degeneration; CH: Cherry-Hooper.

Comparison – CMOS Amplifiers

Reference	[GR04]	[SSH+04]	[CL07]	[WSJ06]	[LL08a]	[LWL+05]	[TWKC05]	This Work
Bit Rate (Gb/s)	40	40	40	40	40	N/A	N/A	20.4
Supply (V)	2.2	1.8	2.8	1	1.2	2.4	–	1.3
Power (mW)	190	140	250	80	75	120	122	138
Diff. Gain (dB)	15	4	20	20	26	7.4	7	31.2
BW (GHz)	22	39	39.4	23	22	80	70	8.1
GBP (GHz)	124	62	394	230	440	188	157	294
VGA	NO	NO	NO	YES	YES	NO	NO	YES
Type[1]	CGS	DA	DA	CGS	CGS	DA	DA	CGS
Process	0.18-um CMOS	0.18-um CMOS	0.18-um CMOS	90-nm CMOS	90-nm CMOS	90-nm CMOS	90-nm CMOS	90-nm CMOS
Area (mm^2)	0.5	3.3	2.24	0.033 (CORE)	0.56	0.72	0.72	0.891

[1] CGS: cascaded gain stage; DA: distributed amplifier.

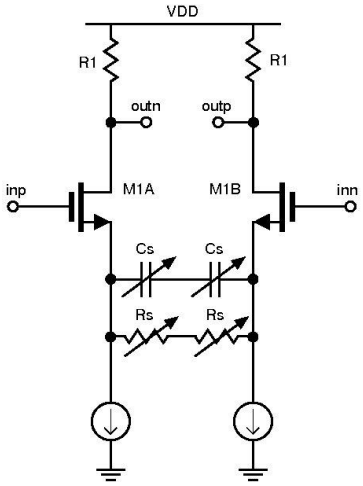
Conclusion

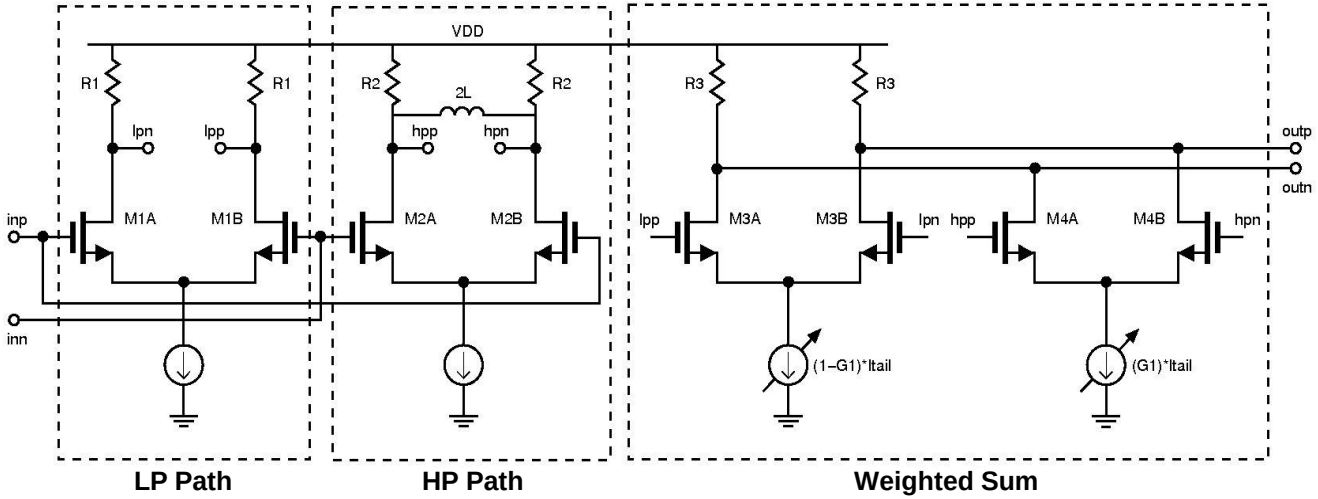
- **A binary receiver AFE targeting 20 Gb/s for coaxial cable was designed in 90-nm CMOS.**
- **The nMOS TIA with active bias used as the preamplifier had not previously been implemented in CMOS.**
- **Main AFE blocks were the broadband preamplifier, analog (split-path) peaking equalizer and post-amplifier, and functionality was verified by measurement up to 20.4 Gb/s.**

Backup Slides

Equalizer Comparison

- **Capacitive-degeneration (CD) and split-path (SP) equalizers have similar transfer functions, but the SP equalizer was chosen due to 1) the absence of varactor models and 2) potentially greater single-stage peaking.**





$A_{CD}(s) = A_{DC}(1 + s/\omega_{z1})/(1 + s/\omega_{p1})$

$A_{DC} = g_{m1}R_1/(1 + g_{m1}R_s)$

$\omega_{z1} = 1/C_sR_s$

$\omega_{p1} = (1 + g_{m1}R_s)/C_sR_s$

$A_{SP}(s) = A_{DC}(1 + s/\omega_{z1})/(1 + s/\omega_{p1})$

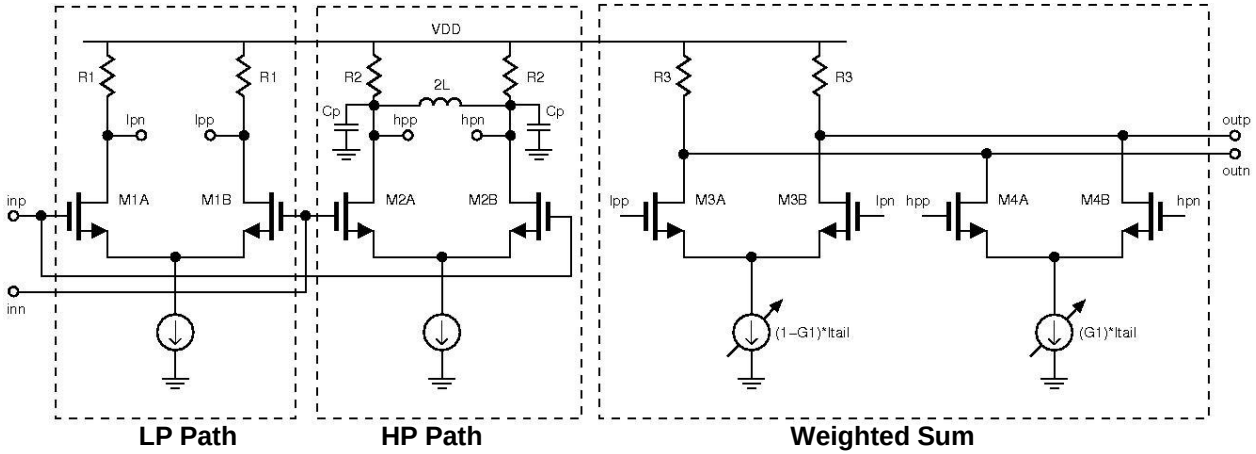
$A_{DC} = g_{m1}g_{m3}R_1R_3$

$\omega_{z1} = R_2/L(1+g_{m4}g_{m2}R_2/g_{m3}g_{m1}R_1)$

$\omega_{p1} = R_2/L$

Equalizer Comparison

- **The split-path (SP) equalizer actually has a 2nd order transfer function due to the "tank" capacitance C_p:**



$$A_3 = g_{m3}g_{m1}R_3R_1$$

$$A_4 = g_{m4}g_{m2}R_3R_2$$

$$\omega_0 = \sqrt{\frac{1}{LC_p}}$$

$$Q = \omega_0 C_p R_2$$

$$A_{SP}(s) = \frac{v_{out}}{v_{in}} = A_3 \frac{\left[s^2 + s\frac{\omega_0}{Q}\left[1+\frac{A_4}{A_3}\right] + \omega_0^{\,2}\right]}{s^2 + s\frac{\omega_0}{Q} + \omega_0^{\,2}}$$

$$Boost\ Ratio = \frac{A(\omega_0)}{A(\omega_{DC})} = 1 + \frac{A_4}{A_3} = 1 + \frac{g_{m4}g_{m2}R_2}{g_{m3}g_{m1}R_1}$$

Equalizer transfer function (2nd order).

$A_{SP}(s) = A_{DC}(1 + s/\omega_{z1})/(1 + s/\omega_{p1})$

$A_{DC} = g_{m1}g_{m3}R_1R_3$

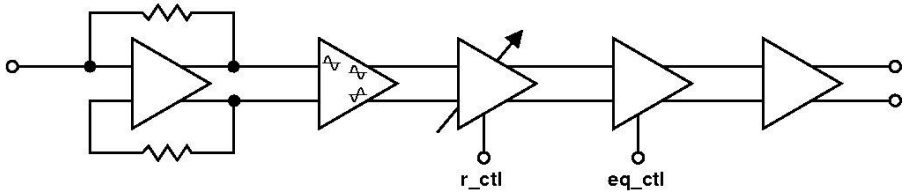
$\omega_{z1} = R_2/L(1+g_{m4}g_{m2}R_2/g_{m3}g_{m1}R_1)$

$\omega_{p1} = R_2/L$

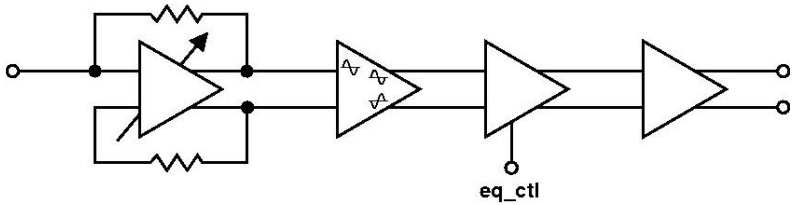
Equalizer transfer function (1st order).

Note that the boost ratio from the 2nd order transfer function is equal to ω_{p1}/ω_{z1} derived using the 1st order expressions. This implies that both expressions predict the same amount of gain boost relative to DC.

Architecture - AFE Blocks



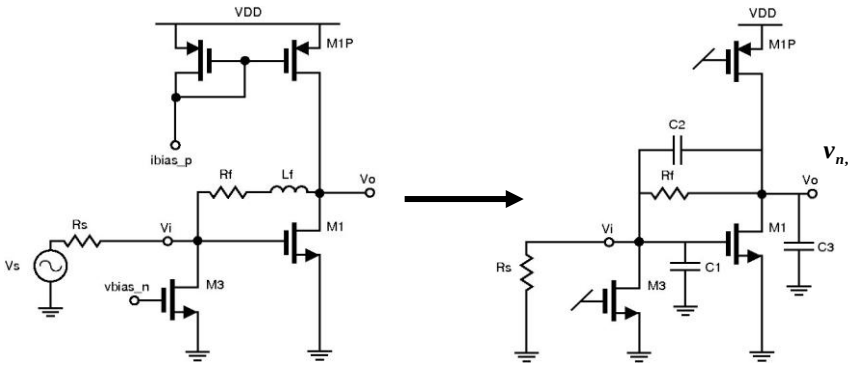
Alternative 1: Post-amplifier before the equalizer. This may be better for noise, since the post-amplifier gain is closer to the input side (and the equalizer has loss). However, this would require a larger equalizer input-swing limit.



Alternative 2: VGA integrated with (or before) the broadband preamplifier. This is probably best in terms of noise, as the required gain is at the front. However, only gain *reduction* is easily implemented here. Subsequent gain stages would still likely be required. Input matching might be affected.

Design – Broadband Preamplifier

- **Noise contribution of the active bias device (M_3):**



$$v_{n,M_3,0}^{\ 2} = \left(I_{n,M_3}^{\ 2}\right) \left| \left(R_S \parallel Z_F \parallel r_{03} \parallel \frac{1}{sC_1} \parallel \frac{1}{sC_2}\right)\left(g_{m1} - \frac{1}{\left(Z_F \parallel \frac{1}{sC_2}\right)}\right) \right|^2 \Bigg/ \left| \frac{1}{Z_F \parallel r_{01} \parallel r_{02} \parallel \frac{1}{sC_2} \parallel \frac{1}{sC_3}} + \frac{\left(R_S \parallel Z_F \parallel r_{03} \parallel \frac{1}{sC_1} \parallel \frac{1}{sC_2}\right)}{\left(Z_F \parallel \frac{1}{sC_2}\right)}\left(g_{m1} - \frac{1}{\left(Z_F \parallel \frac{1}{sC_2}\right)}\right) \right|^2$$

(1) $v_i = \left(\frac{v_0}{z_2} + i_n\right)\left(z_1 \parallel z_2\right)$

(2) $\frac{v_0 - v_i}{z_2} + g_{m1} v_i + \frac{v_0}{z_3} = 0$

$z_1 = \left(R_S \parallel r_{03} \parallel \frac{1}{sC_1}\right)$

$z_2 = \left(Z_F \parallel \frac{1}{sC_2}\right)$

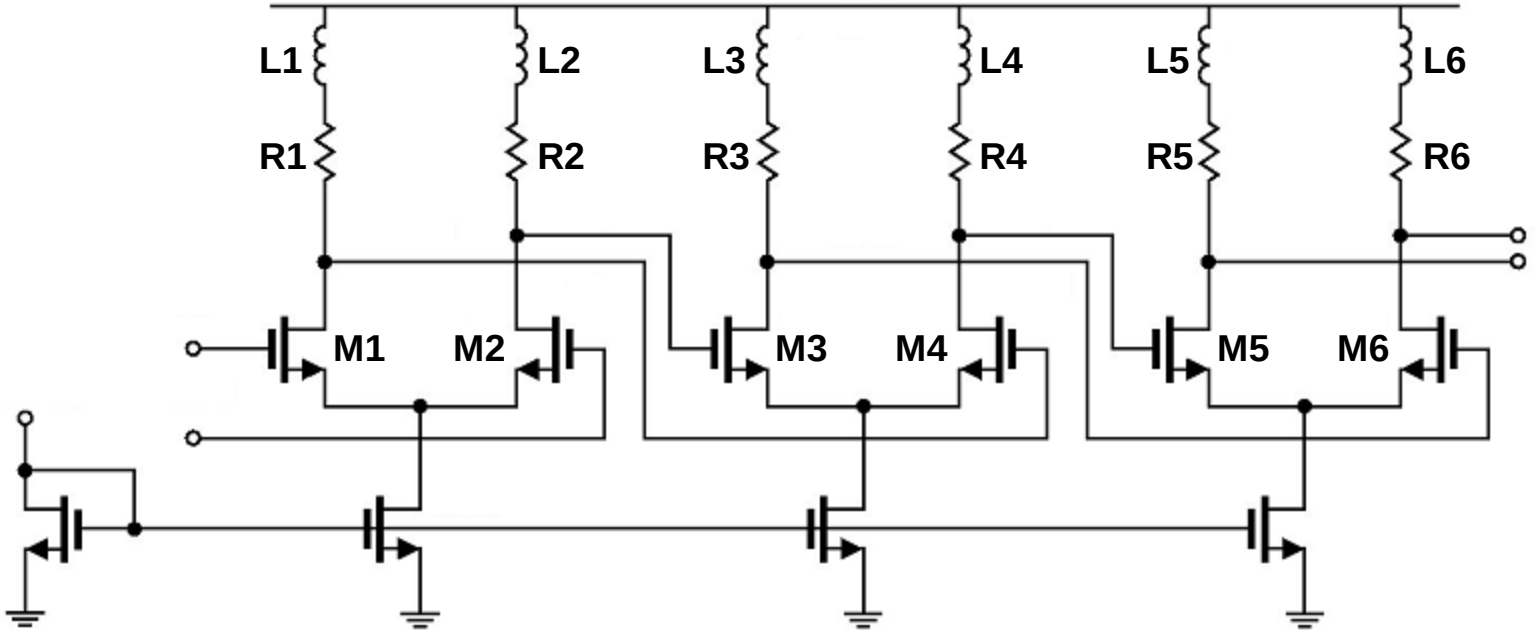
$z_3 = \left(r_{01} \parallel r_{02} \parallel \frac{1}{sC_3}\right)$

$$\left|A_v\right|^2 = \left(\frac{1}{R_S^{\ 2}}\right) \left| \left(R_S \parallel Z_F \parallel r_{03} \parallel \frac{1}{sC_1} \parallel \frac{1}{sC_2}\right)\left(\frac{1}{\left(Z_F \parallel \frac{1}{sC_2}\right)} - g_{m1}\right) \right|^2 \Bigg/ \left| \frac{1}{Z_F \parallel r_{01} \parallel r_{02} \parallel \frac{1}{sC_2} \parallel \frac{1}{sC_3}} + \frac{\left(R_S \parallel Z_F \parallel r_{03} \parallel \frac{1}{sC_1} \parallel \frac{1}{sC_2}\right)}{\left(Z_F \parallel \frac{1}{sC_2}\right)}\left(g_{m1} - \frac{1}{\left(Z_F \parallel \frac{1}{sC_2}\right)}\right) \right|^2$$

Noise of M_3 referred to v_s: $\therefore v_{n,M_3,in}^{\ 2}(f) = \left(4kT\gamma g_{m3} + \frac{K_N}{C_{ox} W_3 L_3 f} g_{m3}^{\ 2}\right) R_S^{\ 2}$

Design – S2D

- **Single-ended to differential (S2D) block is used as the preamplifier has no common-mode (CM) rejection.**

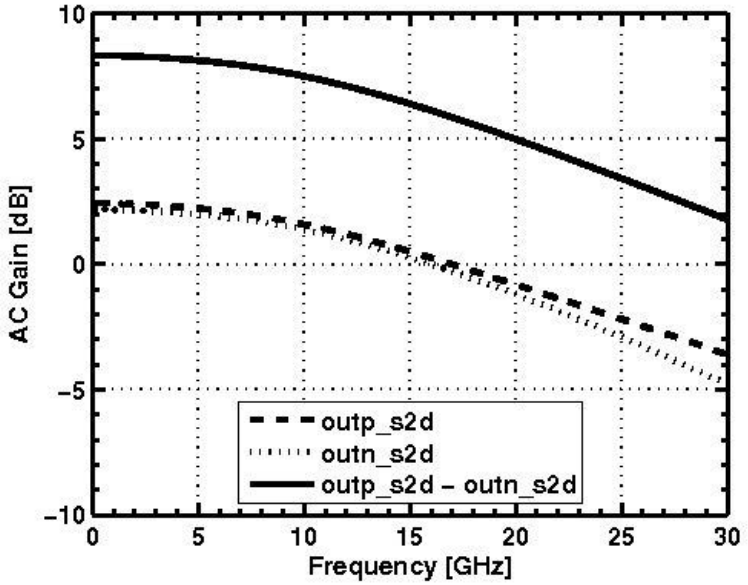


A_{DC} = 8.3 dB, BW = 19.0 GHz.

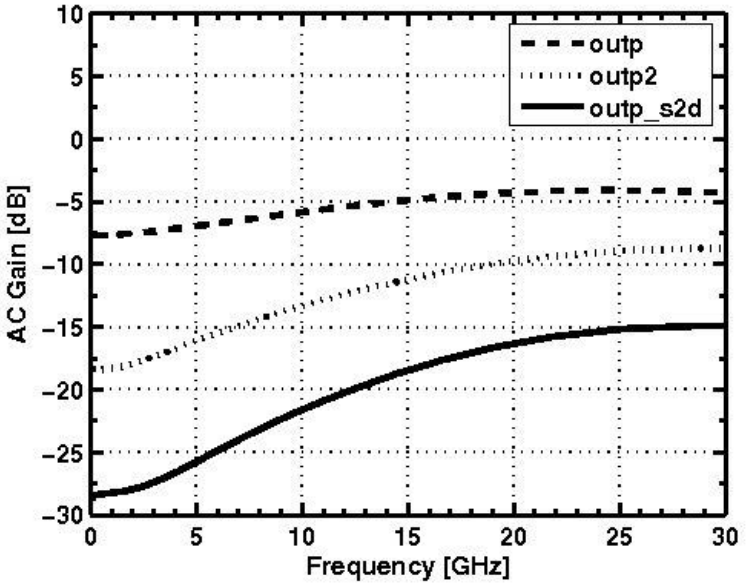
A_{CM} @ 10 GHz = -21.5 dB.

Design – S2D

- **Simulation results:**



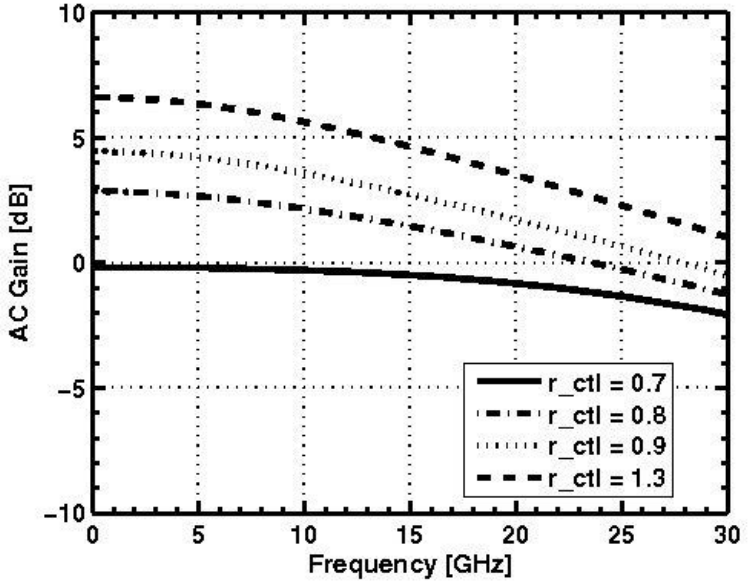
AC gain (single-ended input).
A_{DC} = 8.3 dB, BW = 19.0 GHz.



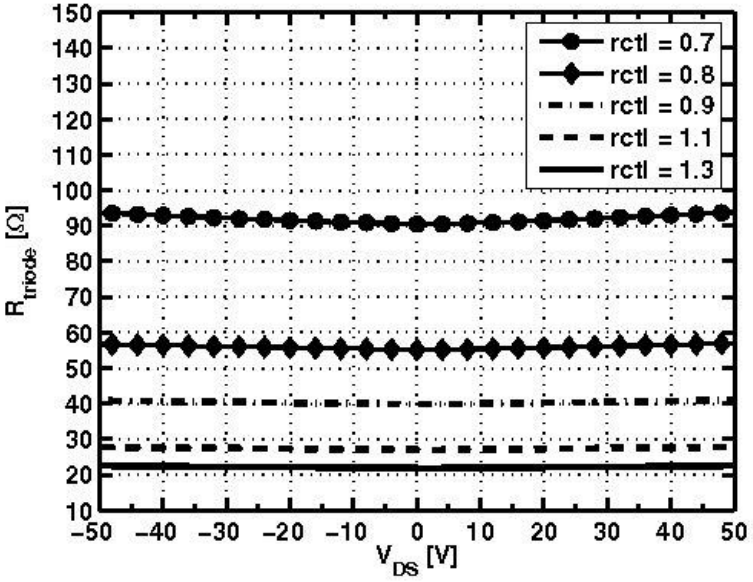
CM gain.
A_{CM} @ 10 GHz = -21.5 dB.

Design – Post-Amplifier

- **Simulation results:**



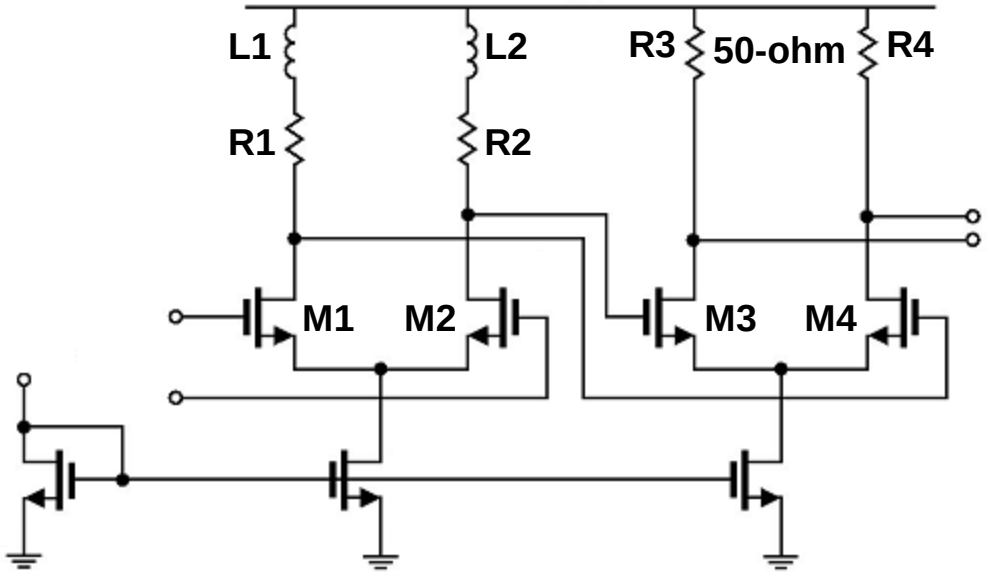
A_{DC} = 0 - 6.5 dB,
BW ≥ 19.6 GHz

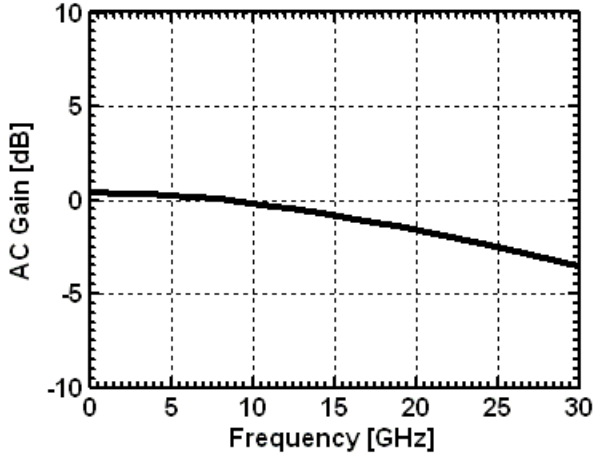


Resistance of triode-region nMOS vs. V_{DS} for various values of *r_ctl*.
ΔR_{triode} (@ V_{DS} = 50 mV) is 3.8% .

Design – Output Driver

- **The output driver provides ~0-dB gain to the 50-ohm testing environment.**

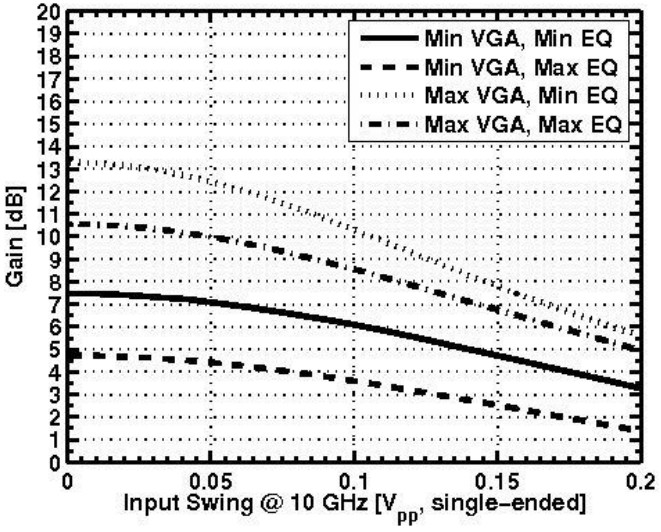




A_{DC} = 0.4 dB, BW = 25.6 GHz

Design – AFE

- **Simulation results - linearity:**



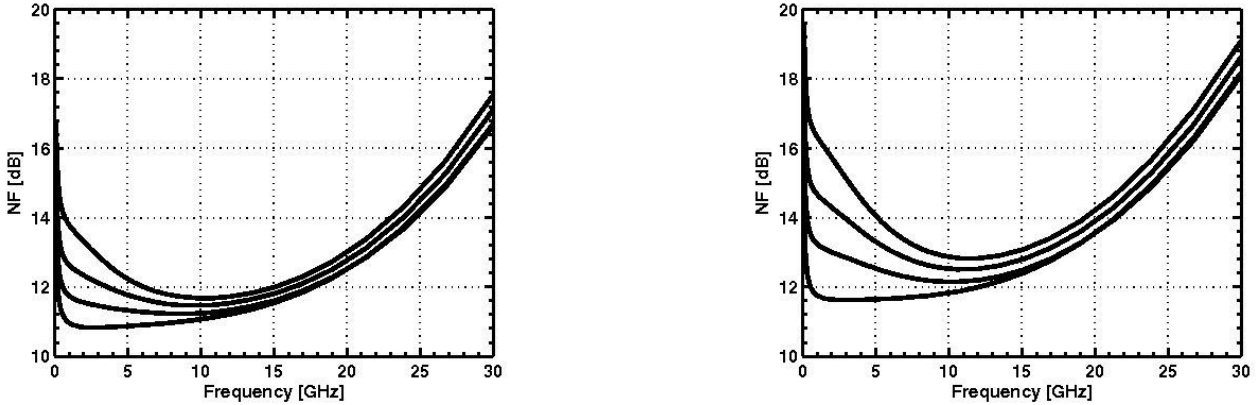
Gain compression at 10 GHz.

VGA	EQ	P_{1dB} @ 10 GHz	P_{1dB} @ 10 GHz (no output driver)
Min	Min	82 mV_{pp}	105 mV_{pp}
Min	Max	93 mV_{pp}	108 mV_{pp}
Max	Min	54 mV_{pp}	87 mV_{pp}
Max	Max	68 mV_{pp}	98 mV_{pp}

Single-ended input P_{1dB} @ 10 GHz.

Design – AFE

- **Simulation results - noise:**



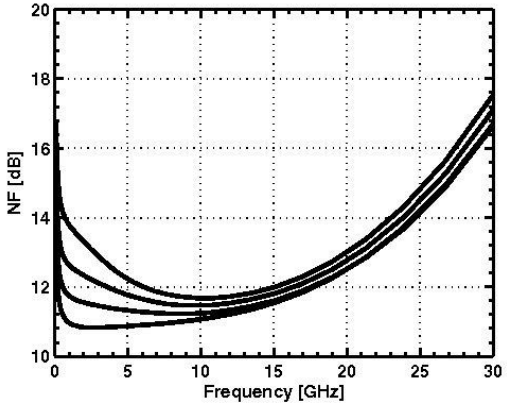
AFE: Simulated single-ended NF for maximum (left) and minimum (right) VGA gains across equalizer setting.

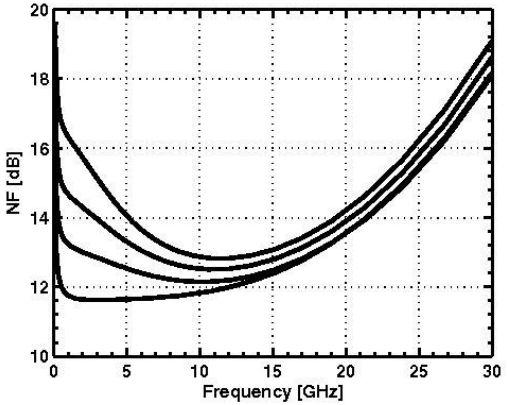
VGA	EQ	Input-referred noise	Differential output noise
Min	Min	0.22 mV_{rms}	1.6 mV_{rms}
Min	Max	0.49 mV_{rms}	1.3 mV_{rms}
Max	Min	0.18 mV_{rms}	3.0 mV_{rms}
Max	Max	0.36 mV_{rms}	2.0 mV_{rms}

AFE: Simulated noise voltages at the limits of VGA and equalizer controls.

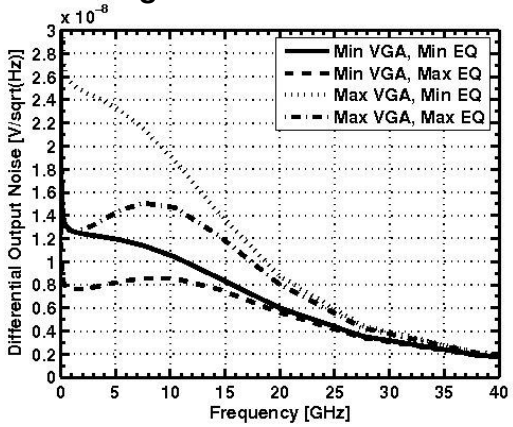
Design – AFE

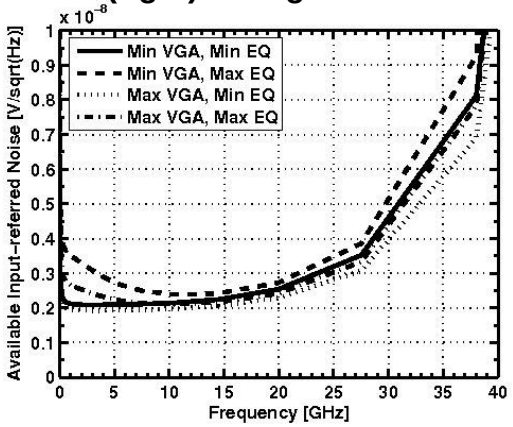
- **Simulation results - noise:**





AFE: Simulated single-ended NF for maximum (left) and minimum (right) VGA gains across equalizer setting.

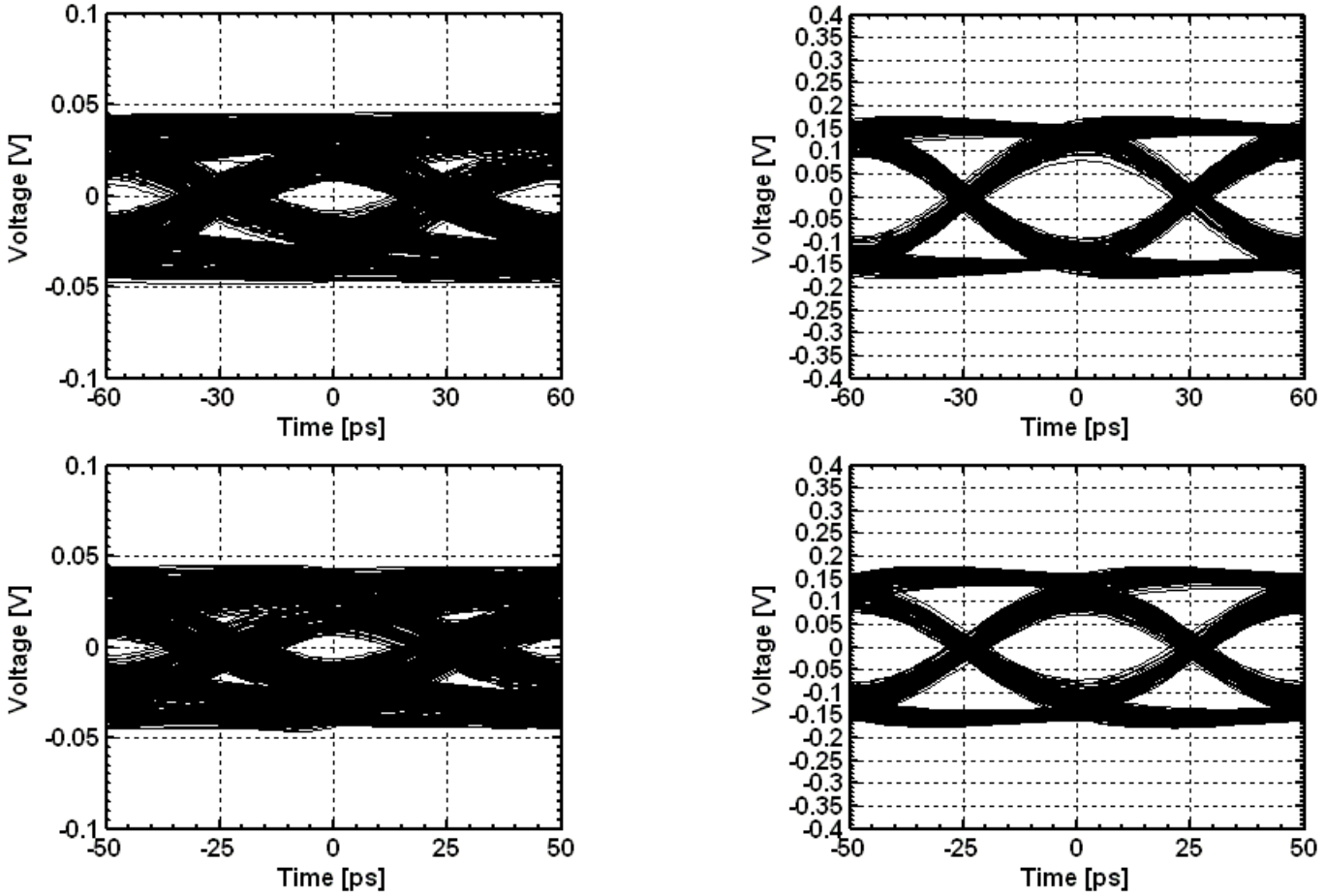




AFE: Simulated noise voltages at the limits of VGA and equalizer controls: differential output noise (left) and single-ended available input-referred noise (right).

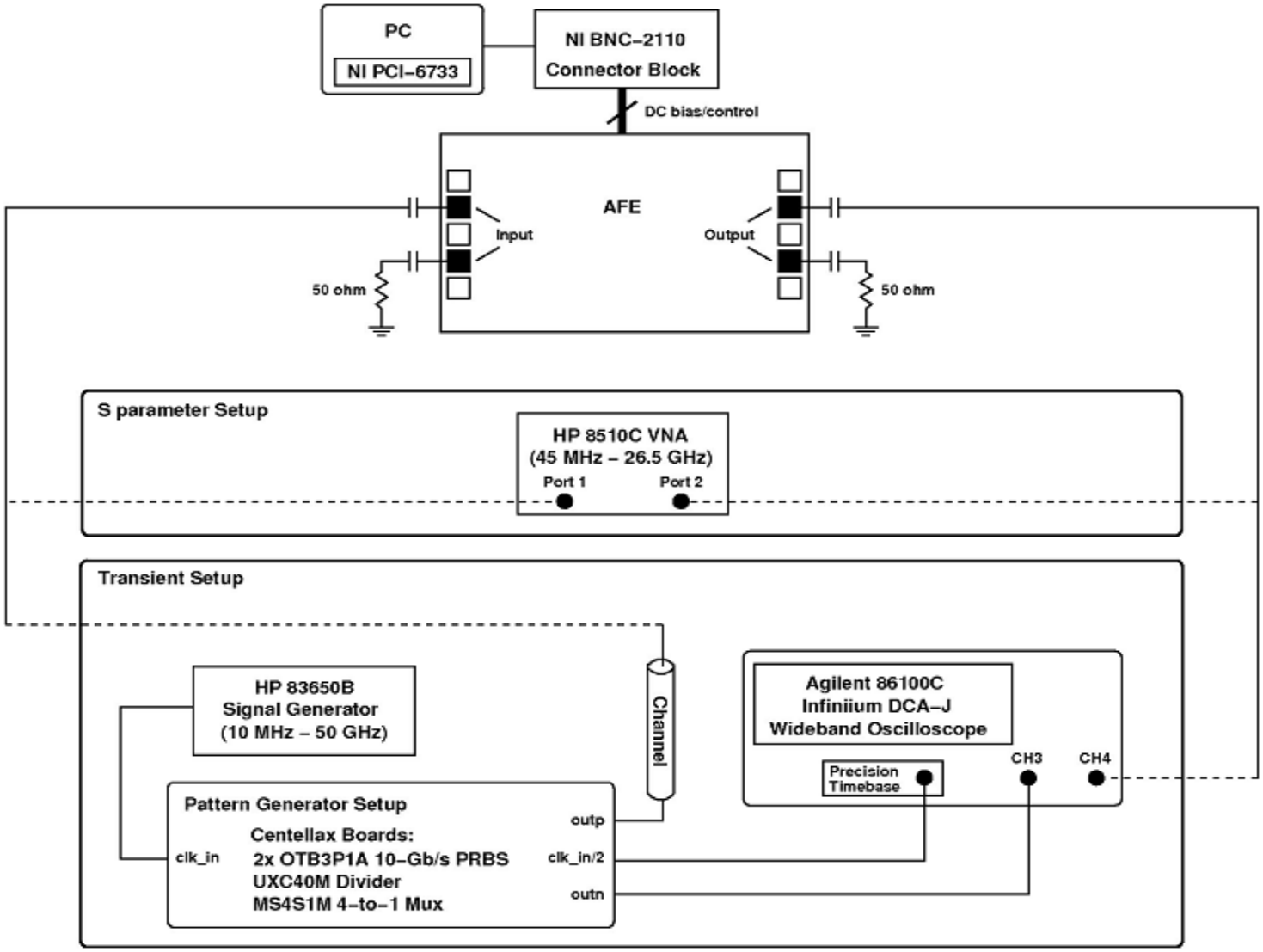
Design – AFE

- **Simulation results - transients:**

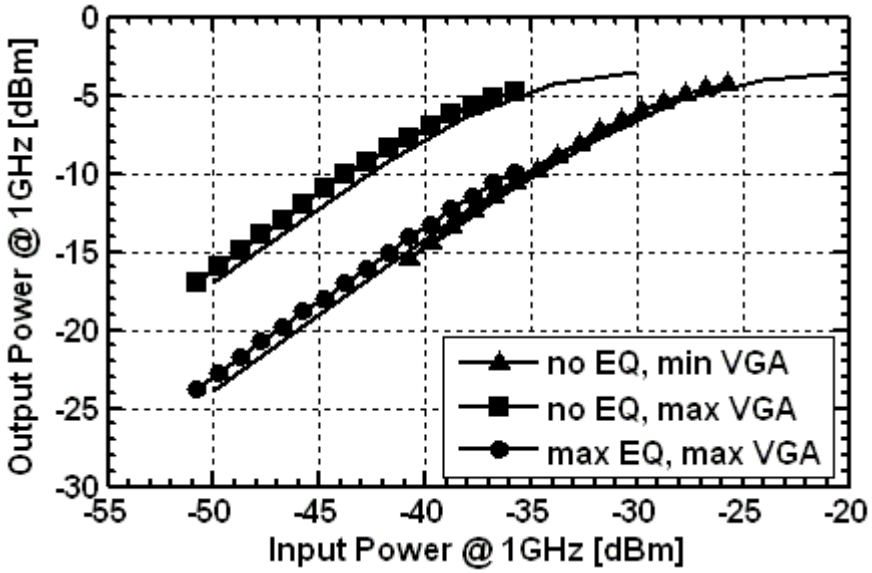


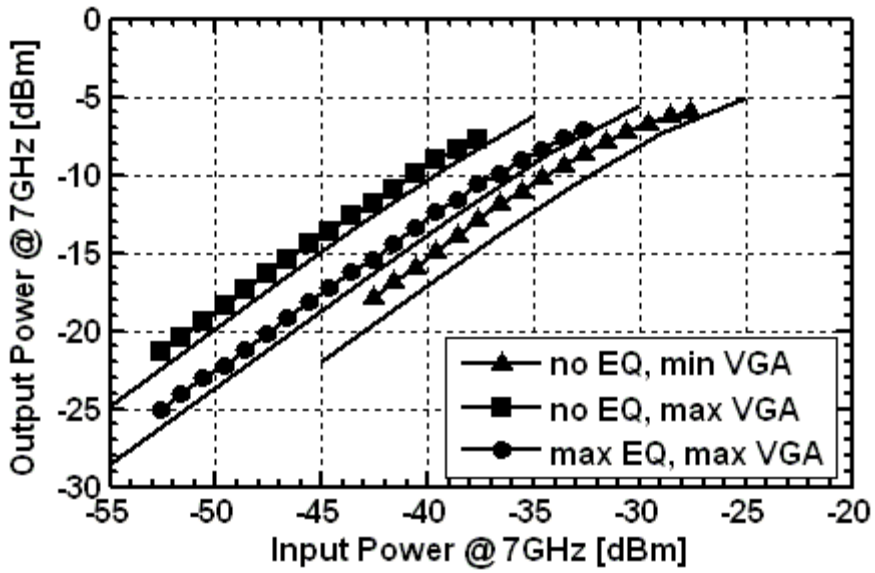
AFE: Simulated single-ended input and differential output eye diagrams: 15-m cable at 16.6 Gb/s (top), and 20 Gb/s (bottom).

Measurement Setup



Linearity Measurements





Measured (markers) and simulated (no markers) P_{1dB} at 1- and 7-GHz.

AFE Setting	P_{1dB} at 1-GHz [dBm]	P_{1dB} at 7-GHz [dBm]
no EQ, min gain	-30.8	-31.6
no EQ, max gain	-39.8	-38.6
max EQ, max gain	-36.8	-35.6