A Time-Interleaved $\Delta\Sigma$-DAC Architecture Clocked at the Nyquist Rate

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***Abstract*—This paper describes a delta–sigma ($\Delta\Sigma$) digital-to-analog converter (DAC) architecture that combines a polyphase decomposition of the interpolation filter and a time-interleaved error-feedback $\Delta\Sigma$ modulator. Noise-shaped oversampling is achieved while clocking the digital circuitry at the Nyquist rate. The design of a third-order 4-bit modulator with eight times oversampling using the architecture is presented. Results from a prototype current-DAC driven by a VHDL simulation of the digital design at 2.66 GHz show that 56-dB linearity is achievable in 90-nm CMOS within a 1-V supply over a 155-MHz signal bandwidth making the architecture suitable for emerging ultra-wide-band and 60-GHz radio applications.**

I. Introduction

STANDARDS for unlicensed wireless communication in both the 3.1–10.6-GHz [ultra-wide-band (UWB)] and 57–64-GHz bands are emerging. Both are likely to employ orthogonal frequency-division multiplexing (OFDM) schemes capable of transmitting data at roughly 500 Mb/s [1], [2]. Transmitter digital-to-analog converters (DACs) for these systems require a linearity of 25–30 dB for an UWB transmitter [2] and 50–60 dB for a 60-GHz transmitter [3] with hundreds of megahertz of bandwidth.

Currently, Nyquist-rate DACs are employed for broadband moderate linearity applications such as these. However, operating a DAC at the Nyquist rate necessitates an analog reconstruction filter with a brick-wall response. Hence, what are usually referred to as "Nyquist-rate" DACs are actually oversampled converters without noise shaping and with a low oversampling ratio to ease the reconstruction filter's requirements. In practice, these DACs are usually operated at $2\times$ to $3\times$ the Nyquist rate [4], [5].

A delta–sigma ($\Delta\Sigma$)-modulated DAC that provides noise shaping with a modest oversampling ratio ($\mathrm{OSR} = 8$ in this paper) offers several potential advantages. First, the requirements of the analog reconstruction filter are greatly reduced. Second, the required number of unit current elements is greatly reduced. These advantages come at the expense of added digital circuit complexity, a particularly attractive tradeoff in nanoscale CMOS processes. Hence, this paper describes a largely-digital architecture that pushes $\Delta\Sigma$-DACs to higher speeds in order to meet the needs of wireless transmitters for emerging broadband applications. The architecture efficiently integrates a parallel digital interpolation filter and $\Delta\Sigma$ modulator to increase the signal bandwidth. An example design is synthesized in 90-nm CMOS and tested using a prototype 4-bit current-DAC. Measurements indicate that the architecture can provide an SFDR of 56 to 54 dB over a 155-MHz bandwidth in 90-nm CMOS while operating completely within a 1-V supply.

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II. Background

Several approaches have been developed to increase the bandwidth of $\Delta\Sigma$-modulators using multiple parallel channels. These approaches can be categorized into three groups: frequency-division multiplexing (FDM) where each channel operates on a different frequency band (e.g., [6]); code-division multiplexing (CDM) where the channels are modulated by orthogonal spreading sequences (e.g., [7]); and time-division multiplexing, also known as time-interleaved modulation (TIM).

Both FDM and CDM are intended for ADC applications, and are not well suited to DACs. The TIM approach was first presented in [8] and applied to the design of an ADC in [9]. This approach demultiplexes the input and employs M modulators operating in parallel at $(1/M)$th the input clock rate. The parallel $\Delta\Sigma$ modulators are coupled, which makes the architecture sensitive to mismatches between paths [9]. In this paper, the TIM approach is applied to a DAC where the modulation is performed digitally so there is no mismatch.

In this paper, we show how a polyphase decomposition of the interpolation filter preceding the TIM $\Delta\Sigma$ modulator efficiently permits the entire digital system to operate at the Nyquist clock frequency f_N. Furthermore, we present a hardware demonstration of a TIM $\Delta\Sigma$ DAC with a multiGHz sampling frequency using a 4-bit current steering DAC implemented in 90-nm CMOS and operated from a 1-V supply.

III. Time-Interleaved DAC Architecture

A conventional $\Delta\Sigma$ DAC is shown in Fig. 1(a) comprising an interpolation filter, $\Delta\Sigma$ modulator, and a current-steering (CS) DAC. An OSR of 8 is assumed. Note that in the conventional architecture, large digital circuits are required to operate at $\mathrm{OSR}\cdot f_N$. Hence, for signal bandwidths of hundreds of megahertz most of the large digital circuitry would have to be carefully custom designed.

Instead, we propose to combine a polyphase decomposition of the interpolation filter with a TIM $\Delta\Sigma$ modulator architecture, as shown in Fig. 1(b). By choosing the time-interleaving factor for the modulator, M, to equal the OSR the entire digital front-end (with the exception of the M-to-1 demultiplexer) operates at the Nyquist clock frequency, f_N, instead of the oversampled clock frequency, $\mathrm{OSR}\cdot f_N$. This permits a conventional standard-cell digital design flow to achieve a bandwidths of hundreds of megahertz in 90-nm CMOS. Note that in either case the analog back-end operates at $\mathrm{OSR}\cdot f_N$.

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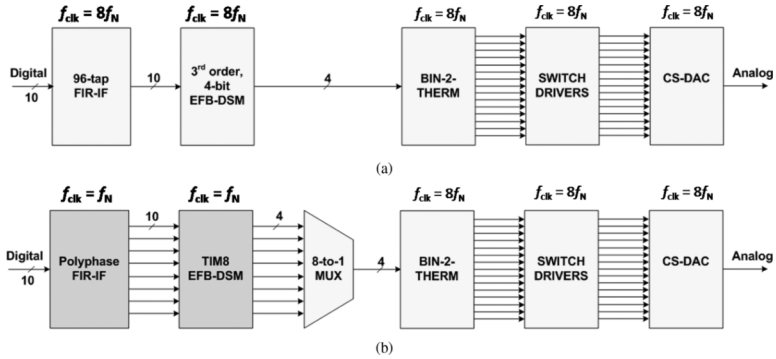

Fig. 1. (a) Conventional ΔΣ DAC architecture. (b) Proposed architecture with TIM interpolation filter and ΔΣ modulator.

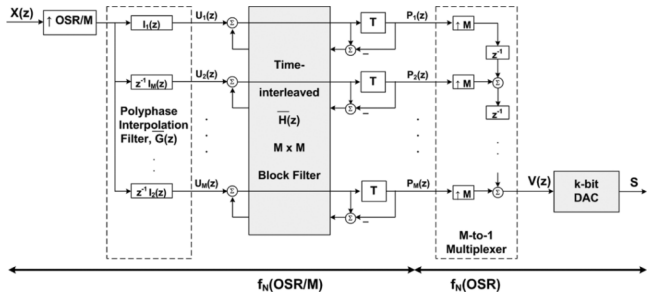

Fig. 2. Detail of interpolation filter and EFB TIM ΔΣ modulator.

IV. Digital Front-End Design

This section describes the design of a polyphase interpolation filter and a TIM ΔΣ modulator as shown in Fig. 2. An OSR of 8 and a signal bandwidth of 166 MHz requires the DAC to operate at an oversampled rate of 2.66 GHz, which we considered to be realistic for an analog current-DAC in 90-nm CMOS.

A. Interpolation Filter

The 10-bit input is sampled at the Nyquist rate. Interpolation gives rise to undesired images out of band which are attenuated both by the digital interpolation filter and an analog low-pass reconstruction filter following the DAC. In this design, a stopband attenuation of at least 25 dB is provided by the digital interpolation filter. This is achievable even with coarse quantization of the digital filter coefficients, as described below.

To meet these requirements, a 95th-order Kaiser-windowed FIR low-pass filter with a passband ripple of 0.2 dB and stopband attenuation of 40 dB was synthesized

$$G(z) = \sum_{k=0}^{l=95} z^{-k} g(k). \tag{1}$$

The 8-component polyphase decomposition of $G(z)$ is

$$G(z) = \sum_{k=0}^{7} z^{-k} I_k(z^8) \tag{2}$$

where the polyphase components are

$$I_k(z) = \sum_{i=0}^{\frac{l+1}{8}-1} g(8i+k) z^{-8i}, \qquad 0 \le k \le 7. \tag{3}$$

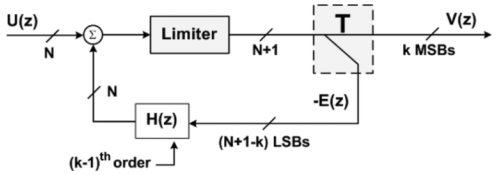

Fig. 3. Stable EFB ΔΣ modulator.

Note that a similar approach can be applied to the design of a cascade of lower-order interpolation filters to maintain a constant Nyquist-rate clock frequency.

The coefficients of $G(z)$, $g(k)$, were quantized using a canonic-signed-digit (CSD) representation. Coefficients with a normalized magnitude <0.1 were quantized using only one nonzero CSD; coefficients with a magnitude >0.1 were quantized using two nonzero CSDs. As a result, the implementation of each polyphase filter, I_k, requires the summation of at most 16 partial product terms. In spite of this coarse quantization, a passband ripple of 0.2 dB and a stopband attenuation of 28 dB is maintained.

B. ΔΣ Modulator

The only previous hardware demonstration of a TIM ΔΣ DAC is [10] where a field-programmable gate array (FPGA) implemented the trivial case of a 1-bit second-order modulator with time interleaving by $M = 2$. In this section, a 4-bit third-order modulator with time interleaving by $M = 8$ is described.

The error-feedback (EFB) ΔΣ modulator architecture shown in Fig. 3 is very efficient but sensitive to inaccuracies in the loop filter $H(z)$ [11]. Fortunately, when the ΔΣ modulator is implemented digitally, as in a DAC, such nonidealities do not arise.

An EFB modulator with a k-bit truncator and a $(k-1)$th-order loop filter can always be made stable [12]. The maximum signal-to-quantization noise ratio (SQNR) for such a modulator is [13]

$$\mathrm{SQNR}_{\max} = 10 \log \left[\frac{3(2k-1)2^{2k-1}}{\pi^{2k-2}} (\mathrm{OSR})^{2k-1} \right]. \tag{4}$$

Based on (4) with $\mathrm{OSR} = 8$, choosing $k = 4$ results in a third-order modulator with a maximum SQNR of 68 dB, providing some design margin beyond the target of 50 to 60 dB.

The noise transfer function (NTF) for the third-order EFB structure is

$$\mathrm{NTF}(z) = 1 - H(z). \tag{5}$$

The SQNR is maximized by placing the NTF zeros at dc and $\sqrt{(3/5)}f_N/2$

$$\mathrm{NTF}(z) = (1 - z^{-1})(1 - 1.908z^{-1} + z^{-2}). \tag{6}$$

As in the interpolation filter, the coefficients of the $\Delta\Sigma$ modulator are coarsely quantized to accommodate high-speed implementation. Each is approximated with at most 3 CSD terms resulting in the following quantized NTF

$$\mathrm{NTF}_{\mathrm{quan}}(z) = (1 - z^{-1})(1 - 1.875z^{-1} + z^{-2}). \tag{7}$$

The corresponding loop filter with quantized coefficients is

$$H(z) = 1 - \mathrm{NTF}_{\mathrm{quan}}(z) = az^{-1} - az^{-2} + z^{-3} \tag{8}$$

where $a = 2.875 = 2^1 + 2^0 - 2^{-3}$.

Next, the $\Delta\Sigma$ modulator is decomposed into the same number of parallel paths as the interpolation filter. Finally, an 8-component polyphase decomposition of $H(z)$ is formed and the polyphase components are assembled into the 8×8 block filter $\overline{H}(z)$ shown in Fig. 2

$$\overline{H}(z) = \begin{bmatrix} 0 & a & -a & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & a & -a & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & a & -a & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & a & -a & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & a & -a & 1 \\ 1/z & 0 & 0 & 0 & 0 & 0 & a & -a \\ -a/z & 1/z & 0 & 0 & 0 & 0 & 0 & a \\ a/z & -a/z & 1/z & 0 & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{9}$$

The ijth entry of $\overline{H}(z)$ is the transfer function from input j to output i of the block digital filter in Fig. 2. A block diagram of the resulting TIM is shown in Fig. 4.

C. Simulation Results

A register transfer level (RTL) description of the design was prepared in VHDL. Carry-select arithmetic was used throughout. Whenever several terms are added to form a y-bit result, all partial products are rounded to $y + 1$ bits *before* adding them. The final sum is then rounded down to y bits. If fewer bits are retained, the resulting nonlinearity would limit the DAC's SFDR.

Simulation results are shown in Fig. 5. The Matlab results show the system's performance with quantized filter coefficients, but infinite precision in all internal computations. The VHDL simulation results include the finite precision of all computations. Tones arise at images of the input frequency due to interpolation, and at harmonics of the input frequency due to rounding. Generally, a degradation of approximately 3 dB is observed due to the finite precision computations in the VHDL simulation compared with the full-precision Matlab simulation across the entire bandwidth.

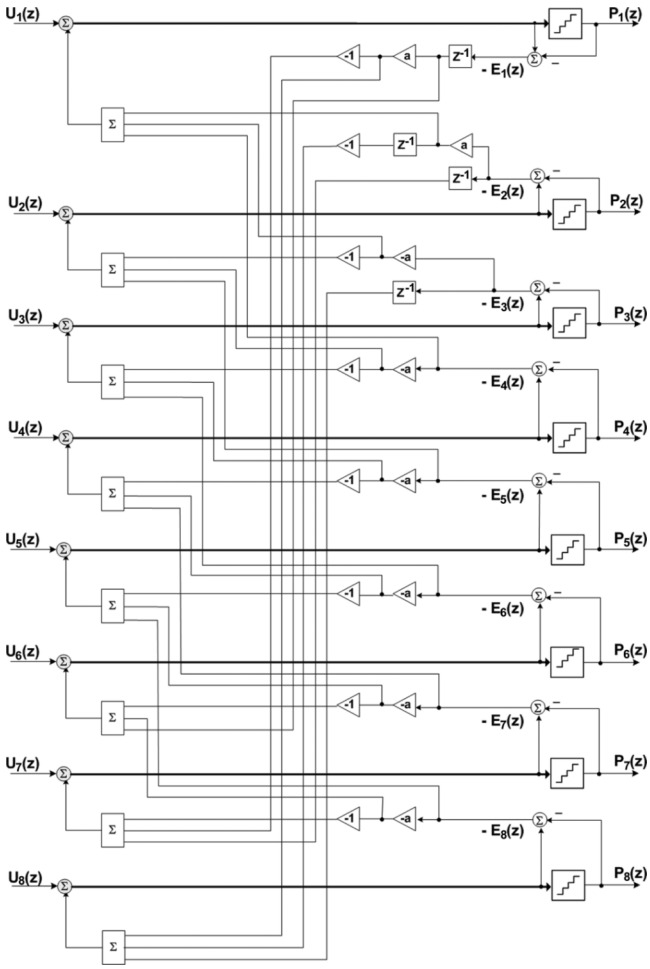

Fig. 4. Time-interleaved-by-8 third-order EFB $\Delta\Sigma$ modulator.

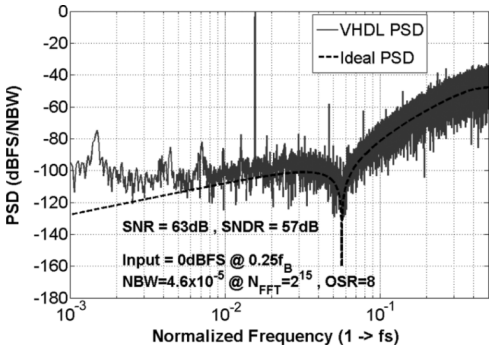

Fig. 5. Output spectrum for RTL simulations of the complete time-interleaved interpolation filter and $\Delta\Sigma$ modulator at 0-dBFS input amplitude and 0.25 f_B.

The design was synthesized in a 90-nm CMOS standard-cell library using Synopsys Design Analyzer, and then placed and routed using Cadence SOC First Encounter. Timing analysis indicates that the worst-case maximum clock frequency of the design is just above 500 MHz. Due to the $8\times$ time interleaving employed, this corresponds to an effective sampling rate of 4 GHz providing significant design margin beyond the test setup's maximum frequency of 2.66 GHz.

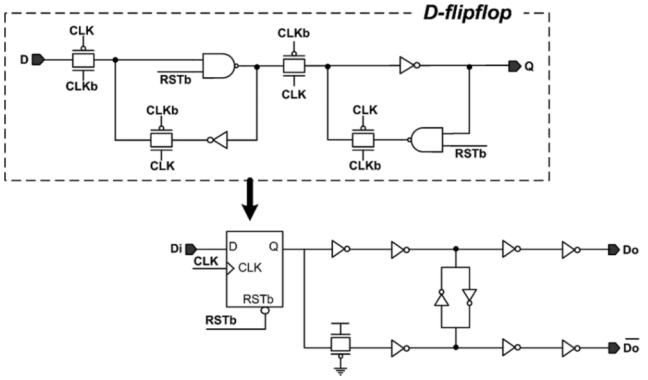

Fig. 6. Switch driver schematic.

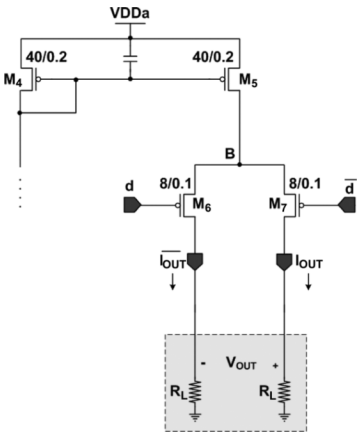

Fig. 7. Current-steering DAC cell shown with off-chip passive load.

V. Current-Steering DAC

To provide a hardware demonstration of the architecture, a 4-bit current-steering DAC was designed in 90-nm CMOS. Referring to Fig. 1(b), the prototype includes the 4-bit binary to 15-bit thermometer-code converter, switch drivers, and a 15-cell current steering DAC.

Fig. 6 is a schematic of the switch driver. A D-flip-flop is included to retime the thermometer codes at the full oversampled clock rate. Cross-coupled inverters are provided between the output data path (Do) and its complement $(\overline{Do})$ to align their transitions. An additional transmission gate is also included in the $\overline{Do}$ path to match its propagation delay to that of the Do path.

A schematic of the simple current-steering cell is shown in Fig. 7. Fifteen such cells are connected in parallel to external passive loads of 50 Ω per side. Within the 1-V supply, cascoding could not be accomodated. Non-minimum gate lengths were used for the current-source transistor, M_5, to increase its output resistance. Minimum gate-lengths were employed in the switching transistors M_6 and M_7, to maximize the cell's switching speed. Each current-steering cell supplies 400 μA.

A die photo of the prototype is shown in Fig. 8. The die area is approximately 400 μm × 500 μm excluding input and output pads (not shown).

VI. Measurement Results

The test setup used for measurements is shown in Fig. 9. A parallel bit-error-rate tester (ParBERT) was used as a high-speed digital pattern generator to drive the DAC input with the results

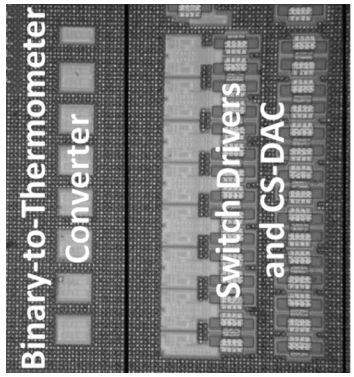

Fig. 8. Die photo of the prototype 4-bit current-DAC fabricated in 90-nm CMOS.

of VHDL simulations. Testing was performed at the ParBERT's maximum operating frequency of 2.66 GHz (166-MHz signal bandwidth).

Fig. 10 shows the SNDR and SFDR measured with two tones at −6 dBFS each. The SFDR varies from 56 to 54 dB corresponding to 8.9 bits of linearity up to $0.93f_B = 155$ MHz. The peak SNDR is 45 dB for 7.3 bits of accuracy with a 3-dB bandwidth of $0.93f_B = 155$ MHz. A missing-tone test, in which the input comprises many equally-spaced tones with one middle bin left empty, is particularly relevant for wireless applications employing OFDM. The measurements used 128 equally-spaced input bins as in an UWB standard [2] with the 64th bin left empty. The sub-channel spacing was 1.3 MHz for a total bandwidth of 166 MHz. Fig. 11 shows the measured missing-tone spectrum with a multitone power ratio of 38 dB.

Table I summarizes this work and compares it to other recently-reported CMOS DACs. The power is based on measurements for the DAC and simulations for the digital portion that have been correlated to measurements made on similar digital signal processor (DSP) blocks in the same 90-nm CMOS design library. The 8-to-1 multiplexer shown in Fig. 1(b) and an associated clock divider would be required for an integrated implementation of the complete DAC system; though not described here, these blocks were designed and their measured power and area consumption included in Table I. All SFDR measurements in Table I are for a two tone input centered around frequency f_{in}. The figure of merit (FOM) is for transmit DACs in multitone communication systems and includes SFDR, the output swing, V_{swing}, and power consumption P [4]

$$\mathrm{FOM} = \frac{V_{\mathrm{swing}} f_{\mathrm{in}}}{P} 10^{\mathrm{SFDR}/20}. \tag{10}$$

The highest reported bandwidth for a ΔΣ DAC in the prior art is [14] for which two-tone measurements are provided up to 26 MHz. This work targets lower SFDR applications resulting in a lower FOM, but has almost 6× greater analog bandwidth enabling its use in emerging broadband wireless applications. A state-of-the-art FOM with comparable bandwidth is achieved in [15], but measurements are made very near the Nyquist sampling rate implying impossible specs for the following reconstruction filter.

Reference [5] in Table I summarizes a DAC typical of modern broadband transmitters: no noise-shaping and low

Fig. 9. Experimental measurement setup.

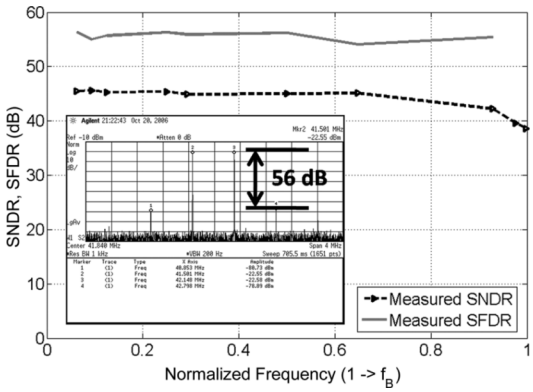

Fig. 10. Measured SNDR and SFDR versus input frequency at a sampling rate of $f_s = 2.67$ GHz. The inset shows a measured two-tone output spectrum around $0.25f_B = 42$ MHz.

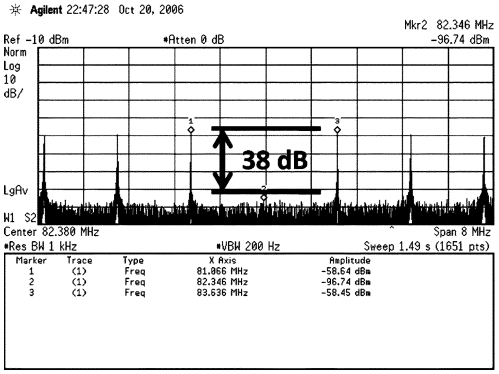

Fig. 11. Multitone test with 128 input bins over 166-MHz bandwidth.

TABLE I
SUMMARY AND COMPARISON TO PREVIOUSLY-REPORTED CMOS DACS WITH TWO-TONE SFDR MEASUREMENTS

	This Work	Clara, '05 [14]	Cao, '06 [5]	Deveugele, '04 [15]
f_{in} (MHz)	154	26	141	101
2-tone SFDR @ f_{in} (dB)	55.4	75	57	67
Swing, V_{swing} ($V_{pp,diff}$)	0.6	1.54	0.27	0.5
Power, P (mW)	139 (99)[1]	62	49	22
Area (mm^2)	1.00 (0.84)[1]	—	0.36	0.35
FOM ($\cdot 10^{12}$ V·Hz/W)	0.39 (0.55)[1]	3.63	0.55	5.14

[1]—excluding interpolation filter

OSR. It achieves a FOM similar to this work in the same technology (excluding the interpolation filter which was not included in [5]). The converter in [5] is smaller in area (0.36 versus 0.84 mm^2), but the area penalty is negated if both designs are scaled to 45 nm (reducing the area of the digital portions by 75%) and the output stage of this design is reduced to provide the same swing as [5]. Furthermore, the higher oversampling ratio in this work $(\mathrm{OSR} = 8)$ offers relaxed specifications on the analog reconstruction filter and requires far fewer unit-current elements than [5]. Hence, the architecture described here is likely to be preferred in systems where minimal analog circuit complexity is desired, offering reduced design and verification time with improved portability and robustness to mismatch.

VII. CONCLUSION

The TIM $\Delta\Sigma$ DAC architecture demonstrated here achieves an analog bandwidth almost $6\times$ greater than the fastest previously reported $\Delta\Sigma$ DAC [14]. This was enabled by combining a polyphase interpolation filter with a TIM. The resulting FOM is comparable to a state-of-the-art converter designed to operate with low OSR and no noise-shaping, typical of DACs in modern broadband transmitters. The architecture has potential advantages for broadband transmitters in nanoscale CMOS, particularly when integrated alongside a digital interpolation filter and analog reconstruction filter.

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