A Multi-Lane Optical Receiver with Integrated Photodiodes in 90nm Standard CMOS

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Abstract: A multi-lane optical receiver with integrated photodiodes is fabricated in a 90nm CMOS process, the first in a standard CMOS node below 100nm. It has a sensitivity of -3.7dBm at a 3.125Gbps data rate and consumes 46.3mW per lane from a 1.2V supply.

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1. Introduction

Fiber-optic interconnects for long-distance data communication are implemented on multiple die, fabricated using disparate technologies, such as GaAs and SiGe [1]. These solutions are relatively cost-insensitive due to the large number of users per channel. For short-reach optical connections such as Local-Area Network (LAN), board-to-board or chip-to-chip interconnects, the system cost must be low. A receiver implemented entirely in a standard Complementary Metal-Oxide-Semiconductor (CMOS) process offers a very low manufacturing cost. Moreover, it is a single-chip solution, which presents further advantages, such as eliminating ground-bounce issues, Electrostatic Discharge (ESD) problems, and bond-wires [2].

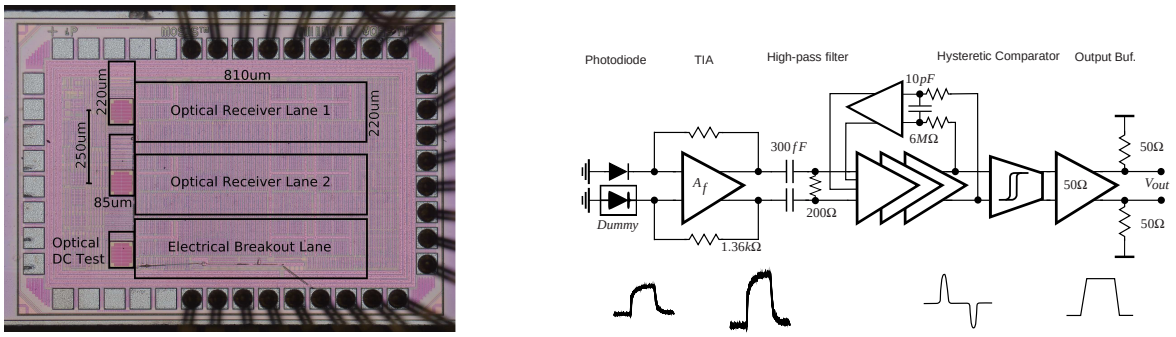
The problem with optical receivers in CMOS technology is the low speed of silicon photodiodes. The photodiode is built as a reverse bias PN junction, which creates a depletion region that is used to collect the electron-hole pairs created when incident photons are absorbed. However, the penetration depth of 850nm light is far greater than the width of the depletion region, resulting in carriers generated deep in the silicon that must diffuse to the depletion layer. This limits the bit-rate to tens of Mbps [2]. Furthermore, smaller technology nodes operate at lower voltages with higher doping levels, resulting in a smaller depletion region, which leads to smaller photodiode intrinsic bandwidth, and photodiode responsivity [1, 3]. However, it is desirable to implement the optical receivers in nanoscale technologies where they can be integrated alongside large amounts of digital logic.

Several methods were investigated to remove slow diffusing current in order to increase the speed of the photodiode in CMOS. Recent research on standard CMOS optical receivers with no process modification or change to the nominal supply voltage has revolved around the use of Spatially Modulated Light (SML) photodetectors [3] and equalization [2]. Unfortunately, SML photodetectors have a lower responsivity than a standard photodiode [1]. A popular approach is to combine an SML photodetector with equalization, as seen in [3–5].

2. CMOS Optical Receiver

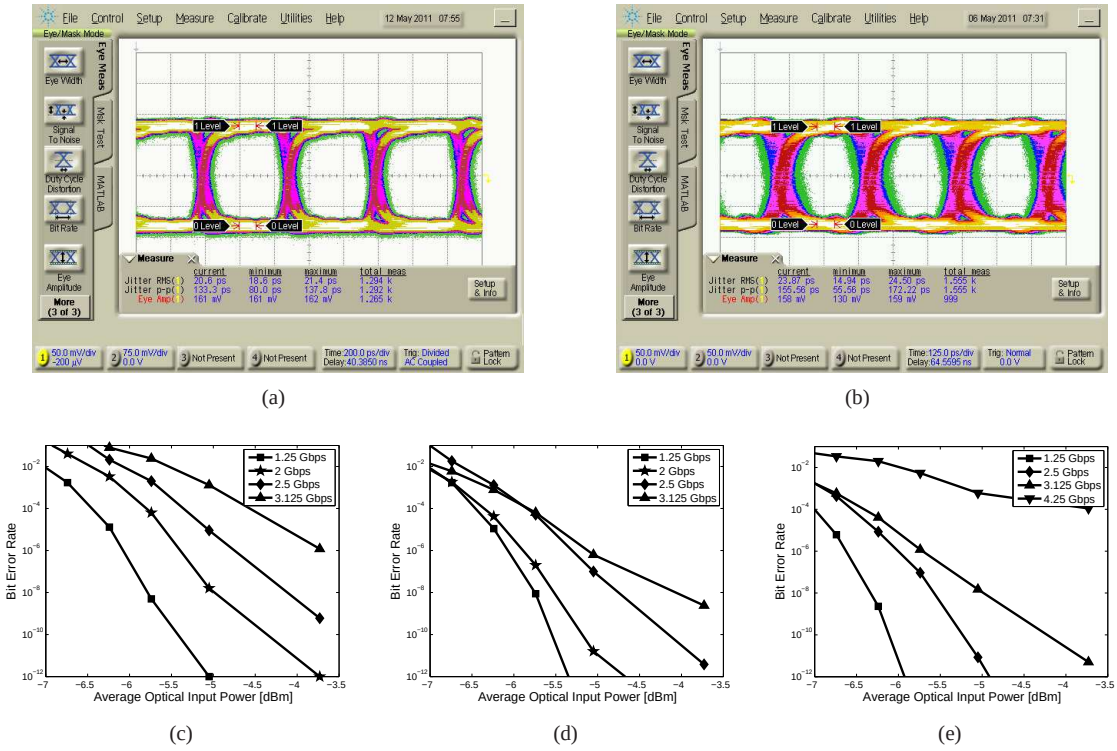
Fig. 1(a) shows a photo of the die. The dimensions of the photodiodes are $72\mu m \times 78\mu m$ and they are spaced $250\mu m$ apart to facilitate coupling to multimode fiber ribbons. Recent work on high-speed photodetection in standard CMOS has focused on the use of SML detectors [3] in which over 50% of the active area is covered by metalization, reducing responsivity. In this work, only approximately 20% of the photodiode's active area is covered by metalization. The measured DC responsivity with 850nm light is 0.141A/W, compared with only 0.05A/W for typical SML detectors [3]. Unfortunately, the intrinsic bandwidth of such structures is typically limited to a few 10's of MHz [2].

Recent research has also used an analog equalizer to extend the bandwidth of the photodiode. When combined with a SML detector, modest equalization is sufficient to permit multi-Gb/s data rates [3]. In this work, because SML is forgone, the bandwidth limitations are more severe and linear equalization would be much more difficult. Other works have also used high non-standard supply voltages to improve CMOS photodetector bandwidth [4]. In this work, a different receiver architecture is used that is compatible with a 1.2V nominal CMOS supply voltage and does not require an SML detector. The block diagram of the receiver is shown in Fig. 1(b). A dummy photodiode provides equal capacitance at both inputs of the differential transimpedance amplifier (TIA). The AC coupling serves two purposes. First, since the input to the TIA is single-ended, the AC coupling removes DC offset in the differential signal.



(a) (b)

Fig. 1. (a) Photo of the die. (b) Receiver block diagram.



(a) (b)

(c) (d) (e)

Fig. 2. Measurement results (a) Eye diagrams of an optical input with an average input power of -3.7dBm and an extinction ratio of 9dB and a supply of 1.2V and PRBS31 pattern at 2Gbps (b) PRBS7 pattern at 3.125Gbps. BER vs. average optical input for a constant 9dBm extinction ratio (c) 1.2V supply and PRBS31 input (d) 1.3V supply and PRBS31 input (e) 1.2V supply and PRBS7 input.

Second, making the corner frequency of the AC coupling 5GHz removes all low-frequency content, which is largely due to the slow-moving diffusion current from the photodiode response, resulting in narrow electrical pulses whenever there are transitions in the received data with minimal inter-symbol interference (ISI). The pulsed signals are then amplified up to 150mV and a hysteretic comparator is used to convert the pulsed waveforms back into non-return-to-zero (NRZ) data.

The amplifier preceding the hysteretic comparator will introduce more DC offset which can overwhelm the small input signal. To solve this problem, offset compensation is included in this stage. An output buffer is included to drive

a 50Ω load per side with $150mV_{pp}$ per side swing.

3. Measurement Results

The chip was built in TSMC's 90nm CMOS process, a manufacturing process that is unmodified, with no additional processing steps - the exact same process used for regular ASICs. It has 1 polysilicon layer, and 9 metal layers. The supply voltage for this design is 1.2V. The die photo is shown in Fig. 1(a). The photodiodes are arranged with a $250\mu m$ centre-to-centre pitch to facilitate standard optoelectronic packaging. The Quad Flat No leads (QFN) package was mounted on a custom Printed Circuit Board (PCB) for optical testing. Optical inputs were applied at 850nm via a multimode optical probe manually aligned over the photodiodes with micropositioners.

The measured output eye diagram with an average input power of -3.7dBm and an extinction ratio of 9dB is shown for various data rates and input patterns in Fig. 2(a,b). Fig. 2(c-e) shows a plot of Bit Error Rate (BER) against average input power. This plot indicates that the input optical sensitivity is -3.7dBm for a 2Gbps Pseudo-Random Bit Sequence (PRBS31) input with a 1.2V supply, and improves to -4.7dBm with a 1.3V supply. Furthermore, the sensitivity improves further to -4.9dBm at 2.5Gbps with a PRBS7 input, meaning that higher data rates are achievable through the use of data encoding schemes. A BER of 5×10^{-12} is acheived at 3.125Gbps with a PRBS7 pattern and -3.7dBm input power.

4. Conclusion

Reported here is the first multi-Gbps optical receiver fully integrated (including the photodiodes) in a standard CMOS process node below 100nm. Arraged on a $250\mu m$ pitch, each lane includes a $75\mu m$-diameter photodiode and consumes 46.3mW, and an additional 19.6mW for the output buffer, from a single 1.2V supply. The measurement results of the optical receiver are compared to the most recently published optical receivers in Table 1.

Table 1. Comparison of most recently published optical receivers with integrated photoreceivers in standard CMOS. All values are reported for a PRBS31 input pattern except values in brackets which have a PRBS7 input pattern.

	[3]	[4]	[5]	This work	This work
Technology	$0.18\mu m$	$0.13\mu m$	$0.13\mu m$	90nm	
Area	$0.72mm^2$	$0.1mm^2$	$1.88mm^2$	$0.197mm^2$	
Supply Voltage	3.3V / 1.8V	1.5V	1.2V / -1V	1.2V	1.3V
Power Dissipation	168mW	47mW	58.5mW	46.3mW	55.2mW
Data Rate	5Gbps	8.5Gbps	[5.5Gbps]	2Gbps [3.125Gbps]	2Gbps
Sensitivity	-3dBm	-3.2dBm	[-3.4dBm]	-3.7dBm [-3.7dBm]	-4.7dBm
Responsivity	0.05A/W	0.05A/W	-	0.141A/W	0.236A/W

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