A Digital Phase-Locked Loop with Calibrated Coarse and Stochastic Fine TDC

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Abstract—A coarse-fine time-to-digital converter (TDC) is presented with a calibrated course stage followed by a stochastic fine stage. On power-up, calibration algorithm based on a code density test is used to minimize nonlinearities in the coarse TDC. By using a balanced mean method, the number of registers required for calibration algorithm is a reduced by 30%. Based upon the coarse TDC resuls, the appropriate clock signals are multiplexed into a stochastic fine TDC. The TDC is incorporated into a 1.9 – 2.54 GHz digital phase locked loop (DPLL) in 0.13 μm CMOS. The DPLL consumes a total of 15.2 mW of which 4.4 mW are consumed in the TDC. Measurements show an in-band phase noise of -107 dBc/Hz which is equivalent to 4 ps TDC resolution, approximately an order of magnitude better than an inverter delay in this process technology. The integrated random jitter is 213 fs. The calibration reduces worst-case spurs by 16 dB.

I. INTRODUCTION

Modern wireless and wireline communication standards place challenging demands on the phase noise, spurious tones, jitter accumulation, and modulation bandwidth of phase-locked-loops (PLLs) [1]. Research on digital PLL (DPLL) has been active in this area due to aggressive CMOS scaling and high gate leakage in nanometer CMOS processes. DPLLs have demonstrated they can meet the challenging requirements of modern standards, and they can be advantageous compared with conventional analog PLLs in terms of area, testability, and programmability [2].

In a DPLL, the feedback divider may be replaced with an integer counter and a time-to-digital-converter (TDC) works as a fractional counter. Frequency and phase detection is implemented by a digital subtractor. This DPLL architecture is shown in Figure 1.

The DPLL loop dynamics filter out noise contribution of various noise sources with different responses depending upon their location within the loop. TDC quantization noise and reference jitter are low-pass filtered and are therefore dominant within the DPLL loop bandwidth while the digitally control oscillator (DCO) noise is high-pass filtered and dominant at high frequencies as shown in Figure 2.

Wide bandwidth PLLs are of great interest for wireless and wireline applications, especially for frequency hopping and multi-standard applications [3]. For wide bandwidth DPLLs, TDC resolution must be fine enough to limit the resulting in-band quantization noise.

Different techniques has been used to improve TDS resolution including the gated ring-oscillator (GRO) [4], vernier ring structures [1], and a coarse-fine architecture based on time
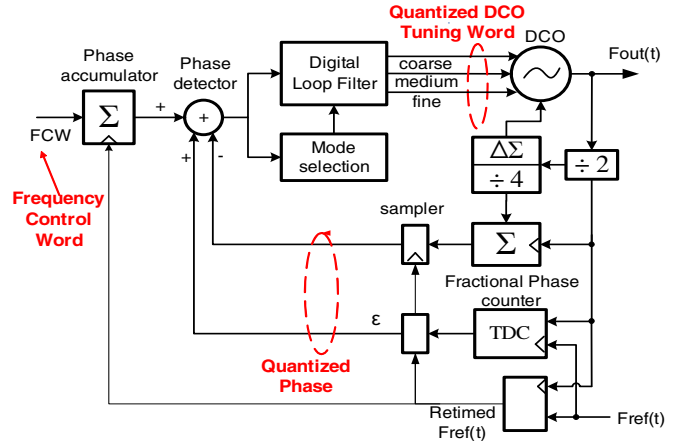

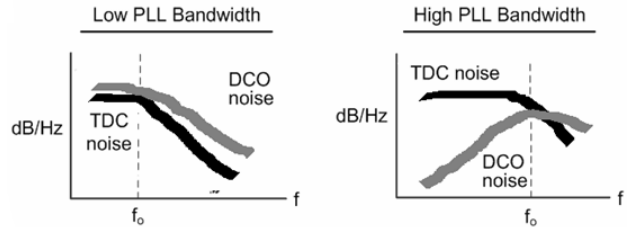Fig. 1. A digital PLL architecture for fractional frequency synthesis.

Fig. 2. Phase noise contributions for low- and high-bandwidth PLLs.

amplifiers [5]. With the GRO, TDC quantization noise is 1st-order shaped; multi-phase coupled oscillators are required to reduce the delay, consuming high power. In a vernier delay line, TDC resolution is determined by the delay difference between two inverters. The main drawbacks of a vernier TDC are inverter mismatch which limits its accuracy, and large area which limits the dynamic range and increases power consumption. The coarse-fine TDC based on time-amplification use a coarse TDC then amplify the residual time quantization noise and apply it to another coarse TDC. This architecture improves TDC resolution but requires high power consumption in the time amplifier and complex calibration techniques.

In this paper, we present a fractional DPLL that incorporates a novel low-power coarse-fine TDC to achieve low in-band phase noise operation. The paper is structured as follows. In Section II, an overview of the proposed coarse-fine TDC is given. In Section III, we discuss TDC nonlinearities and
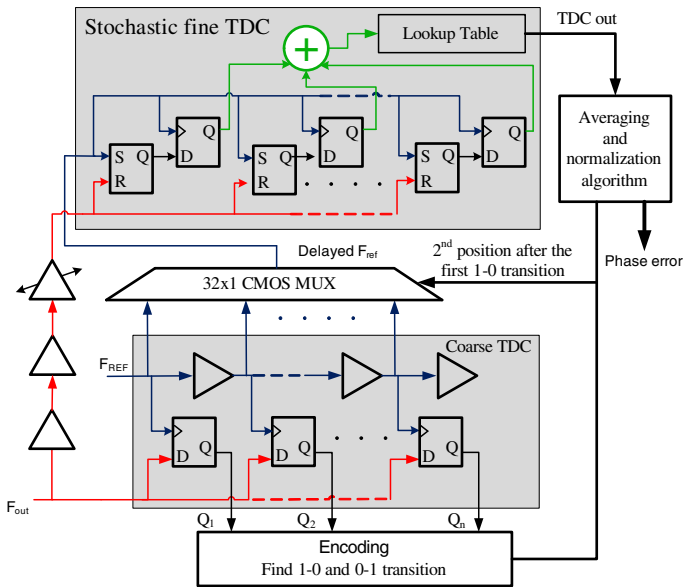
Fig. 3. The coarse-fine TDC architecture.

Fig. 4. The schematic and operation of the stochastic fine TDC.

their effect on phase noise along with a low-area calibration algorithm to alleviate these problems. Finally, measurement results of the DPLL prototype are shown Section IV.

II. FINE-COARSE TDC

The TDC's noise contribution can be minimized by improving the TDC timing resolution and/or increasing the sampling rate of the TDC (i.e. increasing the reference frequency). As demonstrated in [2], reducing TDC resolution by factor of 10 reduces in-band phase noise by 20 dBc/Hz. For example, with a 20 MHz reference clock, 2.5 GHz output clock and 40 ps TDC resolution, the in-band phase noise contribution is around -87 dBc/Hz. If the TDC resolution reduced to 4 ps, the phase noise will drop to -107 dBc/Hz.

We propose a coarse-fine TDC without the power-hungry time amplifier in order to achieve 4 ps TDC resolution in a 0.13 μm technology. As shown in Figure 3, the proposed TDC architecture uses a coarse-resolution TDC to select a delayed reference clock for further comparison with the output clock into a fine-resolution TDC. It uses the stochastic behavior of latch offsets to provide a resolution much better than the technology's inverter delay.

A. Coarse TDC

The coarse TDC generates 32 delayed versions of the low-frequency reference clock by passing it through chain of buffers and then sampling the high-frequency output clock. The buffers are realized as pseudo-differential inverters to reduce the raw TDC resolution and to avoid mismatches between the rising and falling edge transitions. The sampling flip-flops are sense-amplifier flip flops that have a narrow symmetric metastability window which is important when phase error is very small [2].

The 32 outputs of the coarse TDC are a pesudo-thermal code. A binary encoder is needed to detect the position of
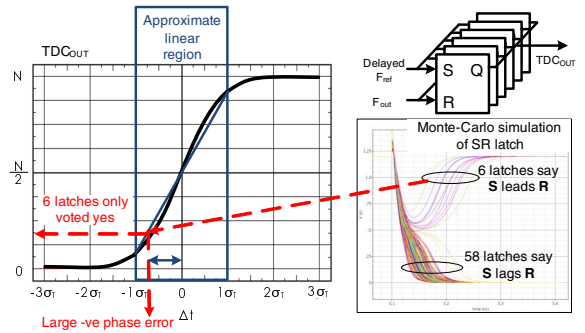
the 1→0 and 0→1 transitions in order to estimate the output clock's period (frequency). The encoder output is also needed to select one of the delayed versions of the reference clock for further comparison with the output clock using the fine TDC. The encoder introduces a delay which makes it impossible to tap the output of the first buffer after where the 1-0 transition occurs, since by then the clock edge has propogated further. To solve this problem, the second buffer after the 1-0 edge transition is tapped into the fine-TDC. Moreover, the DCO clock is also delayed by two buffers and a multiplexer to mimic the extra delay experienced by the tapped version of the reference clock, before comparison by the fine TDC.

B. Fine TDC

Stochastic TDCs have been used for sub-ps measurements in nuclear applications [6]. The stochastic TDC is composed of N equal arbiters evaluating in parallel the phase relation between two incoming signals. Ideally, an arbiter follows a step function with the threshold at $\Delta t = 0$. However, due to device mismatch, each arbiter exhibits a random offset, T_{OFF}, in its threshold. The offset T_{OFF} approximates a Gaussian random variable with standard deviation σ_T. The average stochastic TDC output can be estimated based on the cumulative distribution function (CDF) which follows the error function [6].

The error function has an approximately linear region around $[-\sigma_T, \sigma_T]$, where σ_T is the standard deviation of the offset voltage. The stochastic TDC resolution can be estimated as the inverse of the slope of the CDF function around the mean: $\overline{LSB} = \frac{\sqrt{(2\pi) * \sigma_T}}{N}$ [6]. The arbiters within the stochastic TDC have an offset that exhibits a standard deviation of 32 ps, according to monte-carlo simulations. This enables the fine TDC to have a 64-ps approximately linear region which is around two times the coarse TDC resolution. A wide linear range is desirable since any systematic mismatch (for example as caused by layout mismatch) will shift the CDF to left or right and reduce the useful linear range and the ability of the stochastic TDC to resolve time difference.

To achieve 2 ps average resolution, at least 40 arbiters are required but we used 64 due to the statistical nature of the TDC's average resolution. The arbiters have been implemented as set-reset latches based on cross-coupled NAND gates. The
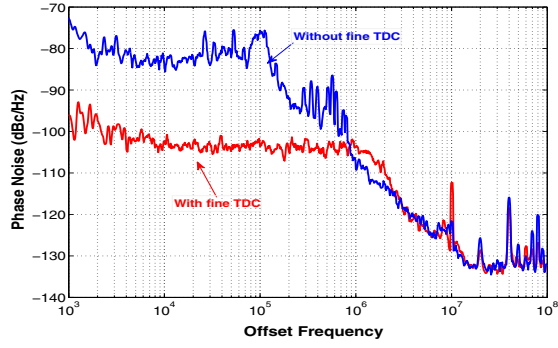
Fig. 5. Phase noise measurement using a HP8565C analyzer with and without a fine TDC.
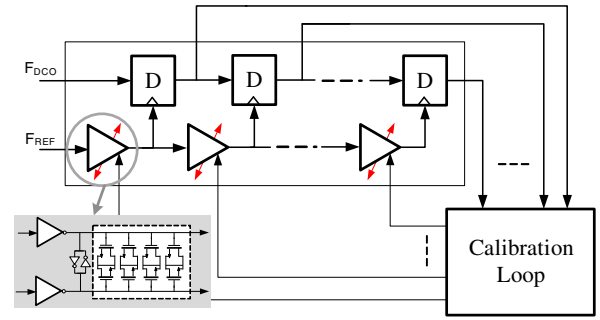

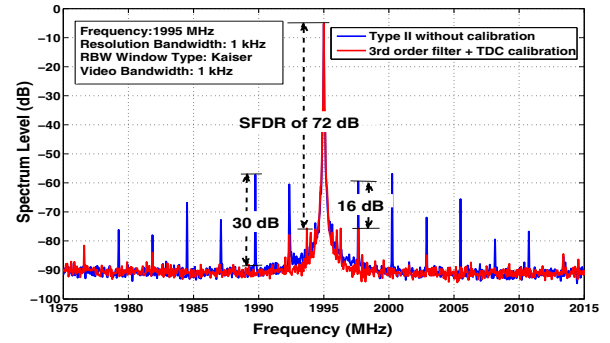Fig. 6. On-chip low-area calibration algorithm of the coarse TDC based on a code density test.

Fig. 7. Reduction of the spurs after TDC calibration and high-order filtering (measured using Tektronix RSA 6114A real-time spectrum analyzer).

output of these arbiters are sampled on the rising edge of the delayed reference clock.

The power consumption of the proposed coarse-fine TDC is 4.4 mW from 1.2 V source. This is quite low compared to other published fine TDC architecture. For example, the coarse-fine TDC based on time amplifier in [5] consumes 70 mW and the GRO in [4] consumes 2.2 - 21 mW depending upon the phase error.

Figure 5 shows phase noise measurements at a 2 GHz DPLL output and 20 MHz reference clock, using a HP8565C spectrum analyzer and KE5FX tool, with and without the fine TDC. The in-band noise is not less than -83 dBc/Hz when fine TDC is disabled which is equivalent to approximately 40 ps TDC resolution, as expected. Once the fine TDC is enabled, the in-band phase noise drops to -104 dBc/Hz which is equivalent to 4 ps resolution. However, in this measurement the in-band noise is limited by the reference clock noise. The loop bandwidth is approximately 1.6 MHz while the integrated random jitter is 213 fs (0.16 degree).

III. TDC Calibration

The PLL in-band phase noise and spurious content are highly sensitive to TDC non-idealities. This includes differential non-linearity (DNL) caused by mismatch between delay elements which is critical when the delayed reference clock is very close to the sampling edge. TDC quantization error causes the phase error to diverge from the ideal value of zero during the steady state operation. This will appear as higher than expected phase noise within the loop bandwidth or as spurious tones when the phase error repeats periodically. Hence, calibration techniques are needed. Furthermore, calibration of the coarse-TDC is crucial to ensure that the residual quantization error applied to the fine-TDC is within an acceptable range.

To enable calibration of the coarse TDC, each delay element includes a 4-bit binary-weighted capacitor bank. A code-density test is employed to measure the DNL of the delay elements. The capacitor bank allows -7 to +8 ps calibration for each delay element around the nominal midpoint of 40ps.

The code-density test needs a large number of hits to achieve accuracy. Accordingly, each delay element needs a wide register to store the number of hits during calibration. In

this work, a balanced mean rather than an absolute mean is used to store the accumulated number of the hits. At the end of balanced mean calibration, registers store the DNL of each TDC bin. To achieve a DNL of 2% with 99% confidence, a 16-bit register is used for each coarse TDC bin rather than 23-bit register which saves 224 registers in total.

Figure 7 shows spectrum measurements where spurs have been reduced from -54 dB to -70 dB at 2.65 MHz offset from the 1.995 GHz carrier by the calibration. Spurs at larger offsets were reduced by 30 dB thanks to the application of a 3rd-order loop filter.

IV. Measurement Results

A chip was fabricated in 0.13 μm CMOS technology from IBM and mounted on a circuit board for testing. The DCO is an LC-oscillator with a digitally-controlled capacitance. A $\Delta\Sigma$ modulator is used to shape the quantization noise of the DCO to high offset frequencies and achieve fine frequency control.

The capacitor DAC within the DCO is composed of three capacitor banks which can switch on/off to increase/decrease the capacitive load. Based on an open loop test, the coarse DCO bank gain, K_{vco}, equals 8.125 MHz/code on average, the medium DCO bank gain is around 650 kHz/code on average, and the fine DCO bank gain is 32kHz/code on average. The DPLL can lock to any frequency between 1.9 - 2.54 GHz from a nominal reference of 20 MHz.

The output clock of the DCO is divided by two using a CML circuit. The half-rate clock is fed to a CMOS divider
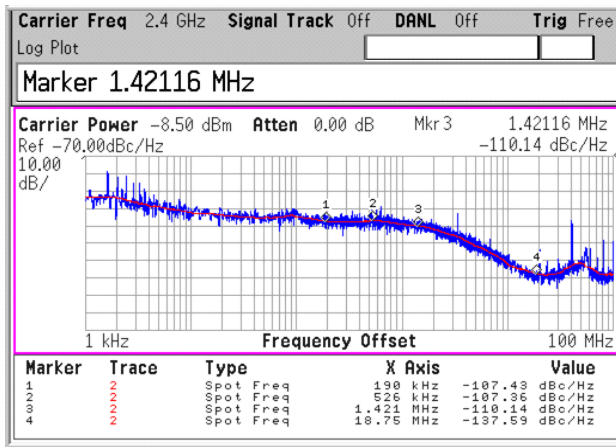
Fig. 8. Phase noise spectrum captured by an Agilent E4448A spectrum analyzer. The loop BW is 1.42 MHz.

Fig. 9. Histogram of TIE jitter captured by DSA70404B Real-Time Scope.

Fig. 10. Die photo of the DPLL (active area is 0.36 mm^2).

and a counter to clock the $\Delta\Sigma$ modulator and to estimate the clock frequency. Aside from the CML divide-by-2, all circuits are made from the standard cell library using standard digital synthesis tools.

A phase noise measurement, using an Agilent E4448A spectrum analyzer, with the coarse-TDC calibrated and fine TDC activated is shown in Figure 8 for a 2.4-GHz output frequency. The in-band phase noise is -107 dBc/Hz. The phase noise at 2 MHz offset is -114 dBc/Hz while it is -137 dBc/Hz at 19 MHz offset. The Table below compares the proposed DPLL with state-of-art published works. The DCO and CML divide-by-two consume 7.8 mW, the coarse TDC consumes 1.4 mW, the fine TDC consumes 3 mW, and the digital logic consumes 3 mW. The active area of the proposed DPLL is 0.43 μm^2 including the calibration algorithm and 0.36 μm^2 without the calibration algorithm. A die photo of the fabricated prototype is show in Figure 10.

	[7]	[8]	[9]	[10]	This
Reference (MHz)	26	40	N/A	35	20
Carrier (GHz)	3.6	2.5	3.96	3.5	2.4
Noise (dBc/Hz)	-95	-105	-96	-101	-107
PLL BW (MHz)	0.15	0.5	0.3	3	1.42
In-band spurs (dBc)	-75	-75	-68	-58	-72
Power (mW)	60	9.7	9.6	9	15.2
Process (nm)	130	90	90	65	130

Time-interval-error (TIE) jitter was also measured using Tektronix DSA70404B real-rime scope. Figure 9 shows the histogram of the TIE jitter on the rising edge of DPLL output clock. The TIE rms jitter is 888 fs (including random and deterministic), the TIE peak-to-peak jitter is 6.35 ps, and the period jitter is 3.27 ps.

V. CONCLUSION

A DPLL with a novel calibrated coarse-fine TDC was presented that is suitable for modern wireless and wireline standards. The proposed DPLL achieves -107 dBc/Hz in-band noise level which 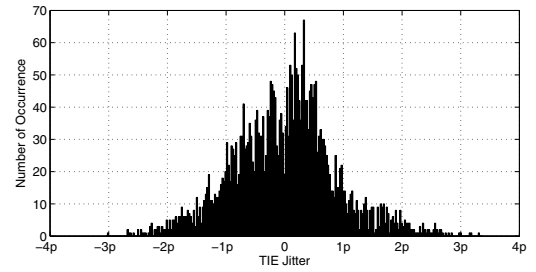is equivalent to 4 ps TDC resolution. The DPLL can lock to any frequency from 1.9 - 2.54 GHZ using 20 MHz reference while the loop bandwidth is around 1.42 MHz. The entire DPLL consumes 15.2 mW from a 1.2 V supply in IBM's 0.13 μm bulk CMOS technology.

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