A 3-Tap FIR Filter With Cascaded Distributed Tap Amplifiers for Equalization Up to 40 Gb/s in 0.18-μm CMOS

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***Abstract*—This paper describes a 3-tap finite impulse response programmable analog filter in 0.18-μm CMOS. The filter is intended for polarization-mode dispersion compensation in 40-Gb/s long-haul single-mode optical fiber links. A novel filter topology is employed, whereby each tap gain comprises a cascade of two distributed amplifiers with adjustable gain. The same lumped *LC* ladders that provide the 25-ps tap delays also serve as artificial transmission lines for the distributed tap amplifiers. The prototype is 1 mm$\times$ 1 mm (900 μm $\times$ 600 μm active area) and consumes up to 70 mW from a 1.8-V supply depending on the tap gains. Linear equalization is demonstrated over a channel with 17 dB of loss at 20 GHz. A 50 mV per side eye amplitude with 14 dB signal-to-noise ratio is demonstrated at 30 Gb/s, and a modest 39 mV per side eye amplitude with 10 dB signal-to-noise ratio is achieved at 40 Gb/s.**

***Index Terms*—CMOS, distributed amplifier, equalization, polarization-mode dispersion (PMD), traveling wave filter, 40 Gb/s.**

I. Introduction

FINITE impulse response (FIR) filters with programmable tap gains are essential building blocks in many communication integrated circuits. They are used on their own as linear equalizers or as part of decision-feedback equalizers to compensate for intersymbol interference (ISI) in optical fiber and chip-to-chip communication applications. This paper describes a novel topology to increase the bandwidth of analog programmable FIR filters. Each tap amplifier is implemented as a cascade of two distributed amplifiers. The same passive *LC* delay line is used for the tap spacing and to distribute the tap amplifiers' input and output capacitances. The new architecture, referred to as a "folded-cascade traveling wave filter," enables equalization at 40 Gb/s in a 0.18-μm CMOS process that has a maximum f_t of only 45 GHz. The filter is 4$\times$ faster than previously reported equalizers in similar technologies [1], [2].

Previous analog FIR filter implementations at data rates of 10+ Gb/s generally operate in continuous-time using a traveling wave filter (TWF) architecture. For instance, at data rates of 40–49 Gb/s, programmable TWFs have been reported in InP/InGaAs [3] and SiGe [4] technologies consuming several hundred milliwatts. At 10 Gb/s, TWFs have been implemented with much lower power consumption including a 7-tap (50-ps tap spacing) design in 0.18-μm SiGe BiCMOS consuming 40 mW [5] and a 4-tap equalizer with 33-ps tap spacing in 0.18-μm CMOS consuming only 7.3 mW [1]. In [6], a 30-Gb/s equalizer in 90-nm CMOS was presented, making use of a crossover TWF topology to extend the bandwidth of each tap in the FIR filter by a factor of two. Other circuit blocks for 40-Gb/s systems have been demonstrated in 0.18-μm CMOS [7]–[9], but no equalizers for these applications have been demonstrated in any similar technology.

The remainder of this paper is organized as follows. In Section II, the need for a 3-tap linear equalizer is motivated by examining polarization-mode dispersion in single-mode optical fiber communication links. Section III describes the evolution of the folded-cascade TWF from a traditional TWF. Section IV describes an integrated implementation of the folded-cascade TWF. Section V summarizes prototype test results.

II. Polarization-Mode Dispersion Compensation

At data rates of 40 Gb/s, ISI limits the reach of long-haul single-mode optical fiber (SMF) links. An integrated circuit equalizer may be used to perform dispersion compensation enabling robust links. In this section, specifications are developed for an equalizer capable of eliminating dispersion as a length limitation in 40-Gb/s SMF links.

Both chromatic and polarization-mode dispersion can cause ISI in SMF. Chromatic dispersion is the result of the wavelength-dependency of the refractive index of the fiber. It can be compensated for using relatively inexpensive optical components (e.g., [10]), and therefore is not considered further here. Polarization-mode dispersion (PMD) results from birefringence, a difference in refractive index experienced by light in two orthogonal polarization modes. Ellipticity of a fiber cross section due to asymmetric stresses applied during or after manufacturing cause birefringence and, hence, PMD. Electronic PMD compensation is more attractive than optical compensation because it allows greater integration with existing circuitry, leading to more compact, less expensive solutions. This is especially true for wavelength-division multiplexed systems, in which every channel needs PMD compensation [11]. Also, because PMD fluctuates with changes in temperature and environment, PMD compensators must be able to adapt to varying channel conditions within milliseconds [12]. Fast and accurate adaptation is more easily performed with electronic dispersion compensators. This work focuses on an electronic compensator for PMD.

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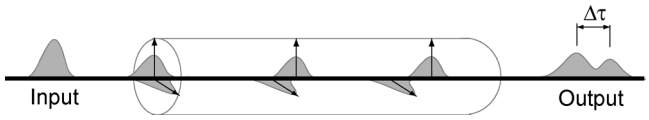


Fig. 1. Pulse bifurcation due to PMD. The power in the input pulse is split between the two polarization modes of the fiber. Birefringence causes a difference in phase velocities between the two modes, resulting in ISI at the output.

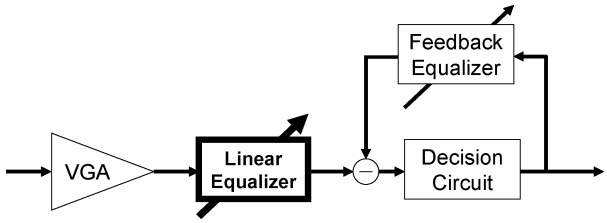


Fig. 2. Typical receiver architecture with decision-feedback equalization. The linear portion of the equalizer is emphasized in this work.

To define an appropriate architecture for the compensator, a model of PMD is required. It results, to a first order, in an input pulse being split into two pulses arriving at the receiver at different times, as shown in Fig. 1. The pulse spacing, $\Delta\tau$, is the differential group delay (DGD), γ is the proportion of the optical power in the "fast" state of polarization (SOP), and $(1-\gamma)$ is the proportion of power in the "slow" SOP. Hence, the impulse response of an optical fiber with PMD is modeled as [13]

$$h_{\mathrm{PMD}}(t) = \gamma\delta(t) + (1-\gamma)\delta(t-\Delta\tau). \tag{1}$$

Equation (1) is a linear time-invariant (LTI) PMD channel model. In reality, both γ and $\Delta\tau$ are time-varying random processes. Significant variations are observed on the order of milliseconds [12]. Even if an equalizer is continuously adapted to track these variations, the system will appear to be LTI over millions of bit periods at 40 Gb/s. Therefore, the LTI model is used throughout this work, as it has been elsewhere [14].

The parameter γ takes on any value from zero to one with uniform probability [15] whereas $\Delta\tau$ has a Maxwellian distribution [16]. The probability density function of the DGD is

$$\rho(\Delta\tau) = \frac{32\Delta\tau^2}{\pi^2\Delta\tau_{\mathrm{avg}}^3}\exp\left(-\frac{4\Delta\tau^2}{\pi\Delta\tau_{\mathrm{avg}}^2}\right) \tag{2}$$

where $\Delta\tau_{\mathrm{avg}}$ is the average DGD [17]. The average DGD is proportional to the square root of the fiber length, L,

$$\Delta\tau_{\mathrm{avg}} = P\sqrt{L} \tag{3}$$

where the constant of proportionality, P, is the fiber's "PMD parameter" in units of $\mathrm{ps}/\sqrt{\mathrm{km}}$.

Although PMD is not a concern over new fibers which can be manufactured with a PMD parameter as low as 0.05 $\mathrm{ps}/\sqrt{\mathrm{km}}$ [18], typical installed fibers have a PMD parameter of 0.5–2.0 $\mathrm{ps}/\sqrt{\mathrm{km}}$ [19]. Therefore, without compensation the reach of some installed fibers is limited to less than 10 km at 40 Gb/s. Therefore, PMD has been identified as the limiting factor in 40-Gb/s optical systems [20].

The frequency response of a fiber link modeled by (1) is

$$H_{\mathrm{PMD}}(f) = \gamma + (1-\gamma)e^{-j2\pi f\Delta\tau}. \tag{4}$$

The magnitude response, $|H_{\mathrm{PMD}}(f)|$, has notches at $f = (2k-1)/(2\Delta\tau)$, $k \in \mathbb{Z}$. The depth of these notches is dependent on γ, with the case $\gamma = 0.5$ resulting in complete nulls. Linear equalization can only amplify or attenuate signal content at particular frequencies. So, if deep notches appear in the frequency response of a channel, linear equalization alone cannot restore the lost portion of spectrum and the data is unrecoverable. However, decision feedback can use past decisions to fill in the missing spectral components and can, therefore, compensate for notches in the channel response. This work envisions a linear equalizer combined with decision feedback to combat PMD in 40-Gb/s optical fiber systems. A typical receiver architecture is shown in Fig. 2. In this paper, we focus on the highlighted linear equalizer portion.

For the linear equalizer, either a FIR filter or a "peaking" filter (designed to provide a variable boost in its high-frequency magnitude response) may be used. Peaking equalizers have been used in combination with decision feedback to equalize simple lowpass channels with relatively small reflections, such as arise in chip-to-chip communication [21]. However, they are not capable of equalizing the wide variety of possible SMF channel frequency responses. Analog FIR filters are preferred since they can provide a more flexible frequency response and can be implemented at high speeds.

FIR filters can be implemented with either baud-rate or fractional tap spacing. It has been shown that fractional tap spacing causes correlation between neighboring state signals (i.e., the tap amplifier outputs) that can lead to instability during adaptation of the tap weights [22]. Furthermore, it has also been shown that the use of fractionally spaced traveling wave filters makes the equalized mean squared error relatively independent of sampling phase [23]. As a result, equalizer adaptation and timing recovery loops can interact and drift. Therefore, baud-rate tap spacing is preferred in this work.

Fig. 3 shows the maximum tolerable average DGD (allowing a 3-dB power margin for noise) for decision feedback equalizers with various numbers of baud-rate forward and feedback taps [24]. The results show that when combined with feedback equalization, a 3-tap linear equalizer allows the receiver to tolerate a much larger average DGD (hence, a much longer fiber) than a 2-tap linear equalizer. However, the addition of a 4th and 5th tap provides little or no improvement. In fact, a 3-tap baud-rate linear equalizer followed by one tap of decision feedback is sufficient to eliminate PMD as the dominant length limitation in typical installed SMF at 40 Gb/s [24]. Recently, 1-tap feedback equalizers have been demonstrated up to 10 Gb/s in CMOS [25] and up to 40 Gb/s in SiGe [26]. The remainder of this paper focuses on the design of a 40-Gb/s 3-tap programmable filter with 25-ps tap spacing for the linear equalizer portion of a receiver.

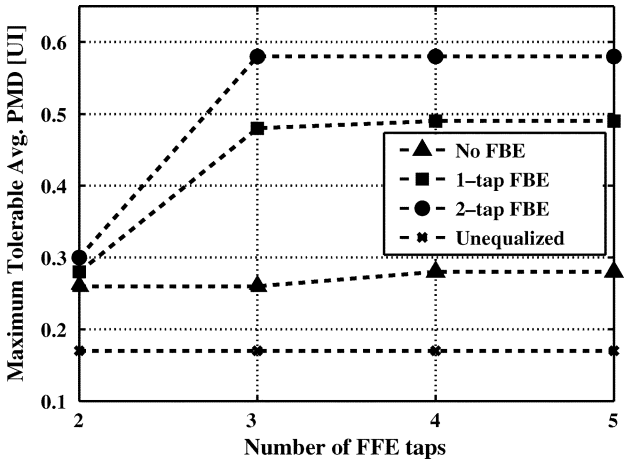


Fig. 3. Maximum tolerable average DGD, $\Delta\tau_{\rm avg}$, for various equalizer architectures allowing a 3-dB power margin for noise [24].

Such a filter is also suitable for the equalization of lossy transmission lines, such as electrical cabling and chip-to-chip interconnect.

III. Traveling Wave Filter Topologies

The TWF topology was first introduced over 30 years ago [27]. It uses transmission lines as broadband passive continuous-time delay elements. To achieve the delays required for a 40-Gb/s equalizer, an integrated microstrip, stripline or coplanar transmission line would have to be on the order of several millimeters long. As a result, the size of an integrated equalizer circuit would become prohibitively large. Long transmission lines also introduce significant series losses.

To combat these problems, artificial transmission lines are often used. These are made of lumped inductors and capacitors in a ladder. Essentially, winding the transmission lines into spirals increases their effective electrical length because of the additional mutual inductance between windings. Thus, the overall wire-length for a given delay is decreased, reducing the chip area and resistive losses.

The conventional 3-tap TWF with artificial transmission lines is shown in Fig. 4(a). The input and output transmission lines must have a characteristic impedance matched to the system impedance, $Z_0 = \sqrt{L/C}$, where L is the value of the lumped spiral inductors and C is the total capacitance at each internal node comprising mostly the tap amplifiers' input and output capacitances. Since larger devices are required to increase the gain in each tap amplifier, each node capacitance C is proportional to the maximum tap gain. The artificial transmission lines are terminated on-chip to a small-signal ground by resistive loads, $R \approx Z_0$.

The tap spacing is also determined by the size of the lumped *LC* elements, $T = 2\sqrt{LC}$. The cutoff frequency of a lumped *LC* transmission line section is equal to $f_c = 1/\pi\sqrt{LC}$. Therefore, the tap spacing and bandwidth of a conventional TWF are inversely related:

$$f_c = \frac{2}{\pi T}. \tag{5}$$

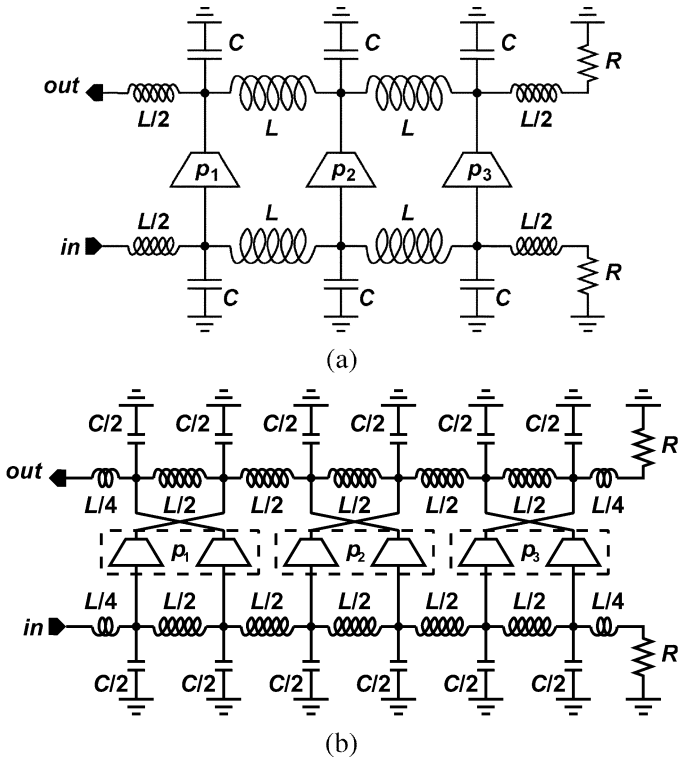


Fig. 4. Previous TWF topologies. (a) Conventional 3-tap FIR traveling wave filter (TWF) using artificial transmission lines. (b) The 3-tap FIR filter using a crossover TWF topology [6].

This inverse relationship between tap spacing and bandwidth is particularly problematic when implementing an equalizer with baud-rate tap spacing. Equation (5) predicts a cutoff frequency of only 64% of the bit rate in this case, which is insufficient to compensate for channel losses.

The crossover TWF topology using an artificial transmission line is shown in Fig. 4(b) [6]. It is a slightly modified version of the TWF topology, using a six-section transmission line to implement a 3-tap filter. By crossing the outputs of neighboring tap amplifiers, their gains add in phase at the filter output. Since twice as many sections are used, the inductance and capacitance per section are halved to provide the same delay per tap. Hence, the bandwidth of this architecture is $2\times$ greater than a conventional TWF having the same tap spacing and tap gain.

Theoretically, it should be possible to increase the bandwidth of the crossover TWF topology by further subdividing the delay lines and using more than two amplifiers per tap. For instance, Fig. 5(a) shows a single tap of a crossover TWF using three amplifiers per tap. Unfortunately, the crossover routing is no longer symmetric. The resulting mismatch and skew between the paths of different length may introduce unacceptable ripple into the frequency response.

In this work, we make use of an intermediate folded transmission line to perform the crossover routing with minimal delay mismatch. A single tap of the "folded-cascade" TWF is shown in Fig. 5(b). The tap spacing is the same as in Fig. 5(a). The delay lines are all composed of 1/3rd-sized *LC* sections, so that the bandwidth is $3\times$ greater than a conventional TWF for the same tap spacing. All paths through the network pass through exactly

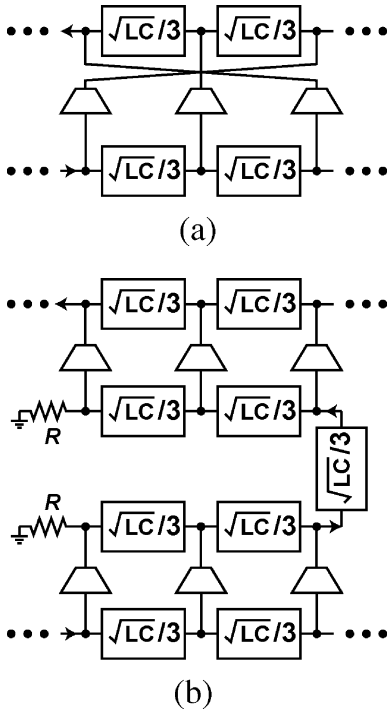


Fig. 5. Distributed tap amplifier topologies. (a) Extending the crossover TWF topology to three or more amplifiers per tap resulting in asymmetric crossover routing. (b) The folded-cascade TWF makes use of an intermediate transmission line to perform the crossover routing with minimal delay mismatch.

five *LC* sections and two gain cells. Hence, the gain through all nine such paths add in phase at the output, combining to serve as one tap amplifier. Using this topology for each tap results in the 3-tap FIR filter in Fig. 6. Notice that any two paths though neighboring tap amplifiers differ in length by six *LC* sections. Hence, the tap spacing is $6\sqrt{(L/3)(C/3)} = 2\sqrt{LC}$, just as in the conventional and crossover TWFs [Fig. 4(a) and (b)].

An alternative interpretation of the folded-cascade TWF is to recognize that each tap is really a cascade of two distributed amplifiers. The filter's input and output delay lines also serve as transmission lines for the distributed amplifiers. The conventional TWF topology is sometimes referred to as a "distributed" transversal filter because the input and output capacitances of the tap amplifiers are distributed over a passive network to increase bandwidth [28], [29]; but, unlike the folded-cascade TWF, the gain for each tap weight in a conventional TWF is provided by a single active circuit.

The artificial delay lines in a folded-cascade TWF can, of course, be further subdivided or even replaced with integrated microstrip, stripline or coplanar transmission lines. Furthermore, it should be possible to generalize the folded-cascade TWF topology even further by replacing the tap weight of Fig. 5(b) with a matrix amplifier [30]. The potential for further increases in gain or bandwidth using such structures require further study.

The folded-cascade TWF topology has drawbacks. First, because it requires two cascaded stages per tap, the power and area requirements are roughly doubled. Also, distributed amplifiers generally have more group delay variation than lumped amplifiers, and cascading them increases this variation. Careful design is required to ensure that the group delay performance is acceptable. A detailed analysis of nonidealities in TWFs was performed in [23], most of which is also applicable to the folded-cascade TWF. For instance, the parasitic input and output capacitances of each gain cell (including any interconnect capacitance not accounted for during design) will change the characteristic impedance of the artificial transmission lines. This, together with process and temperature variations in the on-chip termination resistors can lead to reflections along the transmission lines. In [6], tuning capacitors were provided to compensate for variations in the node capacitances along the transmission lines. However, because this design is pushing the process technology to its limits, additional tuning capacitors could not be accommodated. Fortunately, as explained in [23], first-order reflections due to mismatches on the artificial transmission lines appear within the filter span and, hence, can be managed by the equalizer adaptation.

IV. Prototype Circuit Design

The prototype integrated circuit is a fully differential implementation of the folded-cascade TWF shown in Fig. 6. It is designed for use with a 100 Ω (differential) system impedance with programmable tap gains. The supply voltage is $V_{\rm DD} = 1.8$ V. An analog voltage controls the gain of each tap. A fourth control voltage controls the common-mode voltage at the far end of the input transmission line, $V_{\rm CM}$. Setting this voltage equal to the input common-mode voltage (1.3 V, nominally), no DC current flows through the input transmission line, resulting in constant bias voltages along the length of the transmission line.

A. Transmission Lines

A total of five differential artificial transmission lines are used in the design of this equalizer: one at the input, one at the output, and one internal to each of the three taps. They are terminated by polysilicon resistors on-chip.

The values for the inductance $L/3$ and capacitance $C/3$ of each transmission line section are calculated to provide a characteristic impedance of 50 Ω per side (100 Ω differential) and a tap spacing of 25 ps (one bit period at 40 Gb/s). Since the tap spacing is determined by six *LC* sections, $\sqrt{(L/3)(C/3)}$ must equal to one-sixth of a bit period, or 4.17 ps. The resulting values of $L/3$ and $C/3$ are 209 pH and 83 fF per side, respectively. The node capacitances are made up purely of transistor and inductor parasitics. The inductances are spiral coils. Additional half-sized inductors, $L/6 = 105$ pH, are required at the ends of each transmission line as shown in Fig. 6.

The input differential transmission line is really two single-ended transmission lines as shown in Fig. 7(a), each designed to have a nominal characteristic impedance of 50 Ω. This provides good matching to single-ended test equipment. The two lines are isolated to avoid coupling between the two paths.

The other four transmission lines, Fig. 7(b), are made of coupled stacked differential inductors to minimize both area and series losses. Differential inductors can be used for these lines even if the input is driven single-ended because the first stage of differential amplifiers converts an unbalanced input into balanced differential signals.

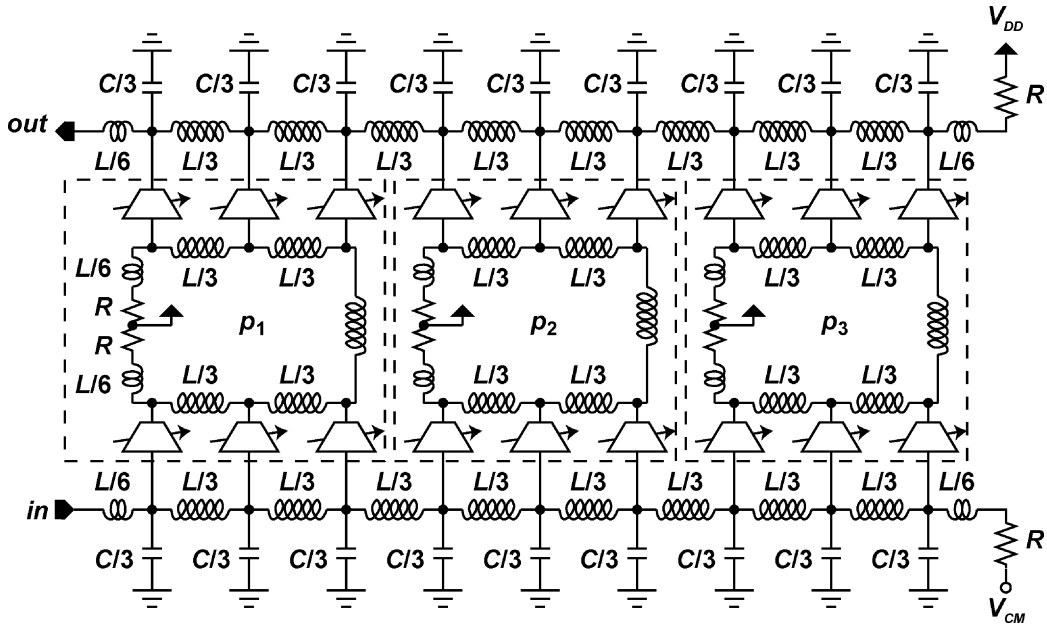
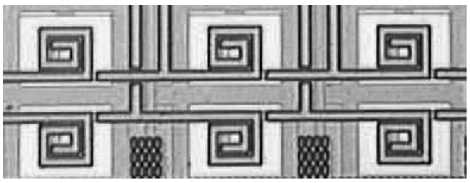
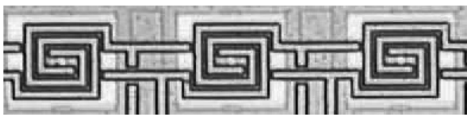


Fig. 6. A 3-tap folded-cascade TWF filter with programmable tap gains.



(a)



(b)

Fig. 7. Photographs of the artificial transmission lines in the prototype folded-cascade TWF. (a) Input transmission line. (b) Intermediate and output transmission lines.

Modified-pi models that include skin-effect and substrate losses were used for both the single-ended [31] and differential spirals [32]. The model parameters were fit to ASITIC [33] simulation results. The models can account for asymmetries in the spiral layouts with unequal terminal capacitances or conductances.

The transmission lines are terminated on-chip with 50 Ω per side. These resistances provide AC termination and a DC path for biasing. The input transmission lines are terminated to an external DC common-mode voltage. All other transmission lines are terminated to the supply voltage; gain cells sink bias currents through the termination resistors on those lines to set the DC common-mode voltages.

B. Gain Cell

Each gain cell is a simple differential pair, as shown in Fig. 8. Six of these differential pairs make up each of the three equalizer taps. Because 40-Gb/s operation is only possible in this technology when distributed circuit techniques are used, more complicated structures such as cascodes were not an option. Cascode structures have an internal circuit node that is not connected to a transmission line. The time constant at this node would limit the speed unacceptably for this application. The differential pair devices were sized so that their parasitic capacitances plus the inductor parasitic capacitances equal the required artificial transmission line capacitances, $C/3 = 83$ fF.

The gain of each of the gain cells is controlled by an analog control voltage, V_{CTRL}, that is provided off-chip. There are three control voltages, one for each tap. The control voltage for a given tap is connected to the gates of the tail current source transistors of all six differential pairs making up the tap. By varying V_{CTRL}, the currents through the differential pairs are varied, thereby changing their transconductance. This tuning mechanism is nonlinear as shown in the measurement results in Fig. 9. However, it is monotonic over the range 0.5–0.8 V, which is all that is required for convergence of gradient descent adaptation algorithms [34].

The maximum total current through the output stage of all three taps combined is limited to 20 mA. This is due to the restriction that the output common-mode voltage must not drop any lower than approximately 1.3 V for all transistors to remain in saturation while allowing differential signal swings in excess of 1 $\mathrm{V_{pp}}$ from a 1.8-V supply.

Each of the three taps has a fixed polarity. The first tap is positive, the second is negative, and the third is positive. This is accomplished by connecting the differential outputs of the tap 2 gain cells to the output transmission line with opposite polarity compared with taps 1 and 3. It was not possible to use a Gilbert cell mixer to implement signed tap weights [35] since the addition of internal circuit nodes would limit bandwidth as described above. It would have been possible to implement tap weights with programmable sign using two parallel gain cells

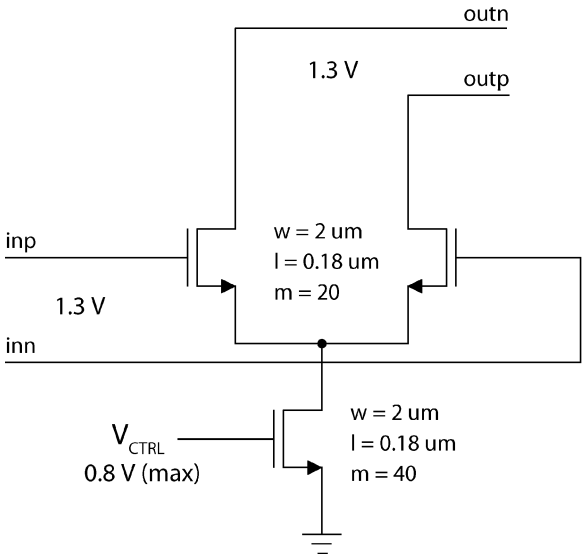


Fig. 8. Schematic of an equalizer gain cell. Six of these cells are used in each tap of the equalizer.

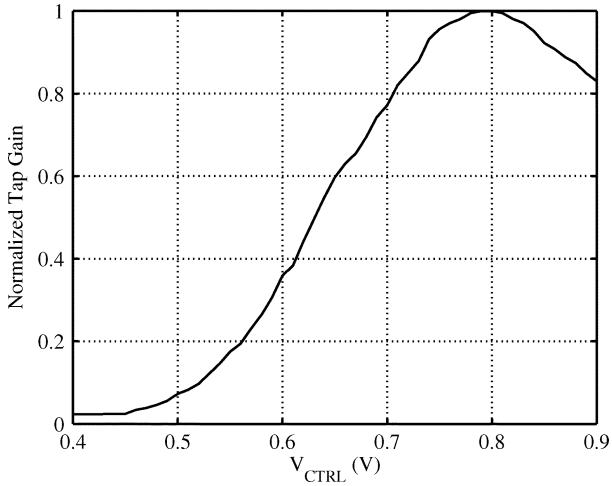


Fig. 9. Normalized tap gain plotted versus control voltage measured for tap 1 with a 5-GHz sinusoidal input.

connected with opposite polarity, as in [6]. However, since the total node capacitances $C/3$ are fixed, the size of each gain cell would have to be halved along with the corresponding tail currents, resulting in a halving of the gain. Hence, fixing the polarities provided a 6 dB increase in the maximum tap gains. This imposes a constraint on the adaptation of the tap weights for equalization. Of course, in any integrated circuit equalizer practical considerations restrict the tap gains to a finite range, but do not cause instability in gradient-based adaptation. In this case, the alternating polarities provide a high-pass response, as required to equalize the typically lowpass channels. System-level simulations verified that when combined with one tap of decision feedback, a 3-tap baud-rate FIR linear equalizer with alternating tap polarities is optimal for a wide variety of PMD-limited SMF channels.

C. Circuit Layout

A die photo of the circuit layout is given in Fig. 10. The overall dimensions of the equalizer IC are 1 mm $\times$ 1 mm. The active area is approximately 900 μm $\times$ 600 μm. The input pads appear on the left, the output at the top, and power and control signals at the bottom.

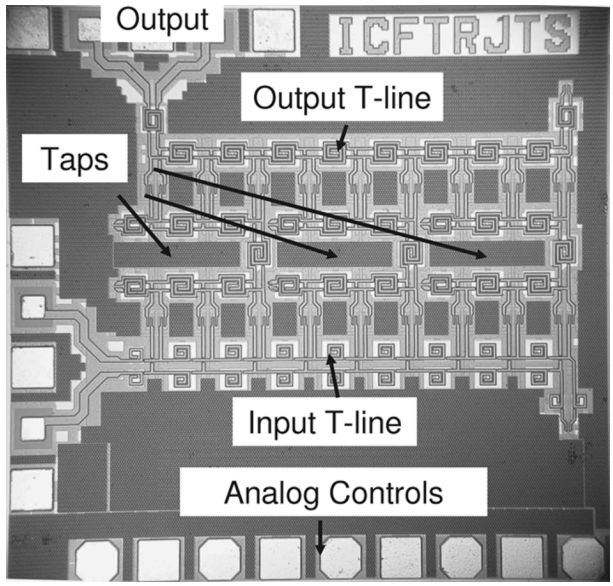


Fig. 10. Die photo of the prototype equalizer. The total area is 1 mm $\times$ 1 mm.

V. Measurement Results

All circuit measurements were made on-wafer. The test setup is diagrammed in Fig. 11. Bias and control voltages were generated externally. Due to the difficulty in avoiding skew between differential signal paths at these speeds, all testing was performed single-ended. One side of the differential input and output were terminated off-chip.

Fig. 12 shows the filter output with a 10 GHz sinusoidal input. The measurement was made by turning on each tap individually, with all other taps turned off. The tap spacing is 23 ps, just under one baud interval at 40 Gb/s. Note that the polarity of tap 2 is reversed compared with taps 1 and 3.

Fig. 13 shows the magnitude and phase response of each tap measured with a two-port network analyzer. Each tap is measured at its maximum gain setting with all other taps turned off. The phase response is linear up to 35 GHz. The group delays, calculated from the slope of the phase responses at 20 GHz $\pm$ 1 GHz, are 31, 52, and 74 ps for taps 1, 2, and 3, respectively, providing tap spacings of 21 and 22 ps. At 20 GHz, the measured phase difference between taps 1 and 2 and between taps 2 and 3 are 160 and 163 degrees (22 and 23 ps), respectively. This is in general agreement with the time-domain measurements at 10 GHz in Fig. 12 (23 ps). Since the measurements are single-ended, the magnitude of the differential gains would be 6 dB greater than shown Fig. 13(a). Significant loss and loss variation is observed from DC to 40 GHz. ASITIC simulations indicate a DC series resistance of approximately 2.5 Ω per *LC* section, increasing to 3.9 Ω per section at 20 GHz due to skin effect, which accounts for the observed losses. It has been shown that the deleterious effects of series losses can be mitigated by terminating the transmission lines with a resistance less than 50 Ω [23], but this was not done here. The gain decreases going

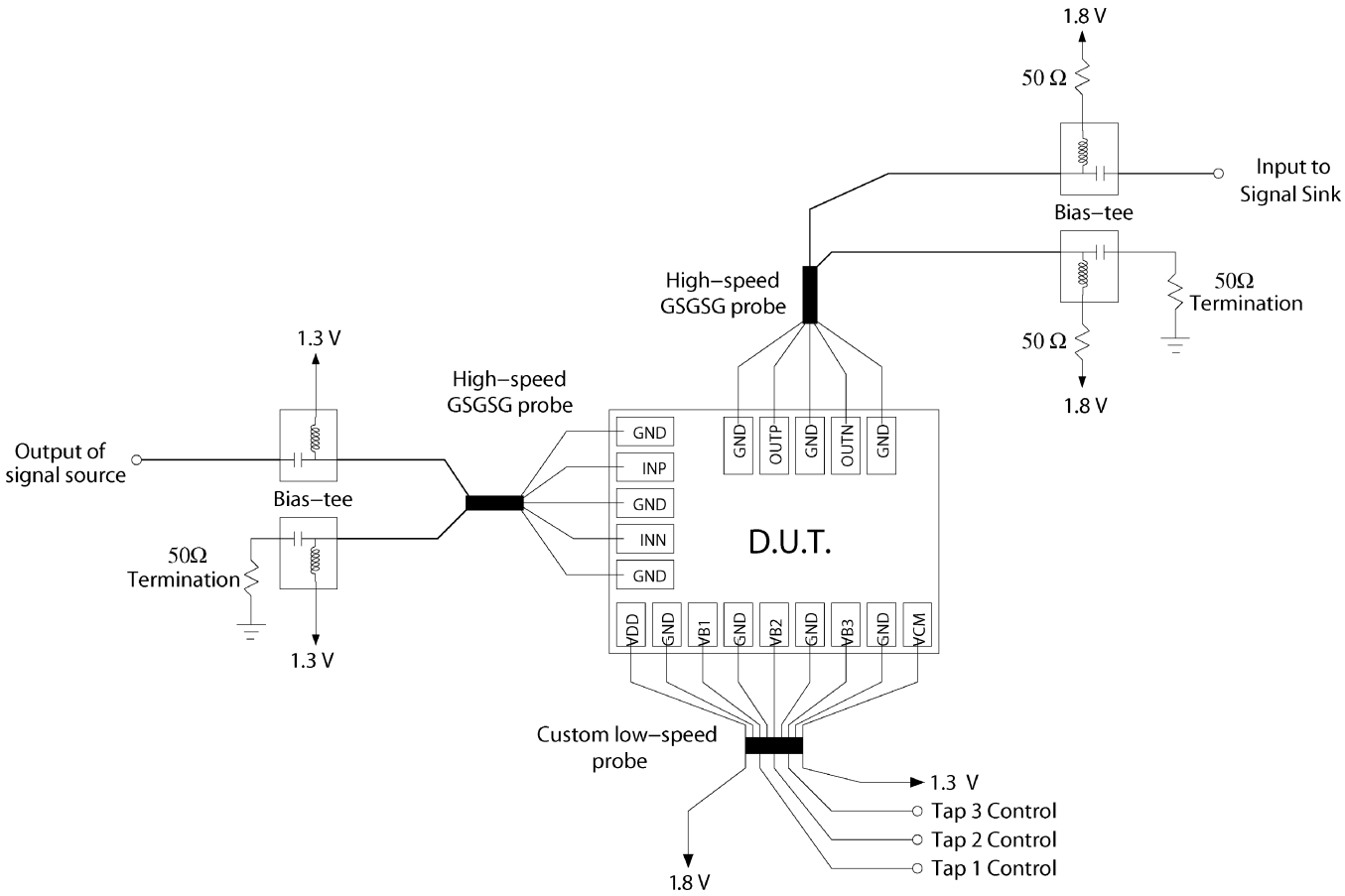


Fig. 11. Test setup for on-wafer measurement of the prototype equalizer.

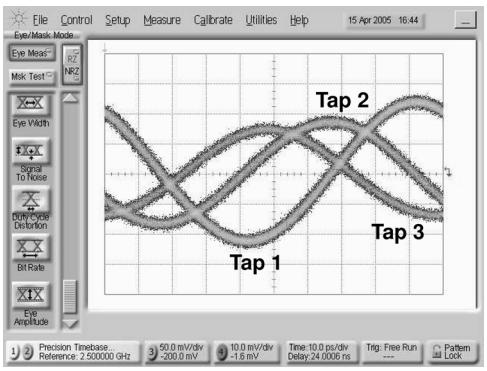


Fig. 12. Measured tap delays with a 200-mV peak-to-peak 10-GHz sinusoidal input.

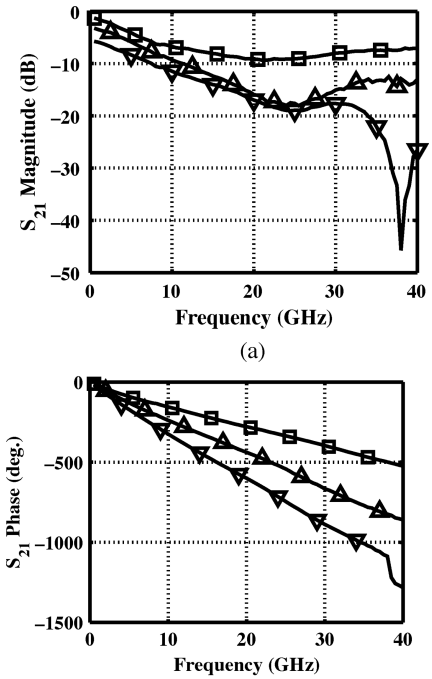


Fig. 13. Single-ended S_{21} magnitude and phase measurements made with a two-port network analyzer: tap 1 (□), tap 2 (△), and tap 3 (▽). (For differential S_{21} magnitude, add 6 dB.)

from tap 1 to tap 2 to tap 3 as the signal path goes through more lossy *LC* sections. These effects can be partially compensated for by appropriately setting all 3-tap gains, as would occur automatically in an adaptive equalizer.

Fig. 14 plots the magnitude of the input and output return losses, both simulated and measured with a two-port network analyzer. The input return loss is greater than 15 dB from 5 to 40 GHz while the output return loss is better than 16 dB up to 40 GHz. The input return loss degrades at low frequencies due to resistive losses along the input transmission line which appear in series with the 50 Ω terminations at low frequencies. Still, the measured input return loss is better than simulated at most frequencies, perhaps because the probe pad capacitances were less than estimated.

TABLE I
MEASURED RESULTS FOR THE PROTOTYPE FILTER AT 2 GHz

	Tap 1	Tap 2	Tap 3
Input 1-dB Compression (dBm)	0.0	1.5	2.5
IIP_3 (dBm)	15.8	17.0	18.3
THD at 0 dBm input (dB)	-31.1	-30.5	-34.9

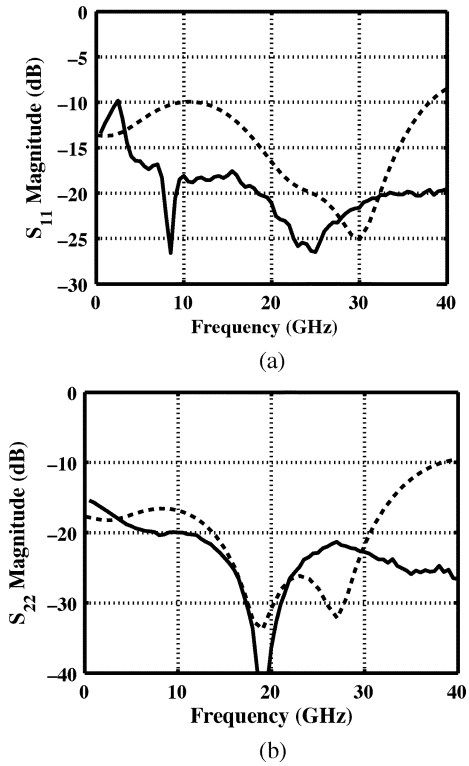


Fig. 14. Return losses of the prototype filter simulated (dashed) and measured with a two-port network analyzer (solid): (a) input return loss, (b) output return loss.

Tests were performed with a 2-GHz input to characterize the filter's maximum input swing. These are summarized in Table I. They suggest that sufficient swing is available to accommodate 4-PAM input signals that might arise in chip-to-chip applications [1]. Tap 3 appears to accommodate a larger input swing because its inputs are attenuated by a longer length of transmission line than taps 1 and 2.

For PMD-limited channels where $\gamma \approx 0.5$, a linear equalizer should be capable of providing a notch in its frequency response at roughly $1/\Delta\tau$. Then, a nonlinear feedback equalizer can restore the lost portion of spectrum with minimal noise enhancement. For instance, for a PMD-limited channel model with $\gamma = 0.5$, $\Delta\tau = 3$ UI, and transmitter and receiver bandwidths of 25 GHz, the frequency response of an ideal 3-tap baud-rate FIR equalizer that minimizes mean squared error has a notch at 7 GHz, as shown in Fig. 15. By appropriately setting all 3 tap gain control voltages, the prototype filter was able to provide the notched frequency response shown on the same plot, demonstrating the potential of the folded-cascade TWF for such applications.

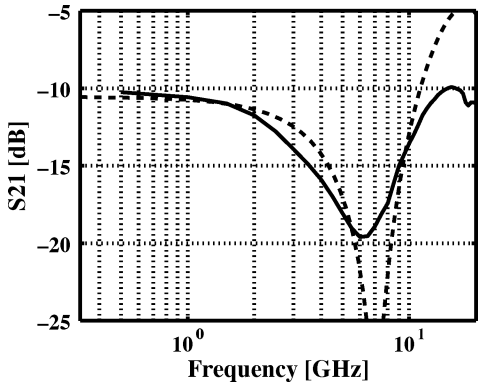


Fig. 15. Single-ended measured S_{21} magnitude response for the prototype filter (solid line) demonstrating a notch. The dashed line is the normalized frequency response of an ideal 3-tap baud-rate FIR equalizer that minimizes mean squared error in a receiver with DFE for a PMD-limited channel model with $\gamma = 0.5$, $\Delta\tau = 3$ UI, and transmitter and receiver bandwidths of 25 GHz.

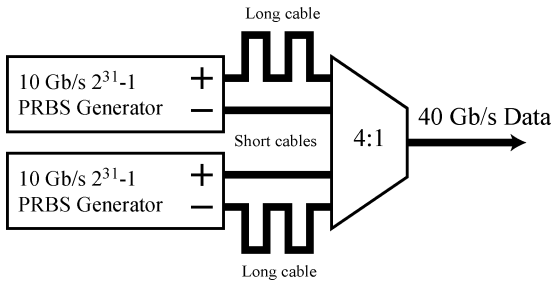
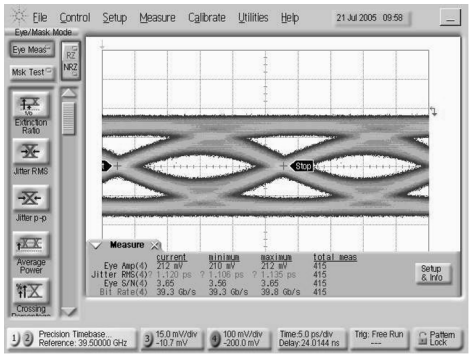


Fig. 16. Test setup for generating the 30- and 40-Gb/s data patterns.

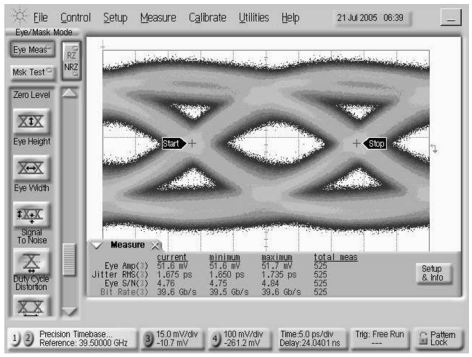
The prototype was also used to equalize 30 and 40-Gb/s non-return-to-zero (NRZ) data. The test setup for generating input data patterns up to 40 Gb/s is shown in Fig. 16. The differential outputs of two 10-Gb/s PRBS sources were skewed by different length cables to provide four uncorrelated 10-Gb/s PRBS $2^{31}-1$ patterns. The four patterns were then multiplexed to generate a 40-Gb/s data pattern. Although there was no way to properly synchronize the 10-Gb/s patterns to produce a true PRBS sequence at the multiplexer output, the resulting 40-Gb/s pattern's broadband spectrum was verified on a spectrum analyzer. In all of the equalization experiments, the filter coefficients were manually adjusted to maximize the eye opening.

First, a short (approximately 2 m) coaxial cable was used to generate ISI. Fig. 17 shows the input and output eye diagrams at 40 Gb/s over this cable. Oscilloscope measurements taken over the center 0.2 UI of the eye diagram are shown; they indicate an eye amplitude of 51 mV per side with a signal-to-noise ratio (SNR) of 4.76 (13.6 dB). If a gaussian noise distribution is assumed, this translates into a bit-error rate (BER) of less than 10^{-10}.

A longer 4 m coaxial cable was used to generate more ISI. The 4 m cable's frequency response is plotted in Fig. 18(a); 10 dB of loss is observed at 15 GHz and 17 dB of loss is observed at 20 GHz. Also shown in Fig. 18(a) for comparison is the frequency response of a PMD-limited channel model with $\gamma = 0.4$, $\Delta\tau = 25$ ps, and transmitter and receiver bandwidths of 25 GHz. Fig. 18(b) shows a 40-Gb/s single-ended unequalized eye pattern at the end of the 4 m cable.

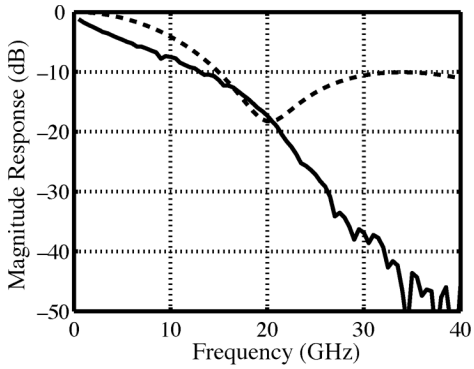


(a)

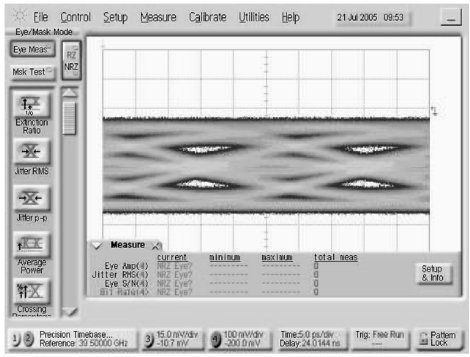


(b)

Fig. 17. Single-ended eye diagrams at 40 Gb/s with a short (approximately 2 m) coaxial cable: (a) equalizer input (b) equalizer output.

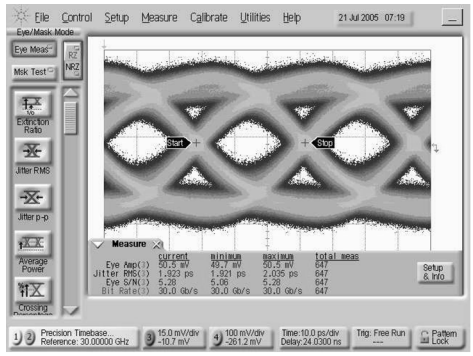


(a)

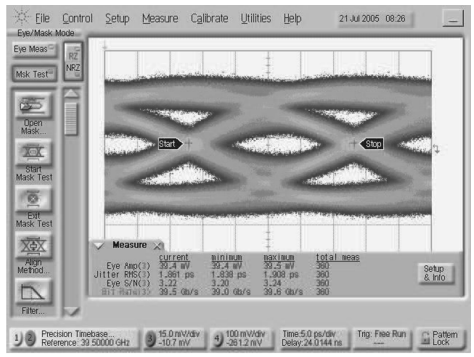


(b)

Fig. 18. Measurements of the 4-m coaxial cable used for 30- and 40-Gb/s testing: (a) measured cable frequency response (solid) along with the modeled response of a PMD channel with $\gamma = 0.4$ and $\Delta\tau = 25$ ps (dashed); (b) channel output (equalizer input) at 40 Gb/s.



(a)



(b)

Fig. 19. Single-ended equalizer output eye diagrams for 4 m cable at (a) 30 Gb/s and (b) 40 Gb/s.

TABLE II
PROTOTYPE SUMMARY AND COMPARISON WITH OTHER RECENTLY REPORTED INTEGRATED CIRCUIT TRAVELING WAVE FILTERS

	This work	[6]	[3]	[4]
Technology	0.18 μm CMOS	90 nm CMOS	InP/InGaAs	0.18 μm SiGe BiCMOS
Data rate (Gb/s)	40	30	40	49
Tap spacing (ps)	25	35	—	6.75
Number of taps	3	3	3	7
Supply voltage (V)	1.8	1	-4.3	5
Power (mW)	70	25	820	750
Area (mm × mm)	1.0×1.0	0.6×0.5	3.0×3.0	2.0×1.0

At 30 Gb/s, the equalized output eye is shown in Fig. 19(a). Measurements taken over the center 0.2 UI of the eye diagram indicate an amplitude of 50 mV per side with an SNR of 5.28 (14.5 dB). This translates into a BER of less than 10^{-13} if a gaussian noise distribution is assumed. The output eye measurement at 40 Gb/s [Fig. 19(b)] indicates a modest eye amplitude of 39 mV per side with a SNR of 3.22 (10 dB), translating into a BER less than 10^{-5} if a Gaussian noise distribution is assumed.

VI. CONCLUSION

This paper described a folded-cascade TWF topology capable of alleviating the delay–bandwidth tradeoff that is inherent in conventional TWF topologies. This topology is particularly useful in long-haul single-mode fiber links, where

a 3-tap baud-rate linear equalizer together with one tap of decision feedback is sufficient for PMD compensation. A 3-tap fully differential prototype is developed in 0.18-μm CMOS. The filter is faster than any previously reported CMOS equalizer, and at 70 mW it consumes less power than other 40-Gb/s equalizers implemented in more advanced technologies. A comparison with other state-of-the-art high-speed equalizers is presented in Table II.

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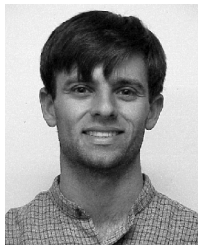

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Dr. Chan Carusone was a co-author of the best paper at the 2005 Compound Semiconductor Integrated Circuits Symposium. He is chair of the Analog Signal Processing Technical Committee for the IEEE Circuits and Systems Society, a member of the technical program committee for the Custom Integrated Circuits Conference, and an associate editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS.