Design of a Dual W- and D-Band PLL

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***Abstract*—This paper describes the design considerations and performance of the highest frequency phase-locked loop (PLL) reported to date. The PLL was fabricated in a 0.13-μm SiGe BiCMOS process and integrates on a single die: a fundamental-frequency 86–92 GHz Colpitts voltage-controlled oscillator (VCO), a differential push-push 160-GHz Colpitts VCO with two differential outputs at 80 GHz, a programmable divider chain, the charge pump, and all loop filter components. It achieves the lowest W- and D-band phase noise of -93 dBc/Hz at 90 GHz and -87.5 dBc/Hz at 163 GHz, both measured at a 100 kHz offset, and demonstrates an extended locking range of 80–100 GHz at the fundamental frequency, and 160–169 GHz at the second harmonic output of the push-push VCO. The single-ended PLL output power is -3 dBm at 90 GHz and -25 dBm at 164 GHz. The chip consumes 1.25 W from 1.8 V, 2.5 V, and 3.3 V supplies and occupies 1.1 mm x 1.7 mm, including pads.**

***Index Terms*—D-band, divider chain, LO distribution, mm-wave ICs, phased-locked loop, phase-noise, SiGe BiCMOS, VCO, W-band.**

I. Introduction

In recent years, the number of publications reporting silicon transmitters, receivers, and transceivers operating in the W-band (75–110 GHz) and D-band (110–170 GHz) has grown steadily. Operation at these frequencies is ideally suited for short and medium range communication with the advantage of (i) encountering much lower atmospheric attenuation levels than those in the now popular 60-GHz band, and (ii) employing a smaller wavelength, comparable to the size of a D-band transceiver front-end, making the integration of on-die antennas economically feasible. The resolution of imaging and radar applications also benefits from shorter wavelengths. Recent W-band and D-band transceivers implemented in SiGe BiCMOS and CMOS technologies have successfully targeted a variety of emerging applications including industrial sensors [1]–[5], imagers [3], [6], [7], 10-Gb/s wireless [8]–[11], and series wireline 107-Gb/s Ethernet links [12]. In each case, a low-noise phase-locked loop (PLL) is either mandatory or desirable, the design and implementation of which is the focus of this paper.

Although 60-GHz or W-band silicon PLLs have recently been reported [13]–[24], none of them operate above 100 GHz and none of the fully integrated PLLs meet the automotive radar requirements of <-80 dBc/Hz phase noise at 100 kHz offset [25], or the integrated phase error demanded by multi-gigabit data-rate wireless links with QPSK, QAM, and OFDM modulation schemes. In this paper, we demonstrate the first D-band PLL in silicon and investigate its phase noise performance for different reference frequencies ranging from 600 MHz to 6 GHz and for PLL bandwidths between several hundred kilohertz to several megahertz.

Section II presents the architecture of the implemented dual-band PLL along with specific circuit blocks and simulation results describing the noise contribution of the individual blocks. Section III discusses fabrication and various layout and isolation techniques to improve the mm-wave performance of the system. Section IV discusses various layout and isolation techniques to improve the mm-wave performance of the system. Section V presents the measurement results followed by the conclusion.

II. PLL Design and Simulation

The loop behavior of third-order charge-pump PLLs has been studied extensively in the literature [26], [27]. PLLs with second-order loop filters have been used to demonstrate phase and frequency locking up to 100 GHz. Third and fourth-order loop filters have also been studied [26]. Higher order filters can help to further reduce the reference spurs but they contribute additional thermal noise to the loop.

In this design, we have selected the classic third-order charge pump PLL architecture with a second-order loop filter for its simplicity and lower noise performance. The problem of reference spur feedthrough was considered secondary in this design because of the relatively large reference frequency (>600 MHz). Such high-frequency spurs are naturally attenuated and typically fall outside the band of interest for most imaging and radar applications. However, they may be of concern in gigabit data-rate millimeter-wave radios. We will examine the contributions to the in-band and out-of-band PLL phase noise from various parameters and circuits, such as divider ratio, reference signal phase noise, and the reference and prescaler buffer noise.

The loop phase margin and closed-loop bandwidth were derived using linear models. In practice, the choice of PLL bandwidth is application dependent. In general, if the phase noise

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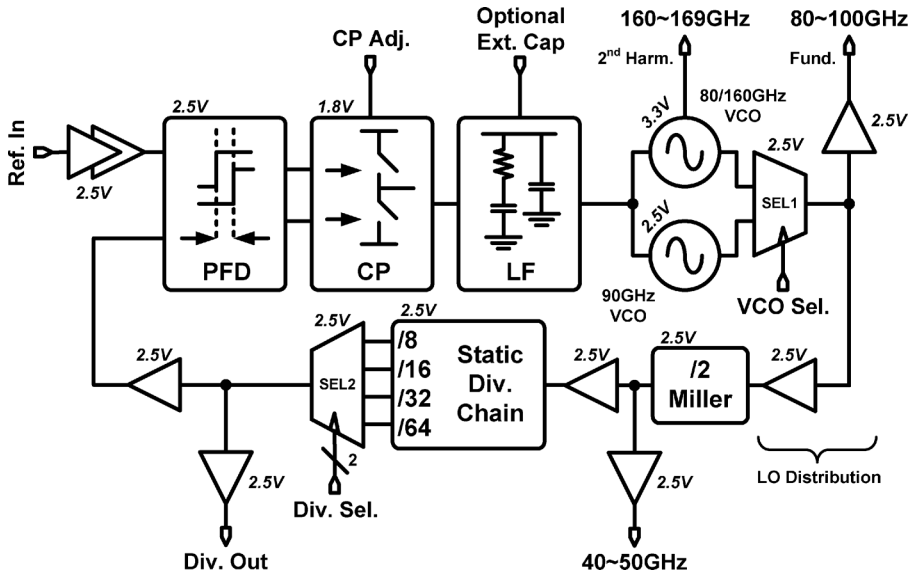

Fig. 1. Simplified PLL block diagram.

of the free-running VCO at the frequency offset of interest is higher than the multiplied phase noise of the external low-frequency crystal reference, a large loop bandwidth is desired in order to minimize the overall phase noise. However, in the case of some high-data-rate fiber optic applications, a low loop bandwidth combined with high phase margin is chosen to avoid excessive jitter peaking. PLL-based clock and data recovery, and some automotive radar systems, often require a large loop bandwidth to track incoming jittery data, or to allow fast VCO modulation ramps. In contrast, most mm-wave active imagers and portable 60-GHz high-data-rate radios, which employ low-cost MHz-range reference crystal oscillators and/or prescalers with very large division ratios, need sub-MHz PLL loop bandwidths.

The charge pump current ($\mathrm{I_{CP}}$) and the prescaler divide ratio (M) were designed to be adjustable, while the loop filter parameters were fixed by die area and stability constraints. However, provisions were made to allow for external filter capacitors in order to reduce the loop bandwidth and to ensure loop stability for all divider ratios. While this PLL does not target a specific application, it is meant as a vehicle to explore the ultimate low phase noise performance that can be realized in the 80–170 GHz range and to identify the critical noise contributors. This will help us optimize the system architecture of future active and passive imaging and industrial radar sensors operating in the D-band.

A. PLL Architecture

This design combines the classic third-order PLL architecture with a W-band local-oscillator (LO) signal distribution tree and a push-push VCO to achieve low-noise phase locking in the D-band. The choice of a push-push over a fundamental frequency D-band VCO was dictated by the difficulty of realizing a 160-GHz divider chain capable of reliable operation over temperature, process, and supply corners.

As illustrated in Fig. 1, the PLL is equipped with two VCOs, a fundamental 90-GHz Colpitts VCO, and a differential 160-GHz push-push Colpitts VCO with simultaneous outputs at 80 GHz [6]. A mm-wave selector chooses the desired VCO signal and is followed by the LO distribution network. The PLL prescaler comprises a 110-GHz Miller divider [2] followed by six static frequency divider stages. A four-input multiplexer is implemented in the divider chain to enable selectable divide ratios of /16, /32, /64, or /128. The divider output and the reference frequency signal are fed into a phase-frequency detector followed by a second-order loop filter (LF) whose output is directly connected to the varactor control nodes of both VCOs. All signals are differential.

B. Charge Pump

The charge pump is implemented using an HBT-MOS differential folded-cascode opamp with SiGe HBT inputs and common-gate 0.13-μm p-MOSFETs (Fig. 2). A common-mode feedback (CMFB) circuit is used to set the output DC voltage at $\mathrm{V_{dd}}/2$ which also matches the common-mode voltage of the VCO varactor. This approach maximizes the CP output swing and the VCO tuning range which, in turn, maximize the PLL locking range.

The charge pump tail current can be adjusted externally from 70 μA to 1500 μA to vary the PLL bandwidth. An order of magnitude of CP current control is typically sufficient to cover a wide range of loop bandwidths and to offer some immunity against $\mathrm{K_{VCO}}$ changes due to process and temperature variations. The combination of bipolar input transistors ($\mathrm{Q_{1–4}}$) and wide swing PMOS cascode loads ($\mathrm{Q_{5–8}}$) allows the charge pump to operate from a 1.8 V supply while achieving high gain and large output swing.

C. Loop Filter

The integrated differential loop filter comprises a pair of 180-pF capacitors, 500-Ω resistors, and 40-pF dampening capacitors. The loop filter capacitors are implemented using unit metal–insulator–metal (MIM) capacitors with the largest possible area allowed by the DRC density rule. This approach minimizes the inductive interconnect required to join individual

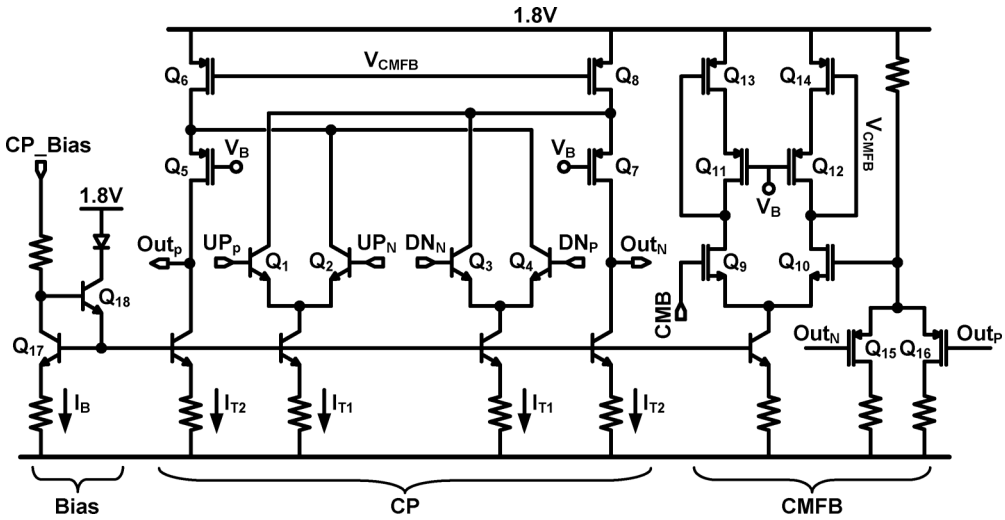

Fig. 2. Charge pump schematic.

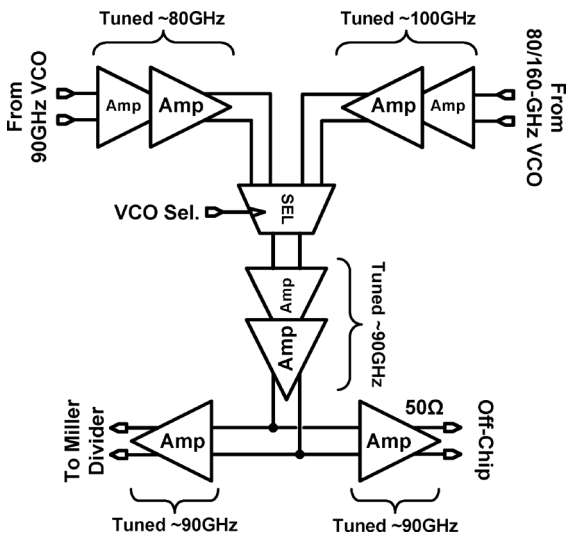

Fig. 3. Block diagram of the LO distribution network.

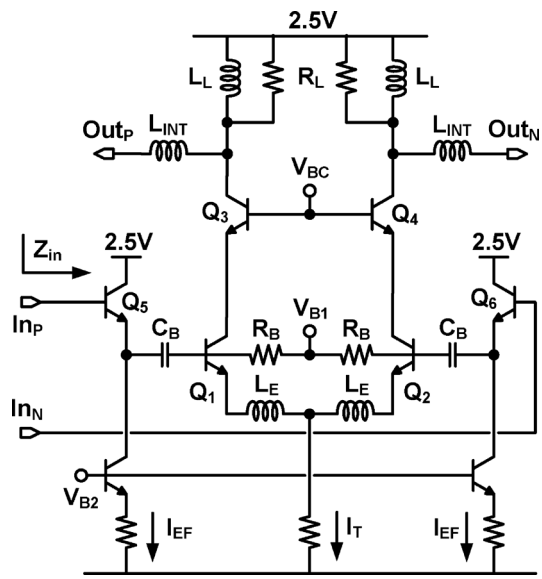

Fig. 4. Schematic of the tuned amplifier block used in the LO distribution network.

unit MIM capacitors and ensures that the areal density of the filter is maximized. Additional loop filter capacitors can be connected externally via a pair of designated pads in order to further optimize the PLL loop for bandwidth and stability.

D. LO Distribution Network

The design of the LO distribution network poses two challenges: (i) the bandwidth must be over 20 GHz to cover both VCO frequencies with sufficient output signal amplitude to ensure reliable operation of the prescaler, and (ii) it must drive the prescaler and the output pads simultaneously. The former problem was addressed by staggering the center frequencies of the LO distribution amplifiers as illustrated in Fig. 3. The amplifiers immediately following each VCO are tuned at the VCO center frequency while all amplifiers common to both VCO signals are centered at the average frequency between the two VCOs.

1) LO Distribution Amplifiers: The LO distribution amplifier stages consist of a pair of emitter followers ($Q_{5–6}$) and a cascode differential pair ($Q_{1–4}$) as illustrated in Fig. 4. The use of the common-collector configuration extends the bandwidth of the overall amplifier chain; AC coupling the emitter followers to the differential pairs (C_B) permits each amplifier to operate from a 2.5-V supply. Special care must be taken to ensure the stability of the entire LO distribution network, particularly because emitter-followers and relatively large current cascode stages are employed. The addition of the resistors (R_L) in parallel with the load inductors (L_L) lowers the quality factor of the matching network which broadens the bandwidth of each stage. Furthermore, this helps to stabilize the amplifier chain. All amplifier blocks are identical except for the matching networks which determine the center frequency of each block.

2) mm-Wave VCO Selector: The schematic of the mm-wave selector is reproduced in Fig. 5. Each half-circuit consists of a pair of emitter-followers ($Q_{7–8}$) and a variable gain amplifier ($Q_{1–6}$). Sel_P and Sel_N select the desired VCO signal. The layout

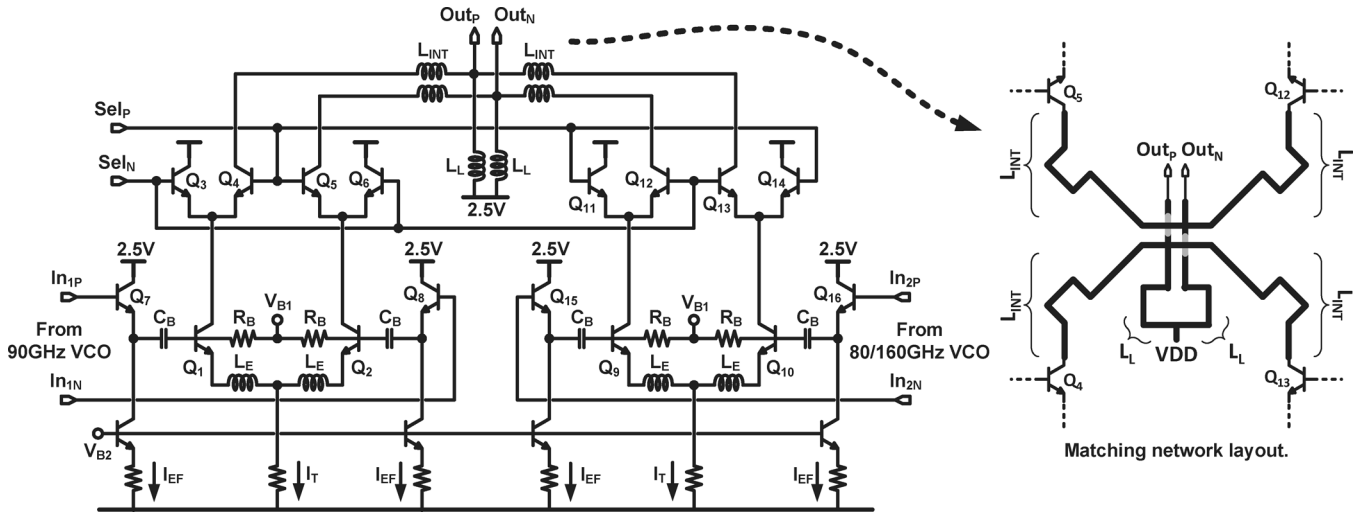

Fig. 5. Schematic of the mm-wave VCO selector and the layout of the matching network.

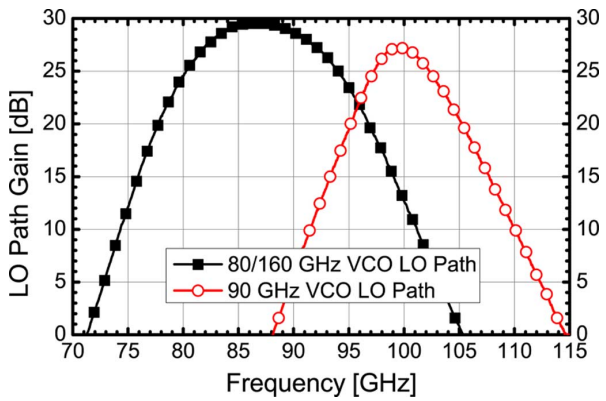

Fig. 6. Simulated small-signal gain of the LO distribution paths.

of the matching network (L_{INT} and L_L) at the output of the selector is sketched in Fig. 5. This arrangement enables a symmetric connection from transistors (Q_{4-5}) and (Q_{12-13}) to the common output and V_{dd} nodes. The simulated small-signal gain of the LO distribution network for both VCO paths is shown in Fig. 6.

E. Voltage-Controlled Oscillators

Both the 80/160-GHz and 90-GHz VCOs use a common-collector Colpitts topology which is known for its low-phase-noise capability [28]–[31]. VCO schematics are shown in Fig. 7. In order to minimize the phase noise, the tank inductor value was chosen as small as possible, and the HBTs were biased at the minimum noise figure current density (J_{OPT}) [30]. Both VCOs employ thin-oxide, minimum gate length, accumulation-mode AMOS varactors whose layout was optimized to maximize the quality factor. The latter remains larger than 6 beyond 170 GHz and is critical in achieving record low phase noise in the free-running VCOs. Furthermore, the technology provides two 3-μm-thick copper layers and thick inter-layer dielectric (ILD) [32] which allow for very high Q inductors to be realized. A MIM capacitor (C_1) was added across the base-emitter junction of the HBT to reduce the noise contribution of the base resistance and alleviate supply pushing. Complete design methodologies for low phase noise VCOs in SiGe HBT and Si CMOS technologies can be found in [30] and [29], respectively.

The 90-GHz VCO employs a single common-collector (the collector inductor is small enough to act almost as a short circuit) transistor per side which enables it to operate from a 2.5-V supply and minimizes phase noise. The 80/160-GHz push-push VCO [7] employs a cascode topology with the second harmonic being tapped off from the base node of the common-base HBTs. This scheme improves buffering of the VCO tank but requires raising the supply voltage to 3.3 V and causes the phase noise to increase compared to a single-transistor common-collector topology.

F. Simulations

Before simulating the phase noise of the PLL, the phase noise of the reference signal source (Agilent E8257D) and of the two VCOs was measured. These stand-alone VCO breakouts, from an earlier fabrication run in the same technology, had slightly different tank inductors and VCO loading than those used in the PLL. Representative plots of the measured signal source phase noise at 625 MHz and 5 GHz are shown in Fig. 8. The measured free running phase noise of the fundamental frequency 90-GHz Colpitts VCO is -105 dBc/Hz at 1 MHz offset (Fig. 9, top) with the noise-floor reaching about -120 dBc/Hz. The phase noise and the noise floor of the free-running push-push VCO is higher, -98 dBc/Hz at 1 MHz offset (Fig. 9, bottom). The higher noise can be attributed to the cascode topology which has higher noise than the CE topology. This higher noise at moderate offset frequencies emphasizes the need for a relatively wide loop bandwidth adjustment range in the PLL design in order to optimize the phase noise for both W- and D-band applications. The measured tuning range and corresponding K_{VCO} for the two VCOs are shown in Fig. 10.

A linear phase-domain model was assembled and simulated using Cadence SpectreRF. The measured reference and free-running VCO phase noise were included in the simulation, along with noise contributions from individual blocks as extracted from transistor-level simulations using the SpectreRF periodic steady-state simulator and PNOISE. The K_{VCO} and phase noise

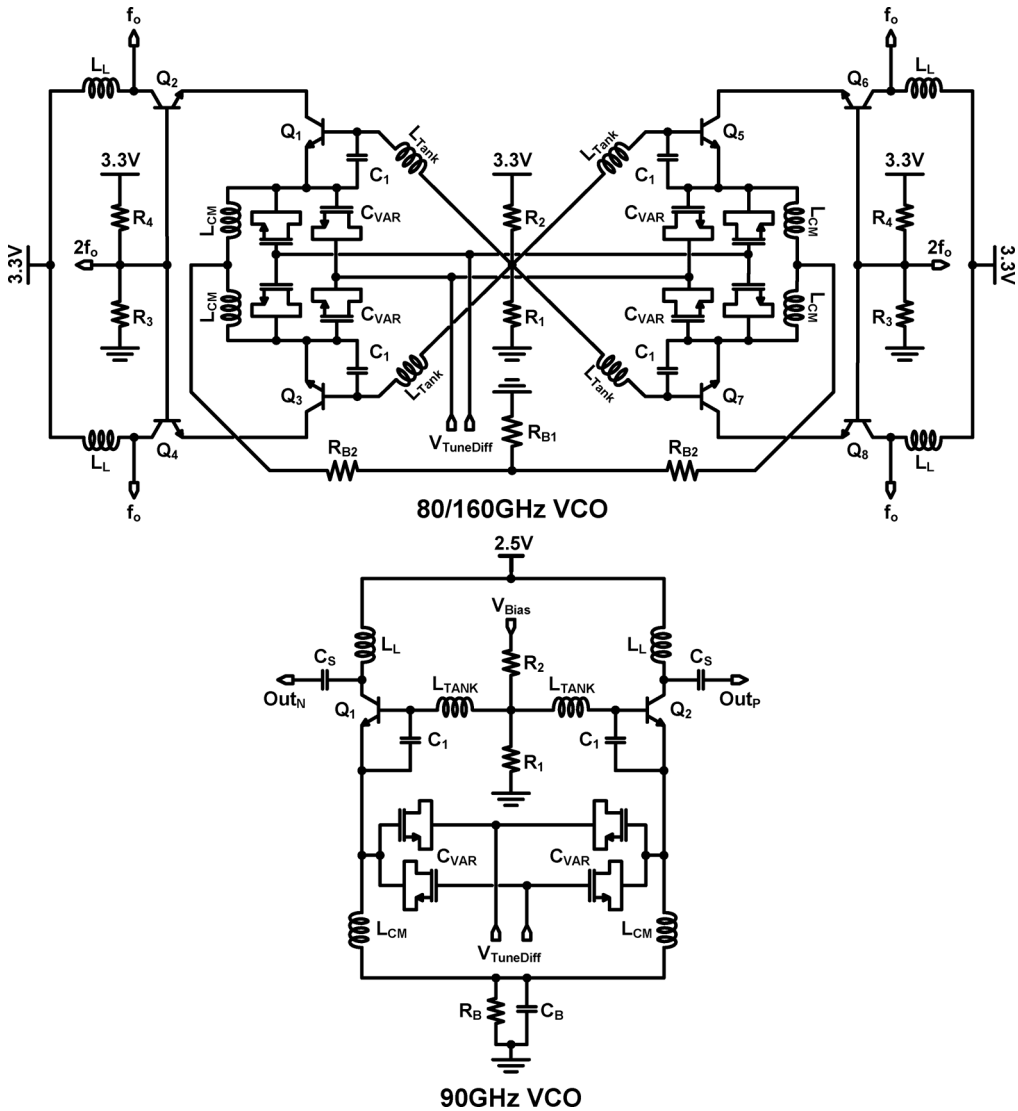

Fig. 7. The schematic of the 80/160-GHz (top) and 90 GHz (bottom) Colpitts VCOs.

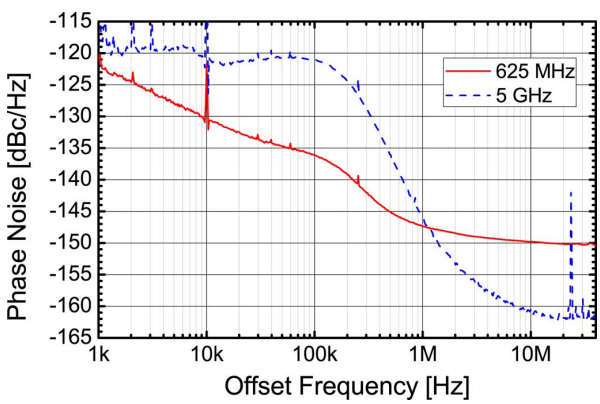

Fig. 8. Measured phase noise of the PLL reference signals at 625 MHz and 5 GHz.

of VCOs vary with the control voltage, but characteristic values of 1.5 GHz/V and −95 dBc/Hz @ 1 MHz offset were used for simulation purposes.

Simulation results of the PLL output phase-noise and the primary noise contributors are shown in Fig. 11 with divide ratios of 128 (top) and 16 (bottom). At a divide ratio of 128, the in-band phase-noise is dominated by noise contributed from the buffer chains that connect the reference signal and the prescaler output to the phase-frequency detector. At larger offset frequencies, outside the loop-bandwidth, the primary noise contributors are the VCO phase noise and the thermal noise of the loop filter.

For a divide ratio of 16, the charge-pump current was reduced by one third and an external 100-nF capacitor was included in order to ensure loop stability and reduce peaking. With this divide ratio, the buffer chains become again a primary source of noise at low offset frequencies, but the reference signal noise can now be seen to be dominant for some in-band offset frequencies. At higher frequencies, the primary noise sources are again the VCO and LPF. For both divide ratios, the contribution of the charge-pump noise current was found to be negligible at the PLL output.

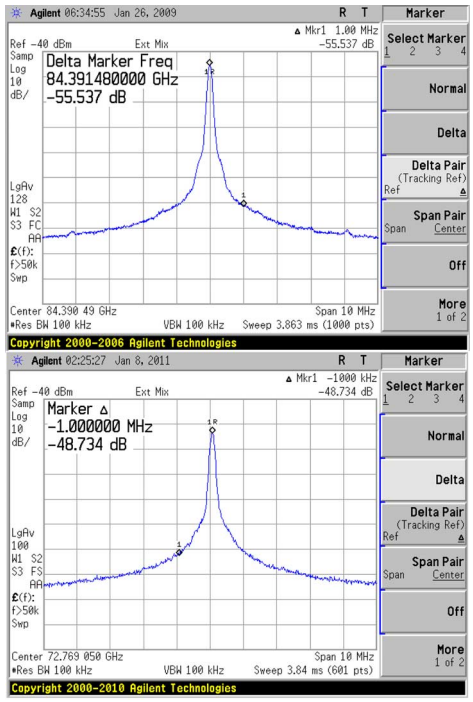

Fig. 9. (Top) Measured output spectrum of the fundamental 90-GHz Colpitts VCO. (Bottom) Measured output spectrum of the fundamental 80/160-GHz VCO.

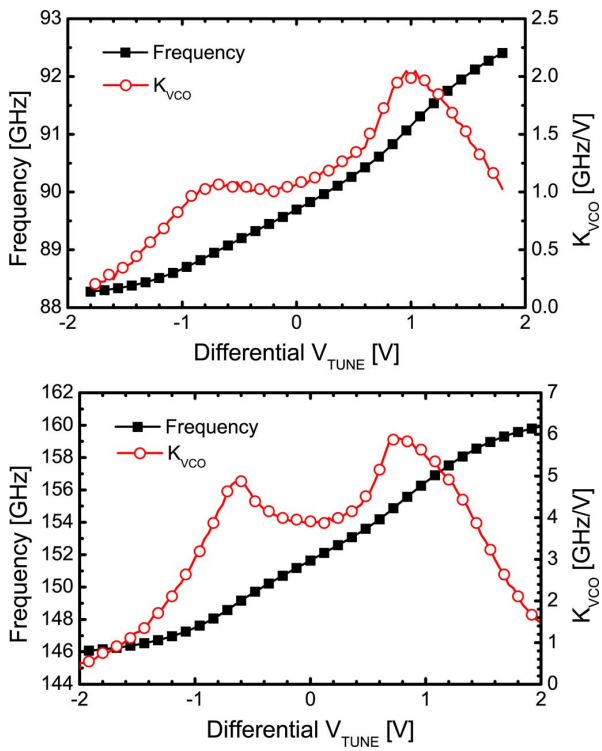

Fig. 10. The measured frequency and K_{VCO} for the 90-GHz Colpitts VCOs (top) and 80/160-GHz push-push (bottom).

III. Fabrication

The circuit was fabricated in STMicroelectronics' 0.13 μm SiGe BiCMOS process with HBT f_T and f_{MAX} of 230 GHz and 280 GHz, respectively. The process offers six layers of copper metallization, the top two being 3 μm thick [32].

All critical circuit blocks use separate power supplies to prevent noise injection from neighboring digital circuits. This type of isolation is accomplished by surrounding each block with alternating grounded substrate taps (P-TAPs) and n-wells (N-TAPs) which are tied to a quiet power supply. Furthermore, grounded stacked metal shields, extending from metal 1 to the top-metal aluminum layer, isolate the power supply metallization planes from one another. Sensitive analog bias and signal lines, which are implemented in metal 5, are shielded using grounded metals 6, 5, and 4 in a Faraday cage configuration. A three-dimensional layout view of this type of isolation structure is shown in Fig. 12. The photo of the 1.1 mm x 1.7 mm die is shown in Fig. 13. The location of the inputs, outputs, and various circuit blocks are annotated on the die photo.

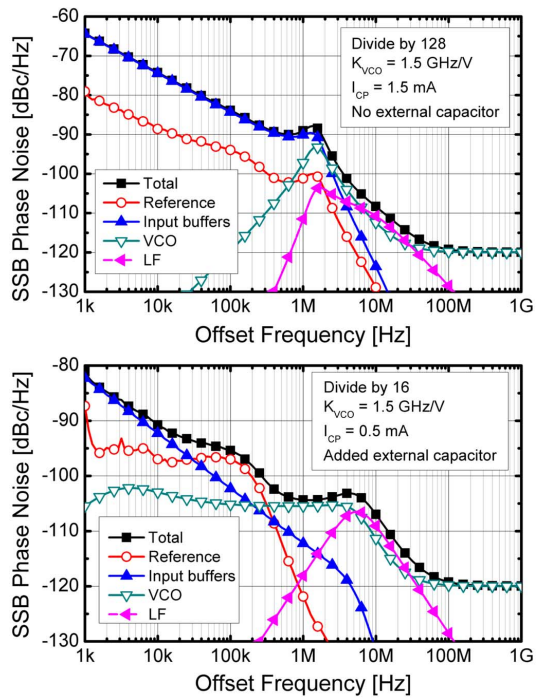

Fig. 11. Simulated PLL phase noise contributors at the VCO output using the measured reference phase noise, measured free running VCO phase noise, and simulated block-level phase noise. Shown for divider ratios of 128 (top) and 16 (bottom).

IV. Measurement Results

The PLL operates from a 2.5-V supply except for the charge pump and the 80/160-GHz quadrature VCO which use 1.8 V and 3.3 V, respectively. The total power consumption is 1.15 W or 1.25 W depending if the 90-GHz or the 160-GHz VCO is activated. The LO distribution, 90-GHz and 80/160-GHz VCOs consume 600 mW, 125 mW, and 225 mW, respectively. The remaining power is dissipated in the divider chain, PFD, charge pump, and output drivers.

We have recently shown that the VCO and prescaler power consumption can be more than halved to less than 80 mW and 100 mW, respectively, by employing low-voltage topologies in the same technology [5].

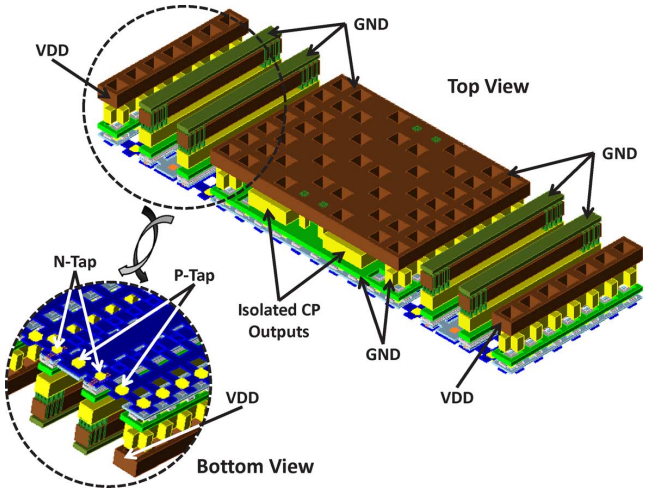

Fig. 12. Three-dimensional layout view of the PLL isolation structure for power supply separation and sensitive analog signal shielding.

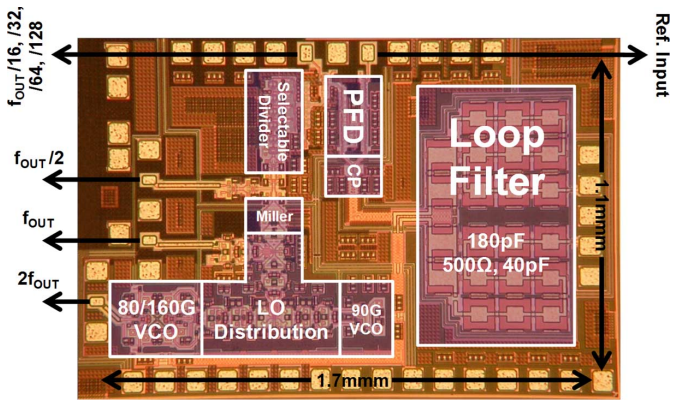

Fig. 13. Die photograph of the PLL. The total area including pads is 1.7 mm x 1.1 mm.

The measured PLL locking range extends from 86 GHz to 92 GHz for the 90 GHz fundamental VCO, and from 162 GHz to 164 GHz for the push-push VCO. It was noted that, by changing the bias current and power supply voltage of the VCOs from the nominal values, it was possible to adjust the center frequency of both VCOs and extend the locking range of the PLL from 80 GHz to 100 GHz in the W-band, and from 160 GHz to 169 GHz in the D-band. The Miller divider and the LO distribution network limit the locking range below 80 GHz, or below 160 GHz for the push-push VCO.

An Agilent E8257D signal source was used as a reference signal and an Agilent E4448A PSA, equipped with phase noise personality software, was employed to conduct phase noise measurements of the fundamental signal, and of the signal after the first divider stage. Phase noise measurements at the final divider output and of the reference signal generator were performed using an Agilent E5052A SSA, but measurements with that instrument are limited to below 7 GHz.

The measured PLL phase noise at 99.2 GHz is illustrated in Fig. 14 for a constant charge-pump current of 0.5 mA. Results are shown for the minimum and maximum divide ratios (16 and 128). The symbols correspond to measurements performed at the fundamental frequency output of the system (using the

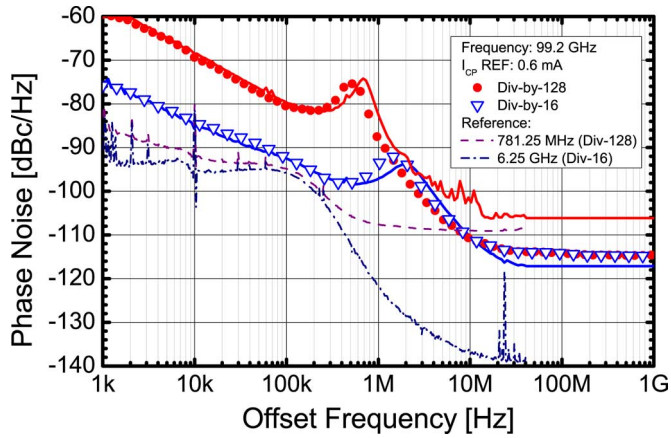

Fig. 14. Measured PLL phase noise at 99.2 GHz for divider ratios of /16 and /128. Symbols show the measured phase-noise at the fundamental frequency, and the lines show the frequency scaled phase-noise results as measured at the final divider output. The measured phase noise performance of the reference source are shown in dashed and dash-dotted lines, multiplied by the divide ratio ($20\log_{10}(N)$).

Agilent E4448A PSA with an 11970W waveguide harmonic mixer), whereas the solid lines were captured using the Agilent E5052A signal source analyzer at the final divider output. The phase-noise data were then multiplied to the fundamental frequency according to the appropriate divide ratio. Additionally, the phase-noise data of the two reference signals are shown for the two divide ratios and similarly multiplied to the fundamental frequency. For a divide ratio of 16, the phase noise is better than -90, -95, and -110 dBc/Hz at 100 kHz, 1 MHz, and 10 MHz, respectively. For a divider ratio of 128, the phase noise is approximately -80, -80, and -110 dBc/Hz at 100 kHz, 1 MHz, and 10 MHz, respectively.

The difference between the measured noise floor at the fundamental (symbols) and final prescaler output (solid lines) can be attributed to the limited dynamic range of the on-chip 50-Ohm output buffers and of the measurement equipment itself. At a divide ratio of 16, the prescaler output shows superior dynamic range when compared with the fundamental output measurements, but at a divide ratio of 128, the prescaler output shows a degraded output noise floor compared with the fundamental. Noise-floor measurements using a divider ratio of 128 require an additional 18 dB of dynamic range (compared with a divide ratio of 16) in order to avoid any degradation and this must be present in both the implemented circuits and in the measurement equipment.

The results in Fig. 14 demonstrate that while the in-band phase noise of the PLL scales appropriately with the changing divide ratio (approximately 18 dB when changing from divide ratios of 128 to 16), the in-band performance does not track the phase noise of the reference signal. This is especially evident at low offset frequencies where the difference between the measured PLL phase noise and the reference phase noise is as large as 25 dB for the divide-by-128 case at 1 kHz offset. Only in the case of the divide-by-16 result at 100 kHz offset does the measured PLL phase noise come within a few dBc/Hz of the scaled reference frequency phase noise characteristic. This observation indicates that there are dominant sources of noise that limit the

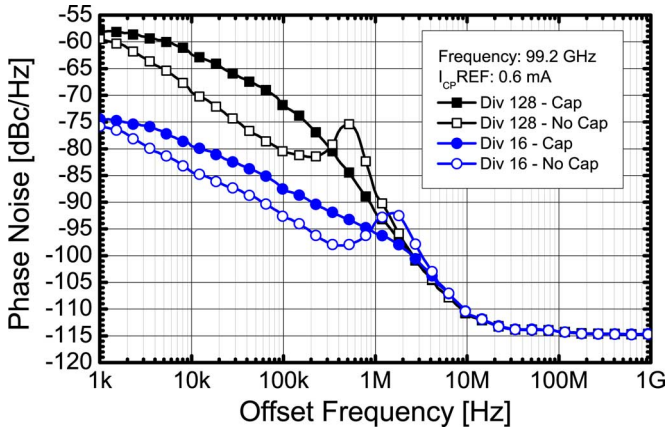

Fig. 15. Measured PLL phase noise at 99.2 GHz for divider ratios of /16 and /128, with and without added external loop capacitance.

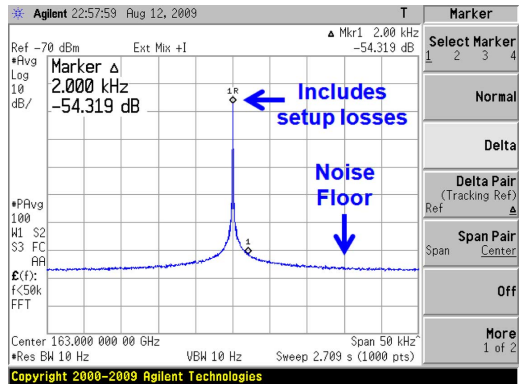

Fig. 16. Measured phase noise of the PLL at 163 GHz and /16 divider ratio.

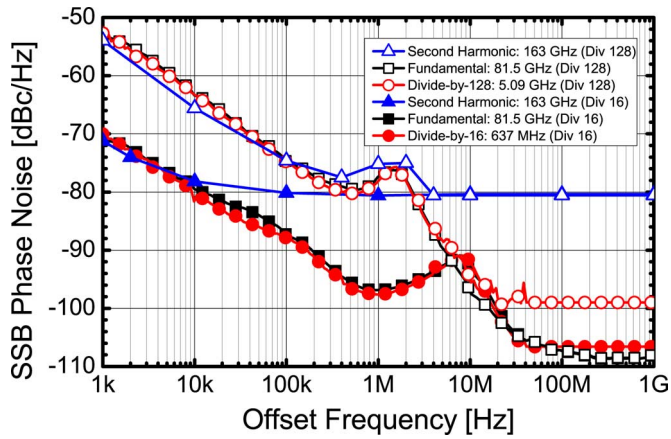

Fig. 17. Measured PLL phase noise at 163 GHz (square) for divider ratios of /16 (closed symbols) and /128 (open symbols). Measurements at the fundamental (triangle) and final division output (circle) are also shown, multiplied to the second harmonic frequency according to the frequency ratio.

in-band PLL performance other than that of the reference noise. Simulations in Fig. 11 suggest that noise from the buffer paths connecting the prescaler and off-chip reference to the PFD contribute significant noise, especially when operating with a divide ratio of 128, and these measurements reinforce those conclusions. Large-signal noise analysis in SpectreRF indicates that the low-frequency noise is mainly due to the flicker noise of p-MOSFETs in the DC bias network. The latter is a clear area of improvement for this circuit and emphasizes the importance of replacing p-MOSFETs with PNPs when good phase-noise performance is required at small offset frequencies.

The impact of varying the loop-filter capacitance is demonstrated in Fig. 15, with off-chip capacitance added to the filter by applying a DC probe to the east-side pads in Fig. 13. The built-in, DC-filtering capacitors of the probe (120 pF at the probe tip and 0.1 μF additional capacitance farther from the probe tip) increase the capacitance value in the loop filter. This added capacitance leads to the reduction of the loop bandwidth and elimination of peaking, but also results in higher noise at lower offset frequencies because of the increased noise contribution from the VCO, as well as the likely coupling of ambient noise through the DC connecting cables and the probe. Although the in-band noise is raised by as much as 5 dB, specifically between 10 and 100 kHz, the overall impact is beneficial due to the elimination of the higher frequency peaking.

The measured signal power at the second harmonic and at the fundamental outputs is approximately -3 dBm at 80/90 GHz, and -25 dBm at 163 GHz, after de-embedding measurement setup losses.

Fig. 16 is a screen-capture of the measured spectrum at the second-harmonic output of the push-push VCO at 163 GHz. The large losses of the D-band harmonic mixer employed in the PSA setup, and the low output power of the VCO results in the phase noise of the PLL rapidly reaching the measurement noise-floor at small offset frequencies. Fig. 17 shows a measurement noise-floor of approximately -80 dBc/Hz which is reached at less than 100 kHz offset for a divider ratio of 16, and at a few MHz offset with a divide-by-128 ratio. The phase noise data measured at the fundamental frequency and at the final prescaler output have been multiplied to the second-harmonic frequency of 163 GHz and can be seen to be consistent with the second-harmonic data. These results indicate that, at 163 GHz, the phase noise is better than -85 dBc/Hz and -95 dBc/Hz at 100 kHz and 1 MHz offset frequencies for a divide ratio of 16, and -75 dBc/Hz and -78 dBc/Hz at 100 kHz and 1 MHz, respectively, for a divide ratio of 128.

The PLL loop bandwidth was adjusted, by varying the charge-pump current, from 1.7 MHz to 8.5 MHz, and from 0.5 MHz to 1.9 MHz for /16 and /128 divider ratios, respectively. Fig. 18 illustrates the measured PLL phase noise at 81.5 GHz with a divider ratio of 16 for two different charge-pump currents (0.1 and 0.5 mA), resulting in a PLL bandwidth change of approximately 5 MHz.

Fig. 19 plots the measured integrated RMS phase-error of the PLL across multiple center frequencies, for divider ratios of 16 (solid symbols) and 128 (open symbols). The RMS phase error was integrated from 1 MHz to 1 GHz. The data up to 85 GHz was collected using the push-push oscillator, with scaled results for the second-harmonic output being two times larger than those shown in the figure. The results around 90 GHz and 100 GHz were obtained using the fundamental frequency Colpitts oscillator. For both divider ratios, there is a visible trend towards lower RMS phase error at higher frequencies, with the best results, around 4.5° for divide-by-16 and 6° for divide-by-128, occurring around 100 GHz. Measurements of the output

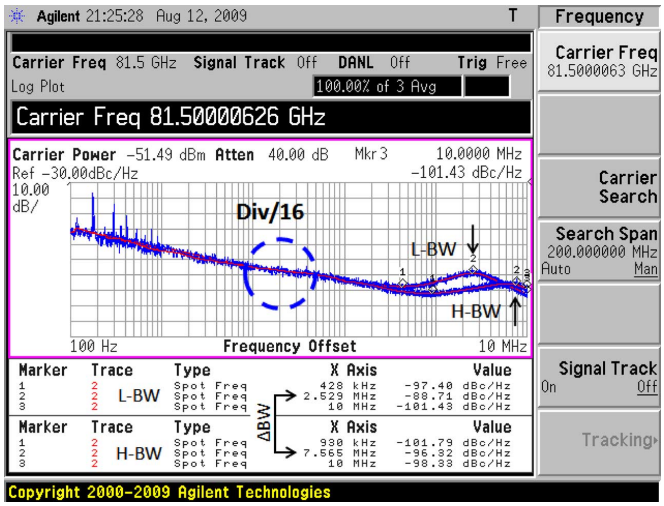

Fig. 18. Measured phase noise of the PLL at 81.5 GHz and with /16 divide ratio for two different charge-pump currents. The low-bandwidth result was produced using a 0.1 mA charge-pump current, and the high bandwidth with 0.5 mA.

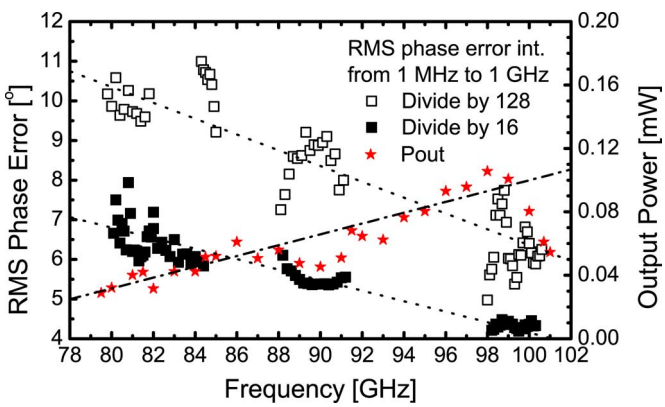

Fig. 19. Measured integrated RMS phase error of the PLL at various frequencies for both divide by 16 (closed symbols) and divide by 128 (open symbols). Integration was carried out from 1 MHz to 1 GHz. The measured output power versus frequency is shown as stars.

power without de-embedding the setup losses, shown as stars in Fig. 18, indicate a steady increase in output power at higher frequencies. The higher output power improves the measured noise floor in the 100 MHz to 1 GHz range, which contributes significant phase error to the overall integrated RMS value, especially when using a divider ratio of 16.

The measured PLL phase noise is compared with simulation in Fig. 20. For these results at 80 GHz, simulations were carried out using a nominal K_{VCO} of 2.5 GHz/V, a VCO phase noise of -95 dBc/Hz at 1 MHz offset, and a VCO noise-floor of -120 dBc/Hz above 10 MHz. Both measurements and simulations used a charge-pump current of 0.7 mA, and no external loop-filter capacitors were employed. The simulation results track the measured PLL phase-noise within 5 dB or better at most offset frequencies, except near the loop-bandwidth, where simulation predicts higher peaking than was observed in measurement.

Finally, an investigation was conducted into reducing the noise contributions of the low-frequency buffers, which was observed in simulation, and later confirmed in measurement.

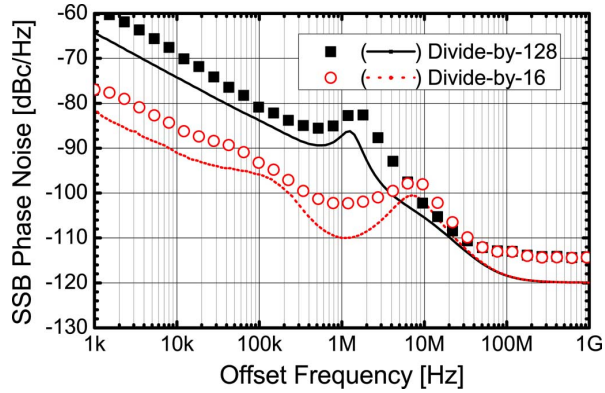

Fig. 20. A comparison of measured (symbols) and simulated (lines) PLL phase noise at 80 GHz for both divide by 16 and 128 cases.

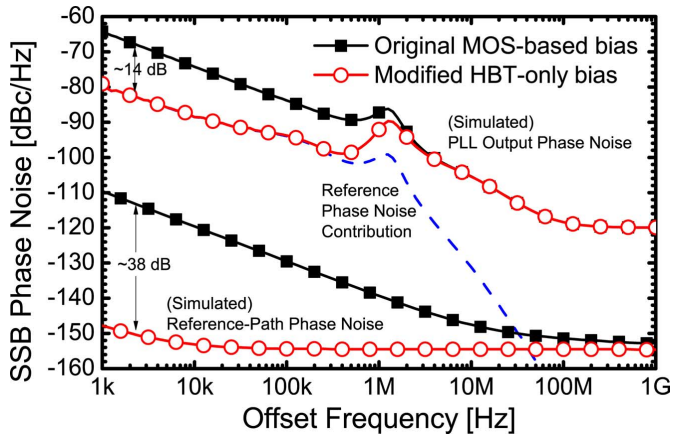

Fig. 21. Simulated PLL phase noise at 80 GHz with a divider ratio of 128, before and after modifying the bias network (top). Simulations of the phase-noise of the input buffer chain before and after modifying the bias are also shown (bottom).

The buffers, which connect the off-chip reference and the prescaler to the PFD, show large 1/f phase-noise contributions when simulated using the large-signal SpectreRF PSS/PNOISE simulator. In Fig. 21, the phase noise of the buffer chain is shown in the lower part of the plot, with square solid symbols. The corresponding phase noise of the PLL (at a divide ratio of 128) with these buffers is shown in the upper part of the figure using the same symbols. The PNOISE results indicate that the majority of noise is produced by the MOSFETs in the bias distribution network. Replacing it with an HBT-based bias circuit eliminates the 1/f noise, reducing the simulated phase-noise of the buffers by about 38 dB at 1 kHz offset, as shown with open circles. As a result, the overall PLL phase noise is reduced by about 14 dB, and is now limited by the phase noise of the reference signal source (shown as a dashed line).

V. Conclusion

In this paper, we have studied the design considerations and experimental phase noise performance limitations of PLLs scaled up in frequency to 160 GHz, as needed for future imaging, industrial sensor, and high-data-rate radio applications in the D-band. A dual W- and D-band PLL with adjustable loop

TABLE I
PERFORMANCE SUMMARY OF THE PLL WITH A DIVIDE BY 16 RATIO, AND NO EXTERNAL CAPACITORS, USING THE FUNDAMENTAL FREQUENCY VCO AROUND 90 AND 100 GHZ, AND FOR THE PUSH-PUSH VCO AT 81.3 (162.6) GHZ AND 84.4 (168.8) GHZ

Offset Frequency	90 GHz (fundamental)	100.2 GHz (fundamental)	81.3 GHz (162.6 GHz) (push-push)	84.4 GHz (168.8 GHz) (push-push)
100 kHz [dBc/Hz]	-93	-91	-93.5 (-87.5)	-91 (-85)
1 MHz [dBc/Hz]	-100	-96.5	-103 (-97)	-97 (-91)
10 MHz [dBc/Hz]	-105	-110	-99.7 (-93.7)	-102 (-96)
Integrated RMS Phase Error	5.4 °	4.3 °	6.0 ° (12 °)	5.8 ° (11.6 °)
Integrated RMS Jitter	166 fs	119 fs	204 fs (408 fs)	192 fs (384 fs)

The numbers in brackets represent the multiplied results at the second harmonic based on the fundamental frequency measurements. Integrated RMS phase and jitter values are calculated over an offset frequency range of 1 MHz to 1 GHz.

TABLE II
COMPARISON TABLE OF THE STATE-OF-THE-ART REPORTED PLLS

	[13]	[15]	[17]	[19]	[24]	This Work
Frequency	45.9-50.5GHz 91.8-101GHz	15.95 – 18.81 GHz (Tripled to 47.85 – 56.43 GHz)	73.4-73.7GHz	95.1- 96.5GHz	79.4GHz	**80-100GHz 160-169GHz**
Divide Ratio	/512	/(56.5 – 64)	/32	/256	/64	**/16, /32, /64, /128**
Phase Noise (dBc/Hz) @100kHz	-63.5 @ 50GHz [3]	-84 @ 52.29 GHz****	-88 @ 73.5GHz	N/A	-81 @ 79.4GHz	**-93 @ 90 GHz [1] -87.5 @ 162.6 GHz [1]**
Phase Noise (dBc/Hz) @1MHz	-72 @ 50GHz	-91 @ 52.29 GHz [4]	N/A	-75.2 @ 96GHz	-86 @ 79.4GHz	**-100 @ 90 GHz [1] -97 @ 162.6 GHz [1]**
RMS Phase Error (1 MHz to 1 GHz)	Not reported	2.4° @ 52.29 GHz [4]	9.9 @ 73.7 GHz[5]	Not reported	Not reported	**4.3° @ 100.2 GHz**
Output Power (dBm)	-10 @ 50GHz -22 @ 100GHz	-7.6 to -4.4 dBm @ 16 – 19 GHz	N/A	-26.8 @ 96GHz	N/A	**-3 @ 90GHz -25 @ 163GHz**
Supply	1.5V	1.2 V, 2.7 V	1.45V	1.2V, 1.3V	5.5V	**1.8V, 2.5V, 3.3V**
Power Consumption	57mW	144 mW	88mW [2]	43.7mW	N/A	**1.15W to 1.25W**
Technology	0.13µm CMOS	0.13µm SiGe BiCMOS	90nm CMOS	65nm CMOS	SiGe	**0.13µm SiGe BiCMOS**
Chip Area	1.1 mm x 0.75mm	0.68 mm x 1 mm	1mm x 0.8mm	1mm x 0.7mm	N/A	**1.1mm x 1.7mm**

[1] Using /16 divide ratio, no external capacitors. [2] Not including output buffers. [3] Measured at 50 kHz offset.
[4] Predicted results based on factor of 3 or 9.5 dB degradation from the tripler.
[5] Scaled from measurement at 36.85 GHz, and integrated from 10 kHz to 10 MHz.

parameters and programmable reference frequency was designed and fabricated in a 130-nm SiGe BiCMOS process and used as a test vehicle. Locking of the PLL was demonstrated from 80 to 100 GHz at the fundamental frequency, and from 160 to 169 GHz at the second harmonic output.

The impact of (i) the choice of reference frequency, (ii) the phase noise of the reference signal source, and (iii) the noise contributions of the loop-parameters and (iv) of the circuit building blocks to the overall phase noise of the PLL, inside and outside the loop bandwidth, were investigated using large-signal periodic-steady-state noise simulations and systematic phase-noise measurements collected simultaneously at the low-frequency (0.6–6 GHz), 40 GHz, W-band and D-band outputs of the PLL. It was determined that test equipment itself and the output power of the VCO buffers can raise the noise floor outside the loop bandwidth and limit phase-noise performance at large frequency offsets. This region is of particular significance for multi-gigabit data-rate wireless systems. At the same time, simulations, which closely track phase-noise measurements, indicate that the 1/f noise of the p-MOSFETs in the bias network of the buffers placed on the reference signal path in front of the phase-frequency detector is the dominant contributor to in-band PLL phase noise when large division ratios of 128 are employed. However, this in-band noise can be

eliminated or significantly reduced by replacing the p-MOSFETs with PNP bipolar transistors or by employing a smaller division ratio and a higher frequency reference signal.

The phase-noise performance of the PLL at various frequencies is summarized in Table I. To the best of the authors' knowledge, this PLL achieves the highest frequency of operation and the lowest phase noise of all fully integrated PLLs operating above 60 GHz to date. A comparison of this PLL to the state-of-the-art is provided in Table II, demonstrating leading phase-noise and integrated RMS phase error results, similar to those of a 17–18 GHz PLL fabricated in a comparable SiGe BiCMOS process.

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