# A D-Band PLL Covering the 81-82 GHz, 86-92 GHz and 162-164 GHz Bands

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***Abstract* — This paper describes the highest frequency PLL reported to date. It achieves the widest locking range and the lowest phase noise of -93.8 dBc/Hz at 90 GHz and 78.9 dBc/Hz at 163 GHz, both measured at a 100-kHz offset. The PLL was fabricated in a 0.13-µm SiGe BiCMOS process and covers the 81-82 GHz, 86-92 GHz, and 162-164 GHz bands. It integrates on a single die a fundamental-frequency 86-92 GHz Colpitts VCO, a differential push-push 160-GHz Colpitts VCO with quadrature outputs at 80 GHz, a programmable divider chain, charge-pump, and all loop filter components. The single-ended PLL output power is -3 dBm at 90 GHz and -25 dBm at 164 GHz and consumes 1.25 W from 1.8-V, 2.5-V and 3.3-V supplies. The chip occupies 1.1mm x 1.7mm including pads.**

***Index Terms* — Charge pump, loop filter, mm-wave, phase-locked loop, VCO, 160-GHz ICs, SiGe BiCMOS.**

## I. Introduction

Several W-band and D-Band transceivers have been recently demonstrated in SiGe BiCMOS and CMOS technologies for a variety of radar sensor [1, 2], imaging [3, 4], radio [2] and serial 107-Gb/s Ethernet [5] applications. In all these applications, a low-noise phase-locked loop (PLL) is either mandatory or desirable.

Although mm-wave silicon PLLs have recently been reported [6, 7, 8, 9], none of them operate above 100 GHz and none of the fully integrated PLLs meet the automotive radar requirements of < -80 dBc/Hz phase noise at 100-kHz offset. This work demonstrates the first D-band PLL in silicon and investigates its phase noise performance for different reference frequencies ranging from 600 MHz to 6 GHz and for PLL bandwidths between several hundred kilo-Hertz and several mega-Hertz.

## II. PLL Architecture and Circuit Design

As illustrated in Fig. 1, the PLL is equipped with two VCOs, a fundamental 90-GHz Colpitts VCO and a push-push Colpitts VCO with simultaneous quadrature outputs at 80 GHz and differential outputs at 160 GHz [4]. A mm-wave selector chooses the desired VCO signal and is proceeded by the LO distribution. The PLL prescaler comprises a Miller stage [10] followed by seven static frequency divider stages which enable a selectable divide ratio of 16, 32, 64, or 128. The divider output and the reference frequency signal are fed into a phase-frequency detector (PFD) followed by a second-order loop filter (LF) whose output is directly connected to the varactor control nodes of both VCOs. All signals are differential.

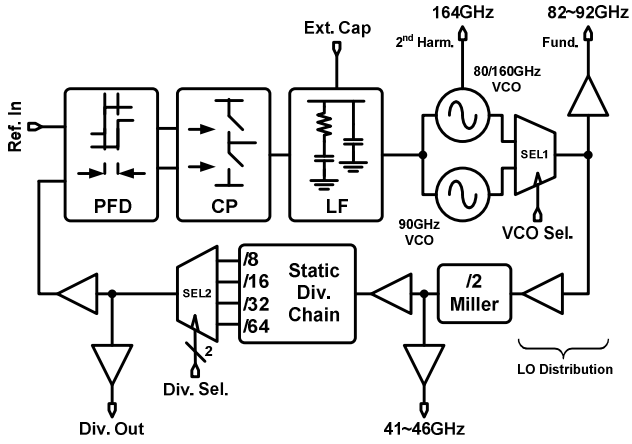


**Fig. 1:** PLL block diagram.

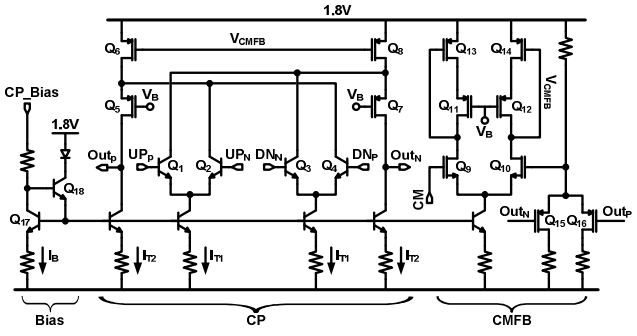


**Fig. 2:** Charge pump schematic.

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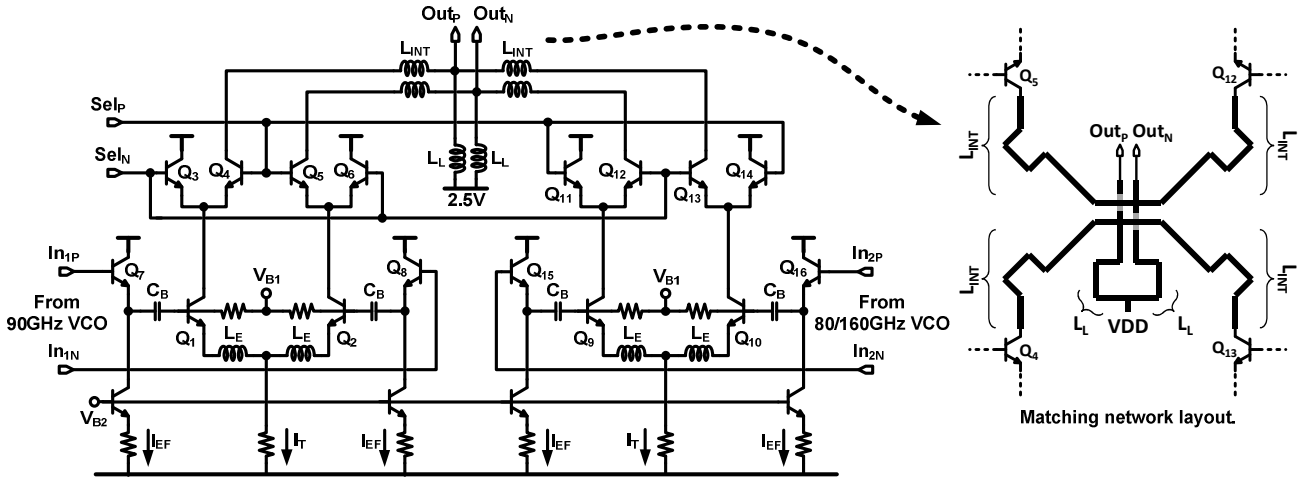


**Fig. 3:** Schematic and critical layout path of the mm-wave VCO selector.

### *A. Charge Pump*

The charge pump (CP) is implemented using a BiCMOS differential folded-cascode opamp (Fig. 2) with SiGe HBT inputs and common gate 0.13-µm PMOSFETs. A common-mode feedback (CMFB) circuit is used to match the common-mode level of the CP to the VCO common-mode tank voltage. The charge pump tail current can be adjusted externally from 70 µA to 700 µA to vary the PLL bandwidth. The integrated loop filter consists of a pair of 180-pF capacitors, 500-Ω resistors, and 40-pF dampening capacitors.

### *B. mm-Wave VCO Selector*

Fig. 3 shows the schematic of the mm-wave selector. Each half-circuit consists of a pair of emitter-followers ($Q_{7\text{-}8}$) and a variable gain amplifier ($Q_{1\text{-}6}$). $Sel_P$ and $Sel_N$ select the desired VCO signal. The layout arrangement of the matching network ($L_{INT}$ and $L_L$) at the output of the selector is sketched in Fig. 3.

The LO distribution amplifiers employ the same half-circuit as the selector, but without current steering transistors $Q_3$ and $Q_6$.

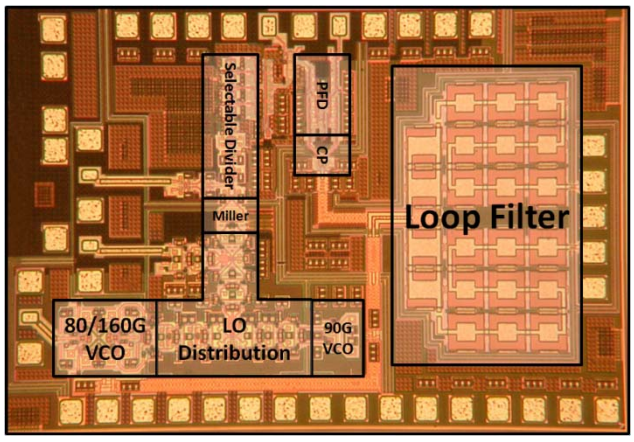


**Fig. 4:** Die photo of the PLL.

## III. Fabrication

The circuit was fabricated in STMicroelectronics' 0.13-µm SiGe BiCMOS process with HBT $f_T$ and $f_{MAX}$ of 230 GHz and 280 GHz, respectively. All critical circuit blocks (i.e. CP, LF, VCOs and LO distribution) use separate power supplies and are surrounded by deep n-well isolation and stacked metal shields (M1 to M6). The photo of the 1.1mm x 1.7mm die is shown in Fig. 4.

## IV. Measurement Results

The PLL operates from a 2.5-V supply except for the charge pump and the 80/160 GHz quadrature VCO which use 1.8 V, and 3.3 V, respectively. The total power consumption is 1.15 W or 1.25 W depending if the 90-GHz or the 160-GHz VCO is activated. The LO distribution, 90-GHz and 80/160-GHz VCOs consume 600 mW, 125 mW, and 225 mW respectively. The remaining power is dissipated in the divider chain, charge pump and output drivers.

The PLL locking range is from 86 GHz to 92 GHz for the first VCO, and 81 GHz to 82 GHz, as well as 162 GHz to 164 GHz, for the push-push VCO. An Agilent E8257D signal source is used as a reference signal and an Agilent

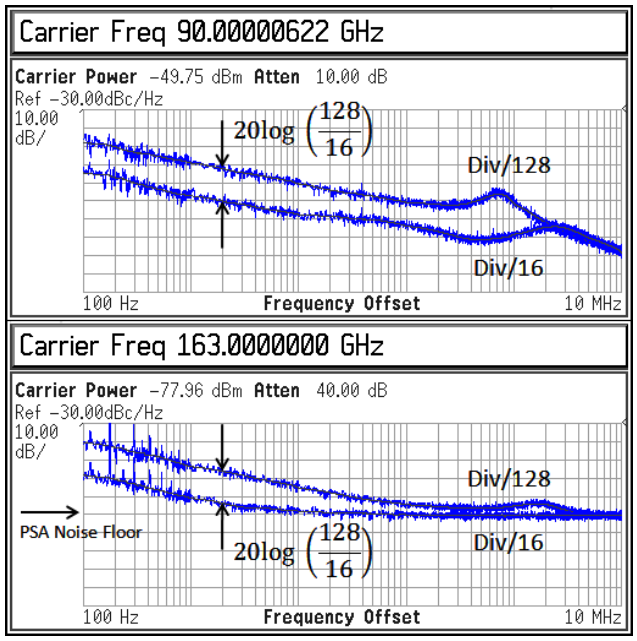


**Fig. 5:** *(Top)* Measured PLL phase noise at 90 GHz for divider ratios of /16 and /128. *(Bottom)* Measured PLL phase noise at 163 GHz for divider ratios of /16 and /128.

E4448A PSA, equipped with phase noise personality software, is employed to conduct phase noise measurements. The phase noise of the reference signal is approximately constant (-120 dBc/Hz at 100-kHz offset) between 600 MHz and 6 GHz. Therefore, by selecting different divider ratios in the prescaler, the phase noise variation can be observed to track the reference frequency.

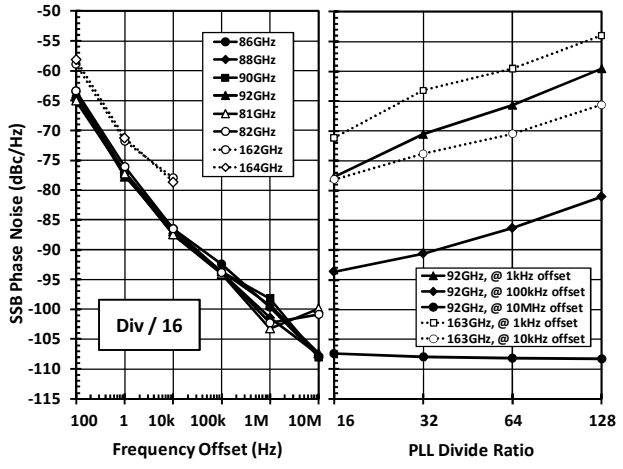


**Fig. 6:** *(Left)* Measured phase noise of the PLL at various frequencies versus frequency offset. *(Right)* Measured phase noise of the PLL at 92 GHz and 163 GHz and at various offsets versus the PLL divide ratio.

Fig. 5 shows the measured phase noise of the PLL at 90 GHz and at 163 GHz.

The single-ended PLL output power is -3 dBm at 90 GHz and -25 dBm at 163 GHz. At 90 GHz, the PLL achieves a phase noise better than -81 dBc/Hz at 100-kHz offset for all divider ratios. At 163 GHz, due to the large losses of the external mixer and the low VCO signal power, the phase noise of the PLL corresponding to the /16 divide ratio is below the noise floor of the PSA for offsets greater than 3-kHz. However, with divide-by-32 ratio the measured phase noise rises above the setup noise floor and is -78.9 dBc/Hz at 100-kHz offset. Furthermore, Fig. 6 shows the measured phase noise of the PLL at various frequencies, offsets and divider ratios. It can be observed that the phase noise is approximately constant for each VCO throughout its entire locking range and that doubling the divider ratio degrades the PLL phase noise by the theoretical 6 dBc/Hz value. The in-band phase noise of the PLL is dominated by the reference signal. This suggests that the PLL phase noise may be improved by using a reference oscillator with better phase noise characteristics.

To investigate the effect of the PLL divider ratio on phase noise, the charge pump current is kept constant for measurements shown in Fig. 5. This causes the PLL loop bandwidth to decrease for higher divider ratios. Furthermore, by adjusting the charge pump current, the loop bandwidth of the PLL at 90 GHz can be varied from 0.54 MHz to 1.72 MHz, and from 1.72 MHz to 5.4 MHz for /16 and /128 divider ratios, respectively. Similar results were also obtained using the 80/160-GHz VCO. Fig. 7 shows the measured PLL phase noise at 81.5 GHz

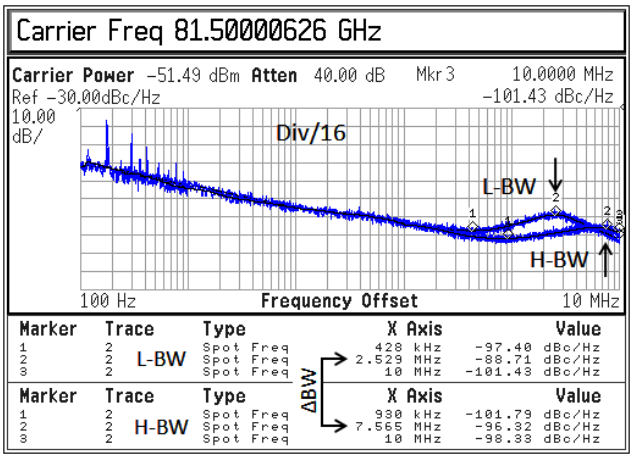


**Fig. 7:** Measured phase noise of the PLL at 81.5 GHz and with /16 divide ratio for two different PLL bandwidths.

**Table 1:** Comparison table of the state-of-the-art PLLs.

| | [6] | [7] | [8] | [9] | This Work |
|---|---|---|---|---|---|
| **Frequency** | 45.9-50.5GHz<br>91.8-101GHz | 73.4-73.7GHz | 95.1- 96.5GHz | 79.4GHz | **81-82GHz**<br>**86-92GHz**<br>**162-164GHz** |
| **Divide Ratio** | /512 | /32 | /256 | /64 | **/16, /32, /64, /128** |
| **Phase Noise (dBc/Hz) @100kHz** | -63.5 @ 50GHz**** | -88 @ 73.5GHz | N/A | -81 @ 79.4GHz | **-93.8 @ 90GHz*** <br>**-78.9 @ 163GHz**** |
| **Phase Noise (dBc/Hz) @1MHz** | -72 @ 50GHz | N/A | -75.2 @ 96GHz | -86 @ 79.4GHz | **-98.2 @ 90GHz*** |
| **Output Power (dBm)** | -10 @ 50GHz<br>-22 @ 100GHz | N/A | -26.8 @ 96GHz | N/A | **-3 @ 90GHz**<br>**-25 @ 163GHz** |
| **Supply** | 1.5V | 1.45V | 1.2V, 1.3V | 5.5V | **1.8V, 2.5V, 3.3V** |
| **Power Consumption** | 57mW | 88mW*** | 43.7mW | N/A | **1.15W to 1.25W** |
| **Technology** | 0.13µm CMOS | 90nm CMOS | 65nm CMOS | SiGe | **0.13µm SiGe BiCMOS** |
| **Chip Area** | 1.1 mm x 0.75mm | 1mm x 0.8mm | 1mm x 0.7mm | N/A | **1.1mm x 1.7mm** |

* Using /16 divide ratio. ** Using /32 divide ratio. *** Not including output buffers. **** Measured at 50kHz offset.

and with /16 divide ratio for two different PLL bandwidths.

## IV. Conclusions

To the best of the authors' knowledge, the PLL reported here achieves the highest frequency of operation, the largest locking range and the lowest phase noise of all PLLs operating above 60 GHz to date. A comparison of its performance to the state-of-the-art is provided in Table 1.

## Acknowledgement

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