Decision Feedback Equalizer Architectures With Multiple Continuous-Time Infinite Impulse Response Filters

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***Abstract*—Decision feedback equalizer (DFE) architectures with varying numbers of discrete-time taps and continuous-time infinite impulse response (IIR) filters are compared for use in typical wireline channels. In each case, the DFE coefficients are optimized to minimize a cost function that equally weights both jitter and vertical eye opening. Even when some reflections are present (e.g., backplane channels) continuous-time IIR taps can be effective if their filter coefficients are properly optimized. Using a DFE architecture with only *two IIR filters* provides adequate results for both a 26-dB loss coax cable and a $16''$ FR-4 backplane channel at 10 Gb/s while keeping the DFE complexity low. Furthermore, the implementation and experimental results of a DFE with multiple (three) IIR filters is reported. Fabricated in a 0.13 μm CMOS process, the DFE consumes 17.3 mW from a 1.2 V supply. A bit error rate (BER) of 10^{-12} was achieved at a data rate of 3.7 Gb/s.**

***Index Terms*—Decision feedback equalizer (DFE), equalization, infinite impulse response (IIR) DFE.**

I. Introduction

IN HIGH-SPEED wireline transceivers, a (DFE) is often used to cancel the effect of the current bit on future bits [1]. Channels whose frequency response is dominated by skin effect and/or reflections will have a long pulse response with post-cursor inter-symbol interference (ISI) extending over many symbol periods. Several attempts have been made to reduce the power consumption of conventional DFEs for these and other applications where many taps are required [2], [3]. Alternatively, a continuous-time tap can be created using an (IIR) filter in the DFE [4], [5]. This approach allows several several post-cursor ISI taps to be canceled simultaneously with reduced power consumption. The two techniques have also been combined to realize an equalizer with one discrete-time tap and one IIR filter in the DFE [6].

This work considers a generic DFE consisting of K discrete-time taps and N IIR filters as shown in Fig. 1. For the conventional discrete-time DFE, $N = 0$, and K taps are used; an example pulse response is shown in Fig. 2(a). The tap weights $(H_1, H_2, H_3, \ldots)$ are chosen to subtract the post-cursor ISI at the sampling point. It is evident that for a channel with several post-cursor ISI terms, a large number of DFE taps are required resulting in higher power consumption. In [6], $K = 1$, and $N = 1$ and the parameters H_1, B_1, and τ_1 are varied. By adjusting the three variables, a better fit to the channel pulse response is obtained. In fact, multiple IIR filters can be used to improve performance further. Using 2-IIR filters, $K = 0$ and $N = 2$, each filter's time constant (τ_1, τ_2) and gain (B_1, B_2) can be varied. By having even more degrees of freedom, once again, a better fit can be obtained to the channel pulse response. Fig. 2(b) shows the channel pulse response and the response of the two feedback filters. In this case, one filter (τ_1, B_1) is used to cancel the first few post-cursor ISI taps, while the second filter (τ_2, B_2) cancels the small residual ISI present at the end of the pulse response. In the past comparisons between IIR and discrete-time DFEs have not described how the coefficients may be optimized and the choice of architectures has been heuristic with no rigorous justification for the number of taps and filters. In this paper, these architectures are systematically compared revealing that an architecture with $N = 2$ and $K = 0$ provides an excellent combination of performance and low complexity for common wireline channels. Also, reported are the implementation and measurement of an integrated DFE incorporating more than one IIR filter.

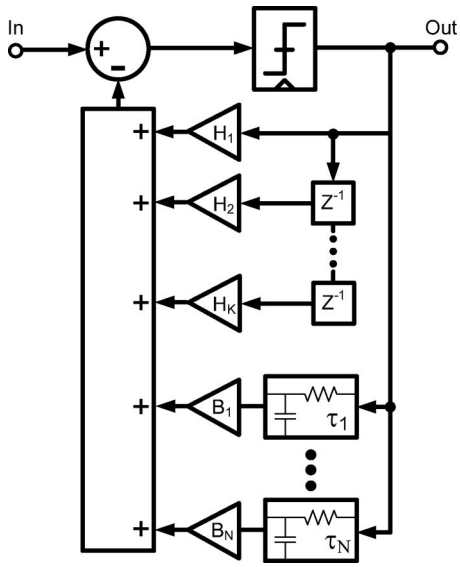

Fig. 1. Generic DFE architecture consisting of Kdiscrete-time taps and N continuous-time IIR filters.

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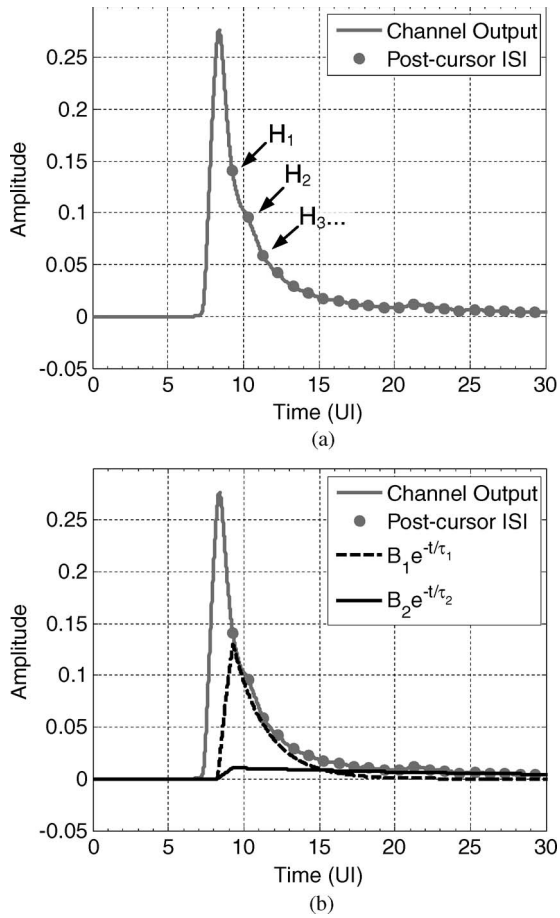


Fig. 2. Pulse response for DFEs employing different number of discrete-time taps and/or IIR filters. (a) Conventional discrete-tap DFE, $K = 10$, $N = 0$. (b) 2-IIR filter DFE, $K = 0$, $N = 2$.

II. DFE Architecture Comparison

It is evident that by increasing the degrees of freedom in a DFE, ie. increasing the number of taps or adding multiple IIR filters, the system can cancel more ISI. It would be beneficial to determine a DFE architecture providing adequate performance while keeping the system complexity as low as possible. Two things need to be considered to correctly identify the optimal DFE architecture. First, metrics need to be determined that will allow for a comparison between the different DFE architectures. Secondly, for each architecture, the DFE variables (filter time-constants, filter gains, and tap weights) need to be adjusted to obtain the best resulting metrics.

Two properties of the equalized signal can be used as metrics: *Vertical eye opening* and *jitter*. Peak-to-peak jitter here includes only deterministic jitter caused by ISI. Vertical eye opening is measured as the eye opening at the sampling point (rising edge of the clock). The negative edges of the clock are aligned to the median zero-crossing times and the sampling points are halfway between, as in an Alexander bang-bang clock recovery unit [7].

An appropriate cost function should consider both vertical and horizontal eye opening. Fig. 3 shows the channel pulse response (in grey) and the pulse response of the IIR filters in the DFE as well as the discrete-time DFE taps (in black). At the rising edges of the clock, the difference between the two pulse

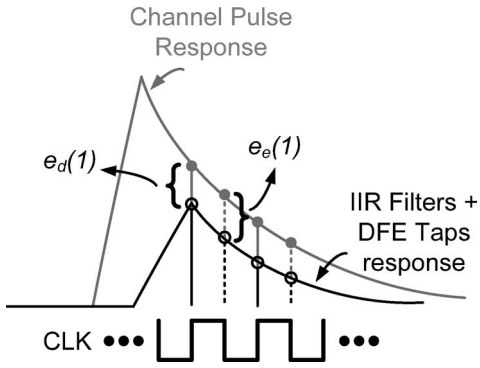


Fig. 3. Channel and DFE feedback pulse response.

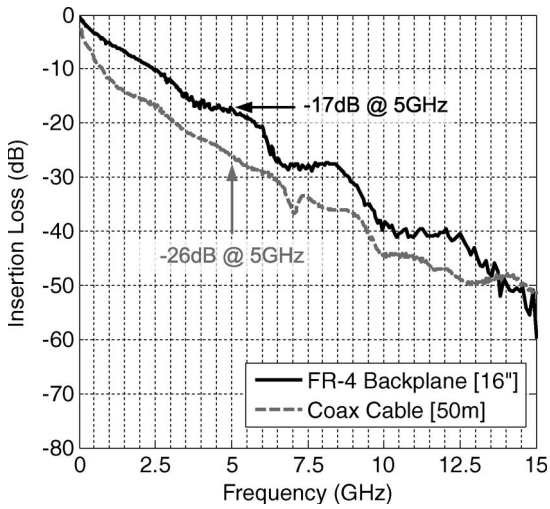


Fig. 4. Measured channel insertion loss.

responses is $e_d(i)$. This error affects the vertical eye opening at the data sampling point. At the falling edges of the clock (zero crossings of data), the difference between the pulse responses is $e_e(i)$ which determines the amount of jitter. The cost function in (1) is a weighted sum of the two errors where α and β are the weighting factors for vertical eye opening and jitter, respectively

$$Cost = \alpha \times \sum_{i=1}^{Q} |e_d(i)| + \beta \times \sum_{i=1}^{Q} |e_e(i)| \,. \qquad (1)$$

In this paper, $\alpha = \beta = 1$ giving equal priority to both vertical eye opening and jitter. Note that Q post-cursor ISI contributors are considered in the cost function (1). The value of Q can be determined by observing how many post-cursor ISI terms contribute significantly to the channel response. An upper bound to Q can also be determined from the longest number of consecutive identical digits the system needs to support. A value of $Q = 120$ was chosen for the channels of interest.

Naturally, depending on the frequency response of the channel, the amount of ISI will vary. This in turn could lead to different optimal DFE architectures for each channel. Two channels have been considered here for operation at 10 Gb/s: a 50 meter coax cable with 26 dB attenuation at 5 GHz and a 16″ FR-4 backplane channel with 17 dB attenuation at 5 GHz with the insertion loss shown in Fig. 4. In both cases, no linear equalization is assumed. For each of the channels and

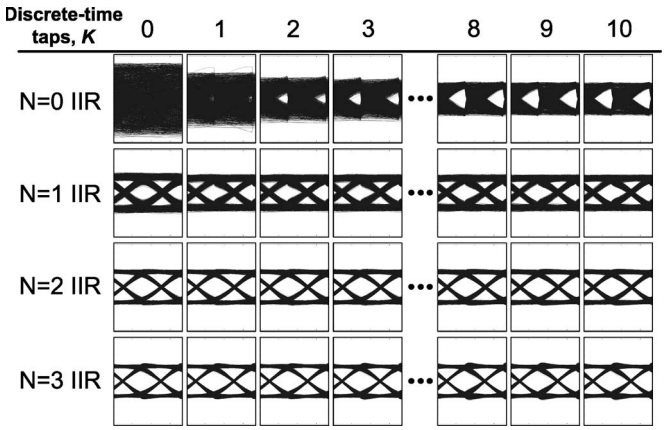


Fig. 5. Simulated eye diagrams for various DFE Architectures.

each DFE architecture, $K \in \{0 \ldots 10\}$ and $N \in \{0 \ldots 4\}$, the DFE parameters H_k, B_N, and τ_N are optimized to minimize the cost function (1) at a 10 Gb/s data rate. A constrained nonlinear minimization is performed using MATLAB's *fmincon* function [8] to determine the optimal coefficients for each DFE. The computation of DFE coefficients offline is practical only when the channel is fixed and known *a priori*.

Fig. 5 shows the resulting equalized eye diagrams for the $16''$ FR-4 backplane channel. For each DFE configuration, the system is simulated and the vertical eye opening and jitter is measured. In Fig. 5, the first row corresponds to having a conventional discrete-time DFE with various numbers of taps (i.e., $N = 0$, $K = 0 \ldots 10$). Each subsequent row adds one IIR filter to the architecture. The measurements from each eye diagram are compiled together in Fig. 6.

Fig. 6(a) and (b) show the results for the $16''$ FR-4 backplane channel. Each curve corresponds to a certain number of IIR filters while the x-axis refers to the number of discrete-time DFE taps, K, and the y-axes plot the two metrics. It can be seen that by increasing the number of IIR filters in the DFE, N, there is a drastic improvement in both quality metrics. While, three or more IIR filters provide the best result, ***two IIR filters*** provide a nearly optimal architecture while keeping system complexity low. It is also evident that adding additional discrete-time DFE taps to the system results in minuscule improvements and can be avoided to reduce complexity.

Fig. 7(a) and (b) summarizes similar results for the 50 meter coax channel. Again it is evident that increasing the number of IIR filters and discrete-time DFE taps improves performance. Once again trying to minimize the system complexity while considering the quality metrics it is evident that ***two IIR filters*** provides a nearly optimal architecture. It should be noted that looking only at the jitter performance, Fig. 6(b), it may seem that the performance degrades when increasing the number of discrete-time taps, for example with $N = 1$ and K increasing from 0 to 1. However, the eye opening, Fig. 1, has increased, so the overall cost function improves. Table I shows the degradation in system performance when all the DFE coefficients vary from their optimal value for both the 50 meter coax cable and the $16''$ FR-4 backplane channel $(K = 0, N = 2)$.

It is interesting to compare architectures having $K = 0$, $N = 2$ and one having $K = 1$, $N = 1$. Both can be thought of as

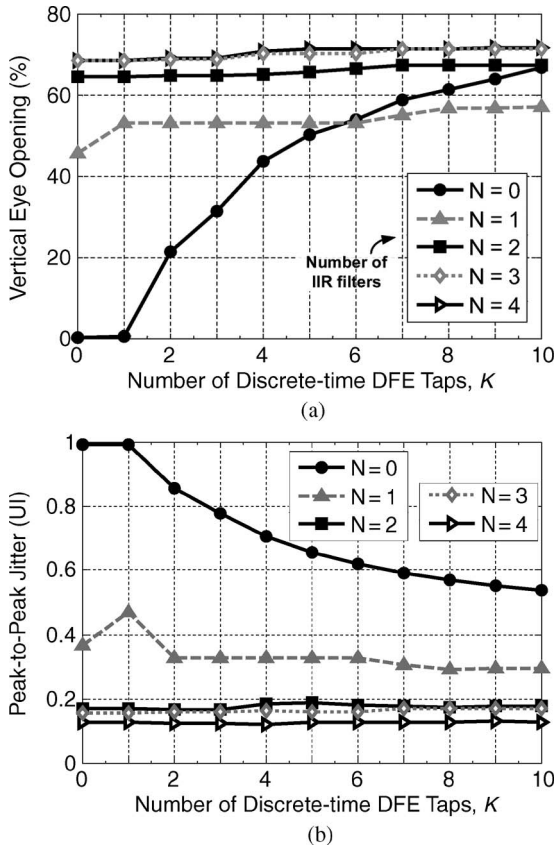


Fig. 6. Simulated DFE architectures at 10 Gb/s (FR-4 backplane channel). (a) FR-4 backplane $(16'')$ simulated vertical eye opening. (b) FR-4 backplane $(16'')$ simulated peak-to-peak jitter.

having similar hardware complexity since both require two taps into the DFE summing node (although, of course an additional passive filter is required when $N = 2$). With $K = 0$, $N = 2$, Figs. 6 and 7 illustrate a significant potential improvement in performance. However, at the highest data rates, it may become difficult to cancel the first post cursor ISI tap using only IIR filters due to delays in the feedback path. Using a discrete-time tap can alleviate the timing issues.

The adaptation of IIR filters has been extensively studied in the literature [5], [9]. Adapting the poles of IIR filters leads to local minima in a mean squared error cost function which creates challenges for any gradient descent adaptation algorithm, including the popular least mean square algorithm [10]. Solutions have been proposed to guide the adaptation of such systems [11]. Implementation of such algorithms will naturally rely upon some digital signal processing which certainly factors into the circuit's complexity.

III. Measurement Results

A chip was fabricated in a 0.13 μm CMOS process with a three IIR filter DFE (i.e., $N = 3$, $K = 0$). Three IIR filters were used to allow for equalization of a particular optical channel (not detailed here) as well as the electrical channels of present interest. A block diagram of the implementation is shown in Fig. 8. The DFE was implemented using a half-rate architecture. The clock phase for the latches can be adjusted

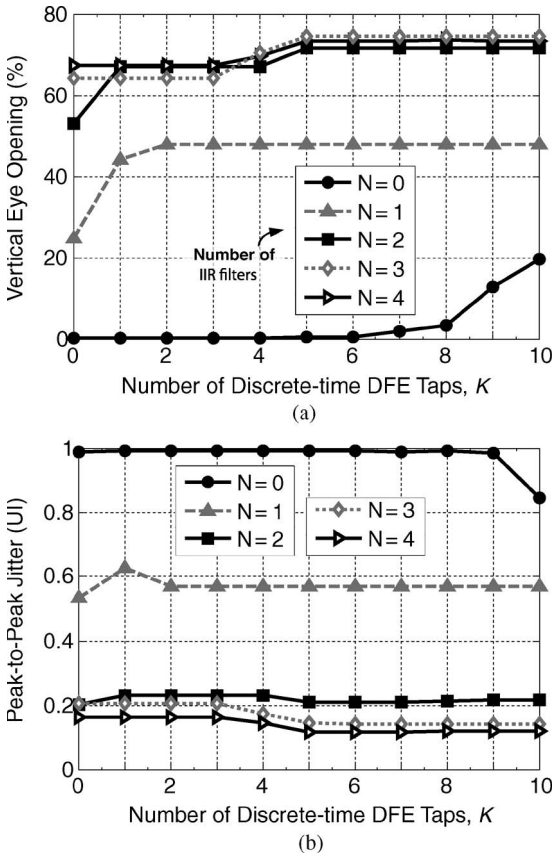


Fig. 7. Simulated DFE architectures at 10 Gb/s (coax cable). (a) Coax cable (50 m) simulated vertical eye opening. (b) Coax cable (50 m) simulated peak-to-peak jitter.

TABLE I
REDUCTION IN VERTICAL EYE OPENING AND INCREASE IN PEAK-TO-PEAK JITTER FOR VARIATIONS IN DFE COEFFICIENTS

	50 Meter Coax Cable		16" FR-4 Backplane	
Coefficient Variation	Vertical Eye Reduction	Jitter Increase	Vertical Eye Reduction	Jitter Increase
-20%	44 %	0.48 UI	26.6 %	0.1 UI
-10%	9.8 %	0.06 UI	11.8 %	0.013 UI
+10%	10.1 %	0.25 UI	12.2 %	0.08 UI
+20%	45 %	0.56 UI	28.4 %	0.17 UI

using an on chip injection locked oscillator (ILO) phase shifter which includes a selectable injection point for coarse phase control and analog tuning for fine phase control [12]. The flip-flops and the muxes are implemented using a Current Mode Logic (CML) architecture. Only one summer is required in this half-rate architecture since no discrete-time taps were used; This is in contrast with [6] which required two summation nodes along with the addition of a discrete-time tap.

The circuit implementation for the IIR filter and current mode summer is shown in Fig. 9(a). A differential pair with varactors at the output is used to tune the time-constant (τ) of the filters. Two of the varactors are implemented using an accumulation mode MOS device to achieve capacitances tunable between 800 fF and 2.5 pF as shown in Fig. 9(b). These two varactors were used to create the faster time constants for canceling the first few post-cursor ISI taps. The third tap responsible for the long tail cancellation is comprised of a

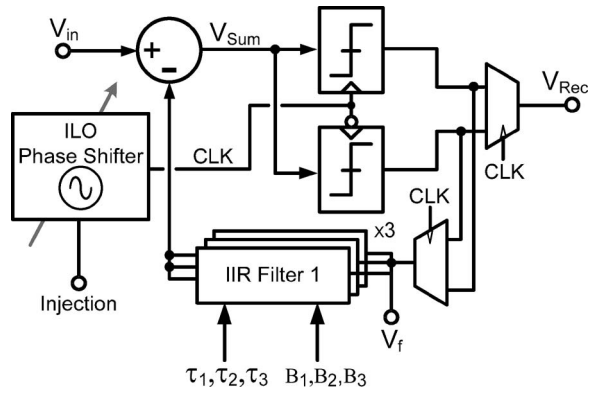


Fig. 8. Fabricated DFE/ILO block diagram.

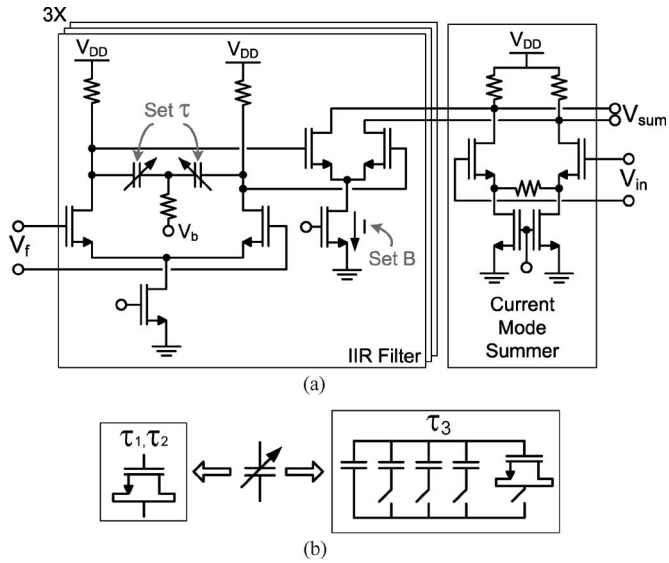


Fig. 9. DFE IIR filter and varactor implementation. (a) IIR filter and current mode summer circuit implementation. (b) Two different varactor implementations.

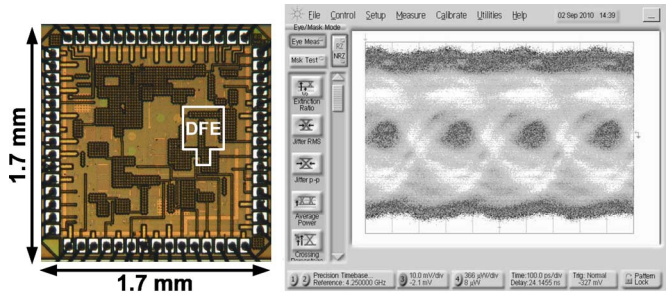
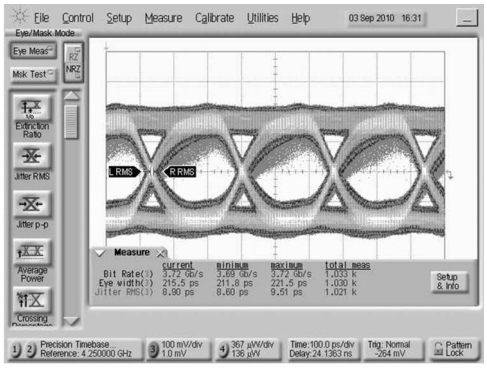
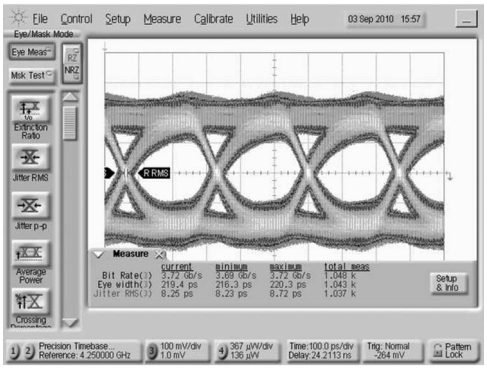


Fig. 10. Chip die photo and input eye diagram. (a) Chip die photo. (b) Measured input eye diagram.

capacitor bank. A 15 pF capacitor is permanently attached, along with 4 switches that can attach capacitors of 10 pF, 5 pF, 2.5 pF, along with the same varactor used in the other RC taps. The current in the second stage of the IIR filter can be varied to control the gain (B). The output of each of the filters is connected together to perform the summation in current mode. The die photo is shown in Fig. 10(a) and the DFE occupies 0.0535 mm^2. The DFE consumes 17.3 mW of power from a 1.2 V supply.



(a)



(b)

Fig. 11. Measured eye diagrams using 10 meter coax cable. (a) Measured 3.7 Gb/s retimed eye (DFE OFF). (b) Measured 3.7 Gb/s retimed eye (DFE ON).

Fig. 10(b) shows the input eye diagram for an input $2^7 - 1$ Pseudo Random Bit Sequence (PRBS) pattern at 3.7 Gb/s. Although it is periodic, PRBS7 data is representative of the data statistics in many real applications, such as those employing DC-balanced line codes. With an input stage approximately matched to the coax characteristic impedance, the prototype performance would match that of the system simulations. However, in order to accommodate optical channels (not described here in detail) very low input impedance was required. Hence, the prototype implementation has an input resistance of $\sim$10 Ω causing considerable mismatch when tested with the coax cable. The resulting reflections caused the input eye to be completely closed even for 8 dB of attenuation at 1.85 GHz. Regardless, the DFE can still function properly for data rates of up to 3.7 Gb/s. The recovered eye diagrams are shown in Fig. 11 with the DFE off and on. Although both eye diagrams look open, it is evident in Fig. 11(a) that the resulting recovered data will contain errors and have a low (BER).

To determine the BER of the system with the DFE OFF/ON a bit error rate tester (BERT) was used. The phase of the external clock was varied on chip using the ILO phase shifter to create the bathtub curve. The bathtub curve for a $2^7 - 1$ PRBS pattern at a data rate of 3.7 Gb/s is shown in Fig. 12. With the DFE on, the system is able to reach a target BER of 10^{-12}.

IV. Conclusion

A comparison of different DFE architectures was presented consisting of a combination of discrete-time taps and continuous-time IIR filters. The DFE coefficients were optimized for vertical eye opening and jitter using a cost function giving equal priority to both. For two typical wireline channels, *two IIR filters* provided adequate results with low system complexity. A multi-IIR filter DFE (three filters) was implemented in a 0.13 μm CMOS process and although the input eye to the system was closed, the DFE achieved error free operation for a data rate of 3.7 Gb/s. The total DFE power consumption was 17.3 mW from a 1.2 V supply.

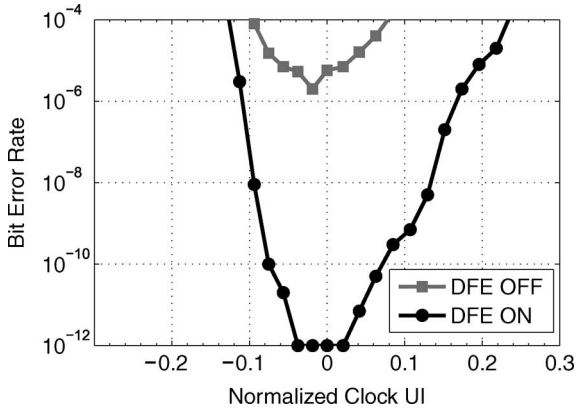


Fig. 12. Measured 3.7 Gb/s Bathtub Curve.

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