CLOCK RECOVERY IN HIGH-SPEED MULTILEVEL SERIAL LINKS

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OUTLINE

- Introduction
- Conventional CDR Methods:

    1. Linear Phase Detector based CDR

    2. Alexander Phase Detector based CDR

- SSMMSE Phase Detector based CDR
- Simulation Results
- Conclusion

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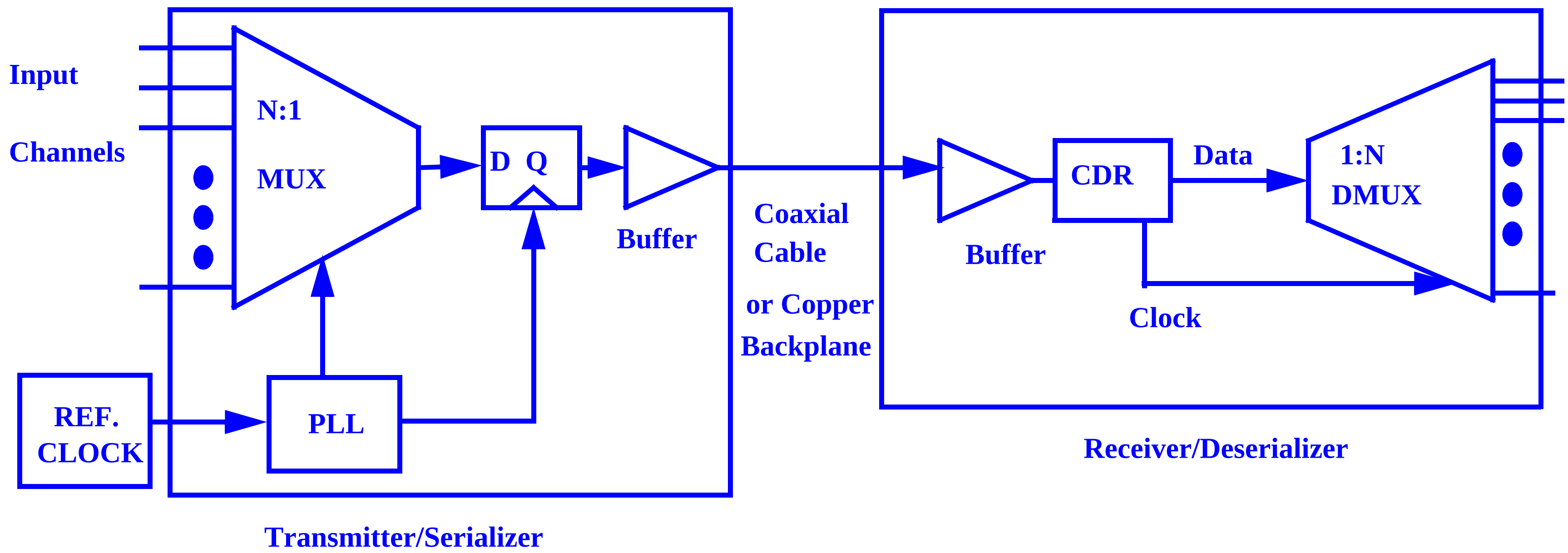
INTRODUCTION

- **Typical Serial Link**



Data Rates up to 40Gb/s

- *CDR extracts a low jitter clock from the received signal and uses it to retime the data.*

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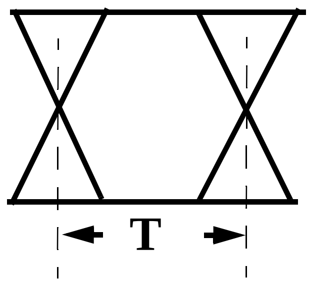
INTRODUCTION (contd.)

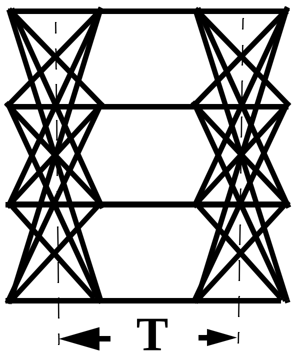
- **Challenges of increasing data rate:**
  1. Finite channel bandwidth (increased ISI)
  2. CMOS circuit speed limitations
  3. Stringent jitter requirements (1ps r.m.s. for 10Gb/s serializers and 0.25ps r.m.s. for 40Gb/s).
- **Altenative: Multilevel Signaling**

NRZ Data(1bit/symbol)



Symbol Rate=Data Rate=1/T

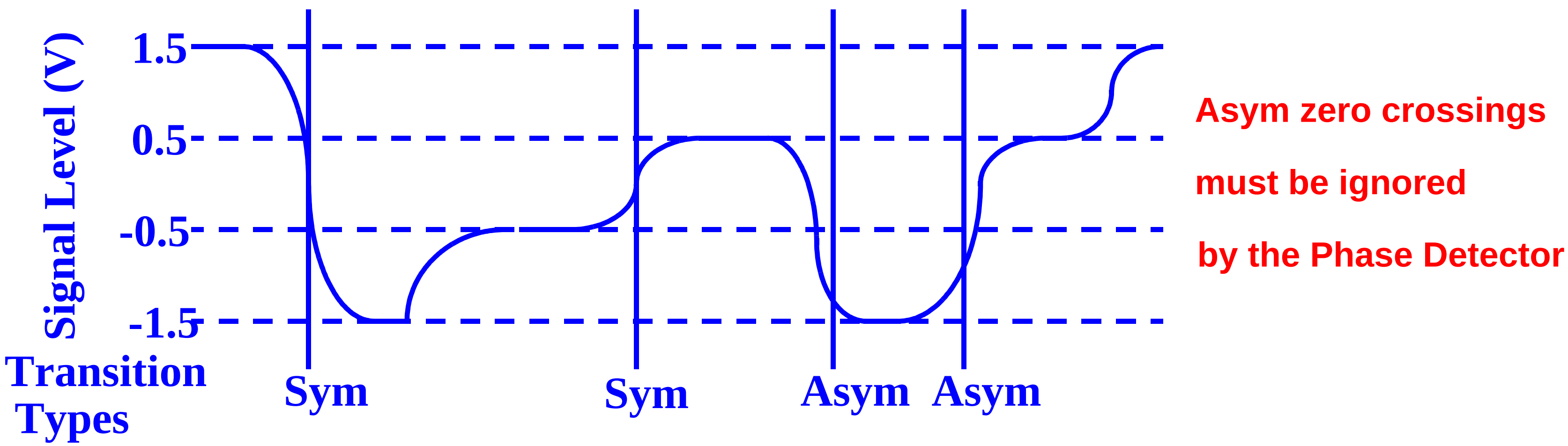
4-PAM Data (2 bits/symbol)



Symbol Rate=1/T; Data rate=2/T

CLOCK RECOVERY FROM MULTILEVEL SIGNALS

- Conventional methods use data transitions to update the sampling phase of the receiver clock.
- Multilevel signals have both symmetric and asymmetric zero crossings; thus resulting in a complicated phase detector (PD) in the CDR.



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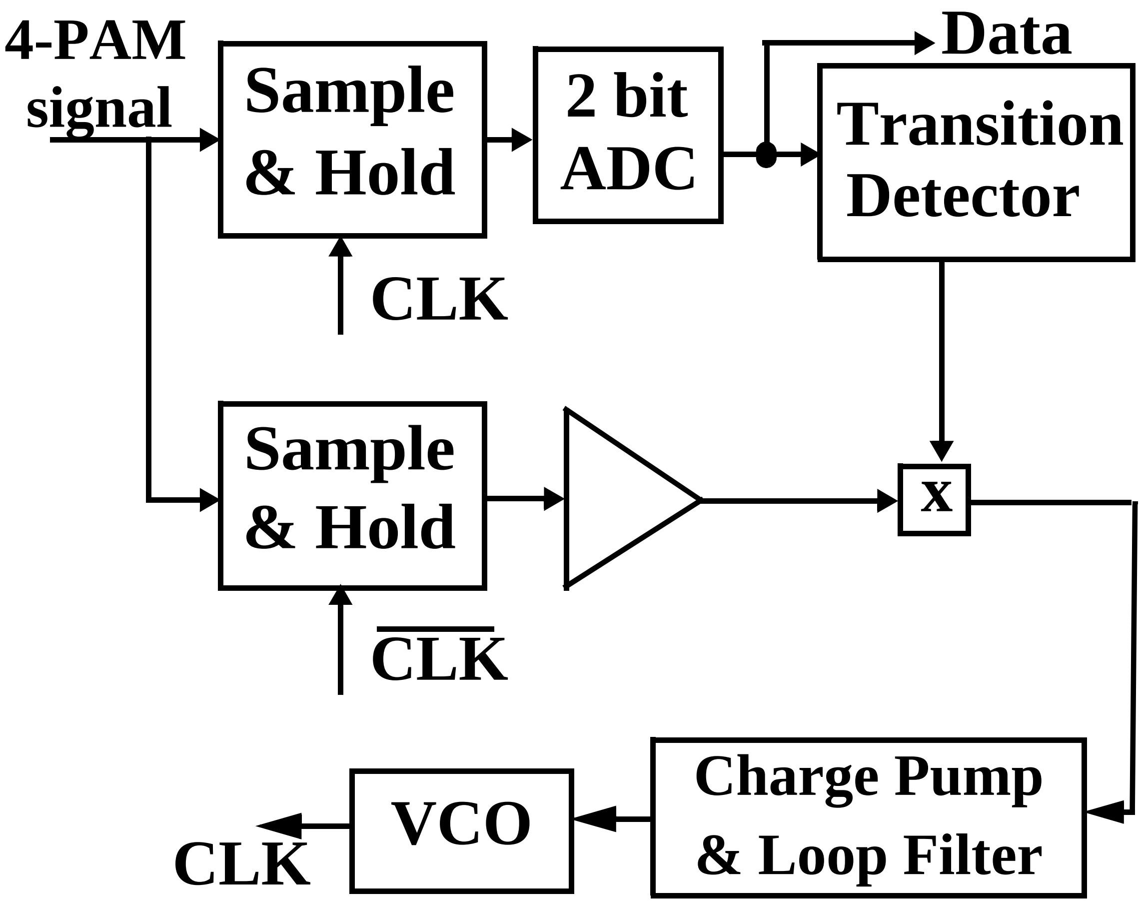
CONVENTIONAL CDR METHODS

1. Linear Phase Detector based CDR



PD produces pulses proportional to the phase error between the transition edge of the data and the clock.

Advantages:

Low Jitter

Diasadvantages:

1. *Difficult to implement at high speeds*
2. *Power hungry*
3. *Requires oversampling of the received wave-form*

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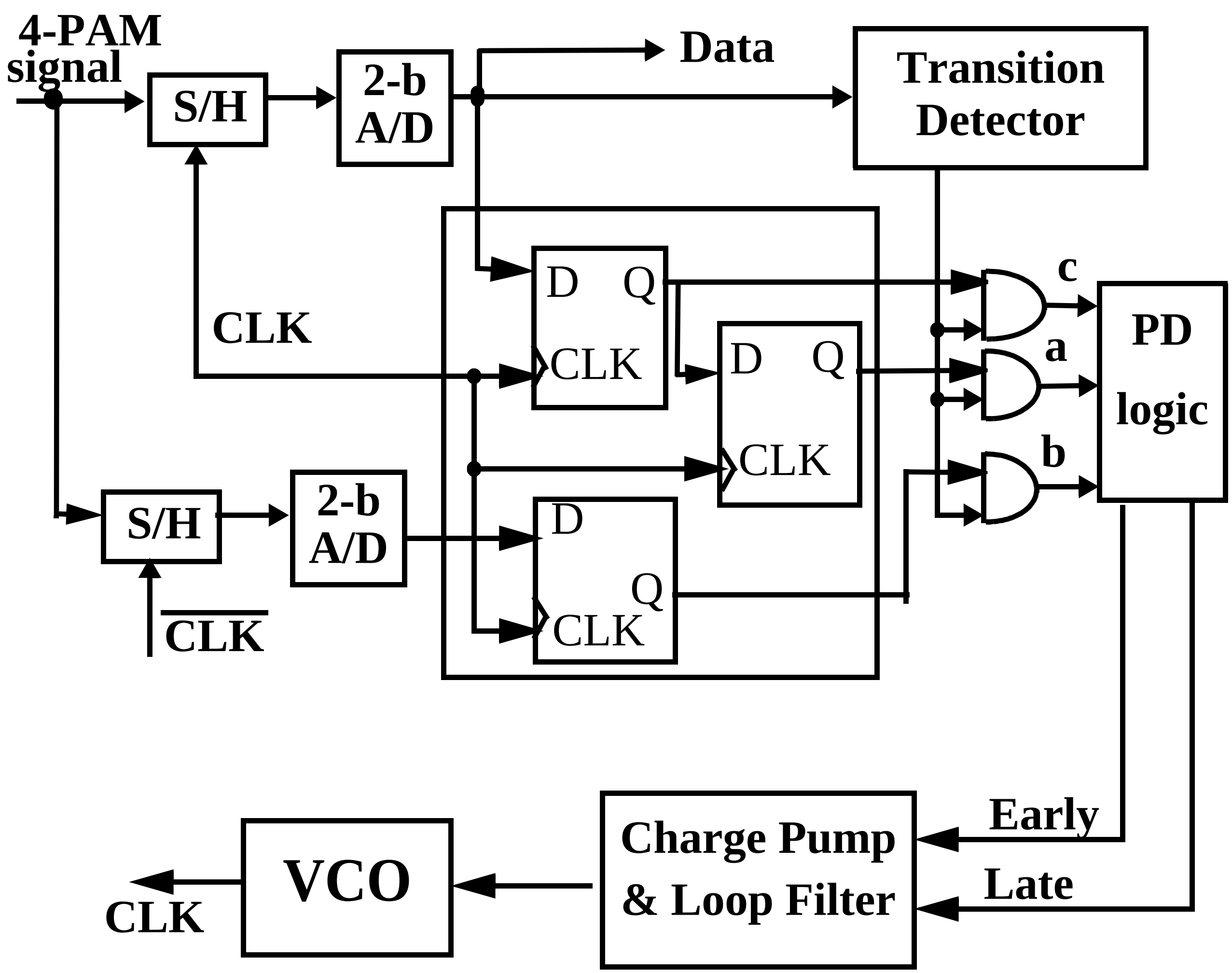
2.ALEXANDER PD BASED CDR (contd.)



Advantages:

More robust

Disadvantages:

1. Higher jitter

2. Requires over-sampling of the received wave-form

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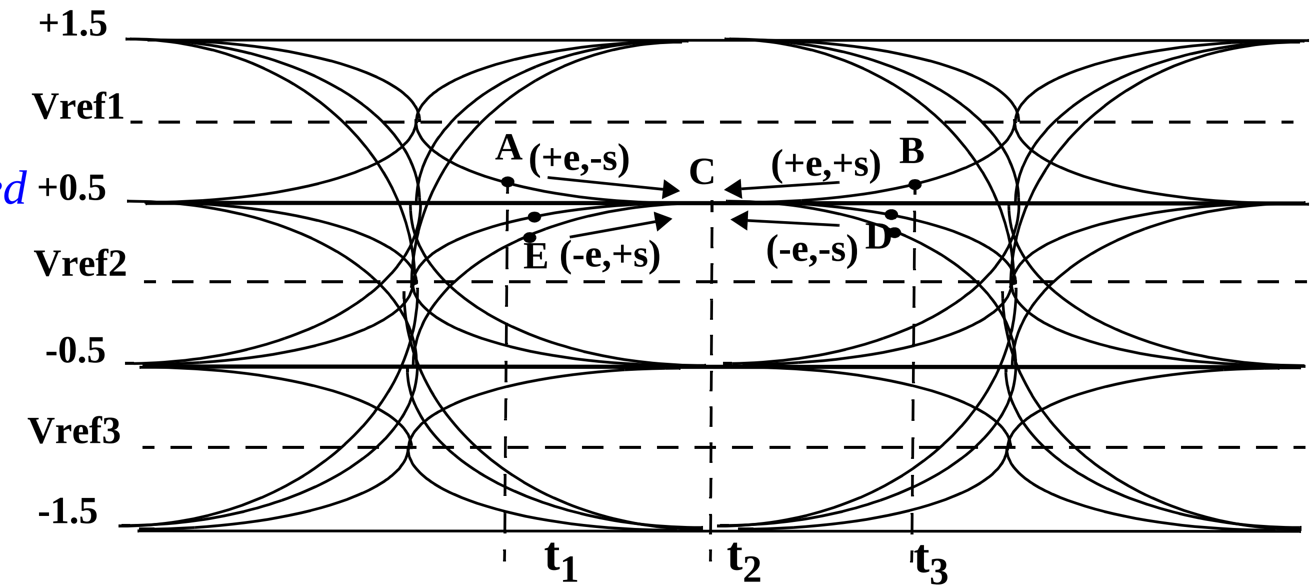
SSMMSE PD BASED CDR

- *4-PAM signal:*

Data transitions are not monitored



- *Truth Table:*

Sampling point	Error (e)	Slope (s)	Sampling Phase
A	1	0	Early
B	1	1	Late
D	0	0	Late
E	0	1	Early

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SSMMSE PD BASED CDR (contd.)

- *Based on Minimum Mean Squared Error criteria:*

$$E_k = E\left[e_k^2\right] = E\left[(A_k - y(kT + \tau_k))^2\right]............(1)$$

- *Update Rule:*

$$\tau_{k+1} = \tau_k - \mu \partial E_k / \partial \tau_k......(2)$$

- *Using an instataneous estimate for E_k:*

$$\tau_{k+1} = \tau_k + 2\mu e_k \dot{y}(kT + \tau_k)......(3)$$

- *Sign-Sign MMSE Update Rule:*

$$\tau_{k+1} = \tau_k + 2\mu \,\mathrm{sgn}[e_k]\,\mathrm{sgn}[\dot{y}(kT + \tau_k)]......(4)$$

- *SSMMSE preserves the direction but not the magnitude of the update*

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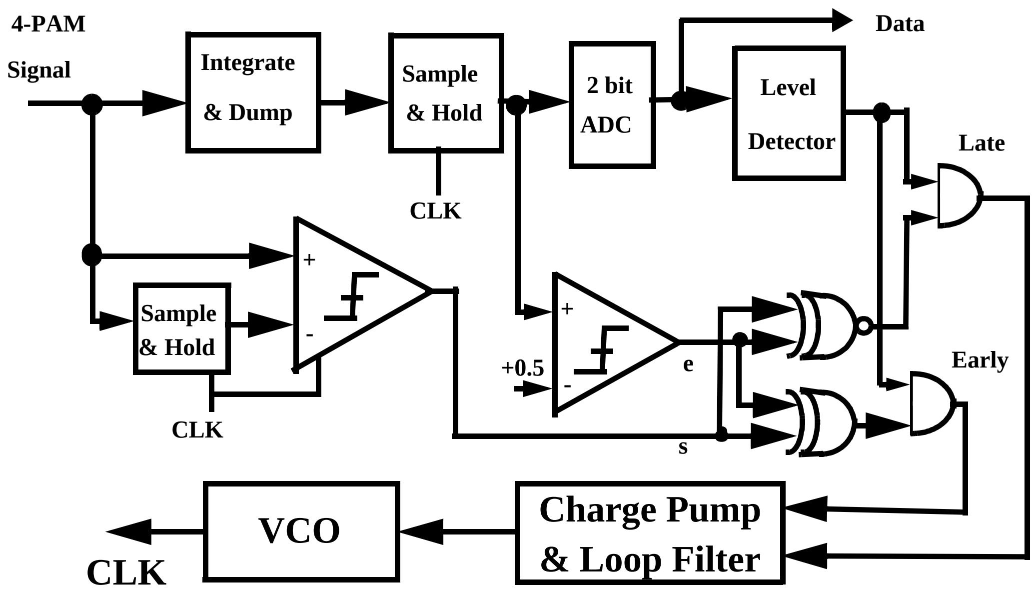
SSMMSE PD BASED CDR (contd.)

- *Problem: High-Speed Slope Detector Required*
- *Solution: Integrate and Dump Receiver*

$$y(kT+\tau) = \int_{((k-1)T+\tau)}^{(kT+\tau)} u(t)dt \Rightarrow \dot{y}(kT+\tau) = u(kT+\tau) - u((k-1)T+\tau)$$



Advantages:

Fewer clock phases than other two methods

Diasadvantages:

Higher jitter

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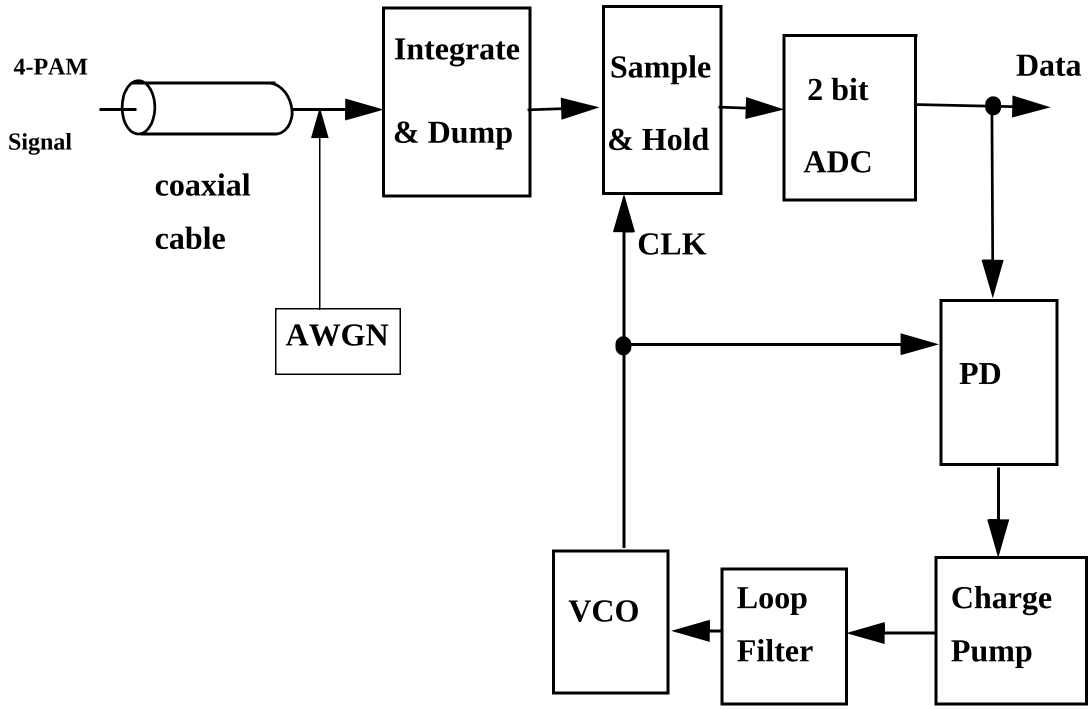
SIMULATION RESULTS

- *Simulated System:*



Symbol Rate	*4Gsymbol/sec*
Cable length	*4m*
AWGN	*SNR=20dB*
VCO Gain	*0.4GHz/V*
Loop Filter	*R1=10kohms* *C1=10pF* *C2=1pF*

- *Charge pump gain was varied to ensure constant loop dynamics.*

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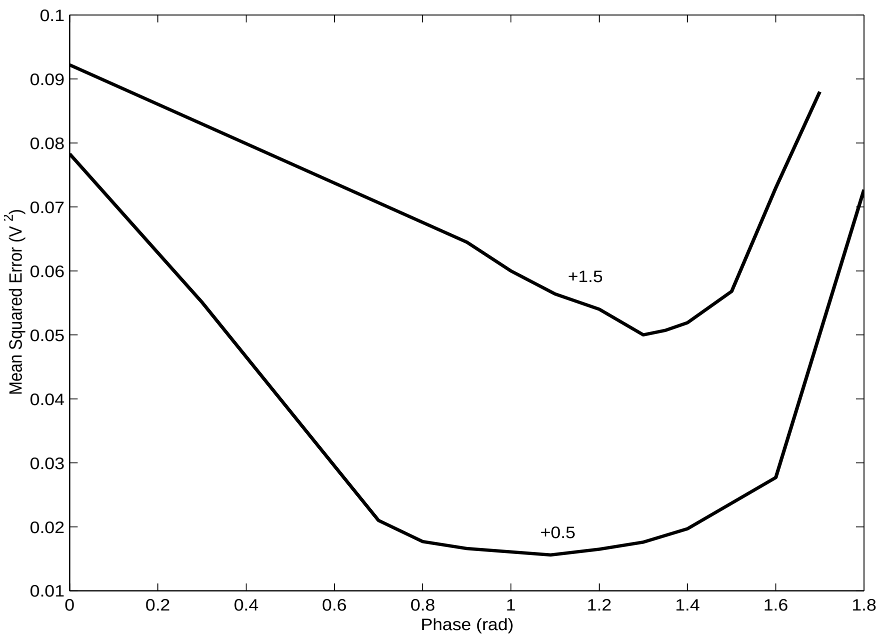
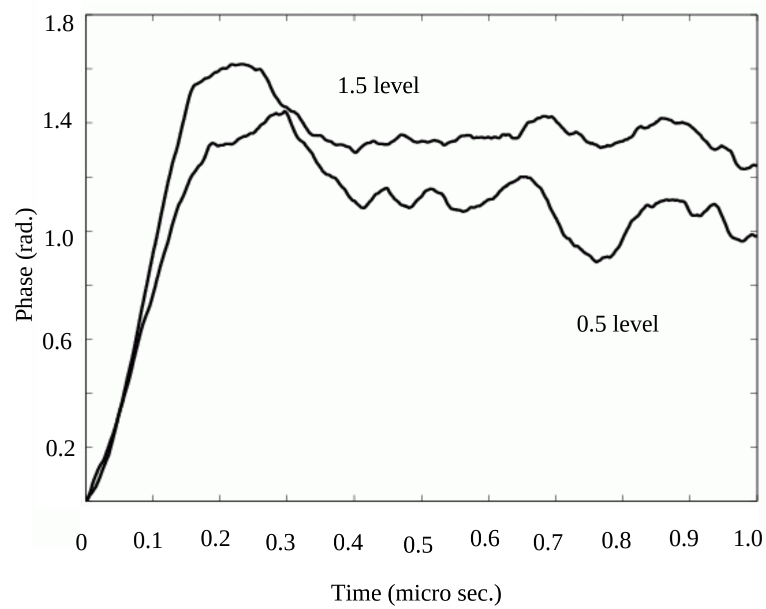
SIMULATION RESULTS (contd.)

- *SSMMSE CDR Performance:*





Monitored Level(s)	Charge Pump Gain	Settling Time	Average Phase in lock	RMS Jitter	Peak to Peak Jitter
V	μ A/rad	μ sec	rad	ps	ps
+0.5 or -0.5	1.6	0.41	1.13	3.2	12.48
+1.5 or-1.5	1.6	0.33	1.35	1.8	7.6

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SIMULATION RESULTS (contd.)

- *SSMMSE PD based CDR Performance (multiple level):*

Monitored Levels	Charge Pump Gain	Settling Time	Average Phase (in lock)	RMS Jitter	Peak to Peak Jitter
V	μA/rad	μsec	rad	ps	ps
Two mid-levels	0.8	0.41	1.13	2.8	10.53
Max. & min. levels	**0.8**	**0.36**	**1.36**	**1.2**	**5.3**
Max./min level and mid level	0.8	0.39	1.27	1.82	7ps
Two mid-levels and max/ min level	0.53	0.42	1.23	1.9	7.4
Max. & min. levels and one mid-level	0.53	0.39	1.31	1.24	5
Four levels	0.4	0.4	1.28	1.5	6

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SIMULATION RESULTS (contd.)

- *Comparison of CDR Performance:*

Phase Detector Type	Charge Pump Gain	Settling Time	Average Phase in lock	RMS Jitter	Peak to Peak Jitter
	μA/rad	μsec	rad	ps	ps
Linear	2000	0.36	**0.86**	**0.5**	**1.8**
Alexander	420	0.32	**0.85**	**1.9**	**8.2**
SSMMSE (two levels=+1.5&-1.5)	0.8	0.36	**1.36**	**1.2**	**5.3**

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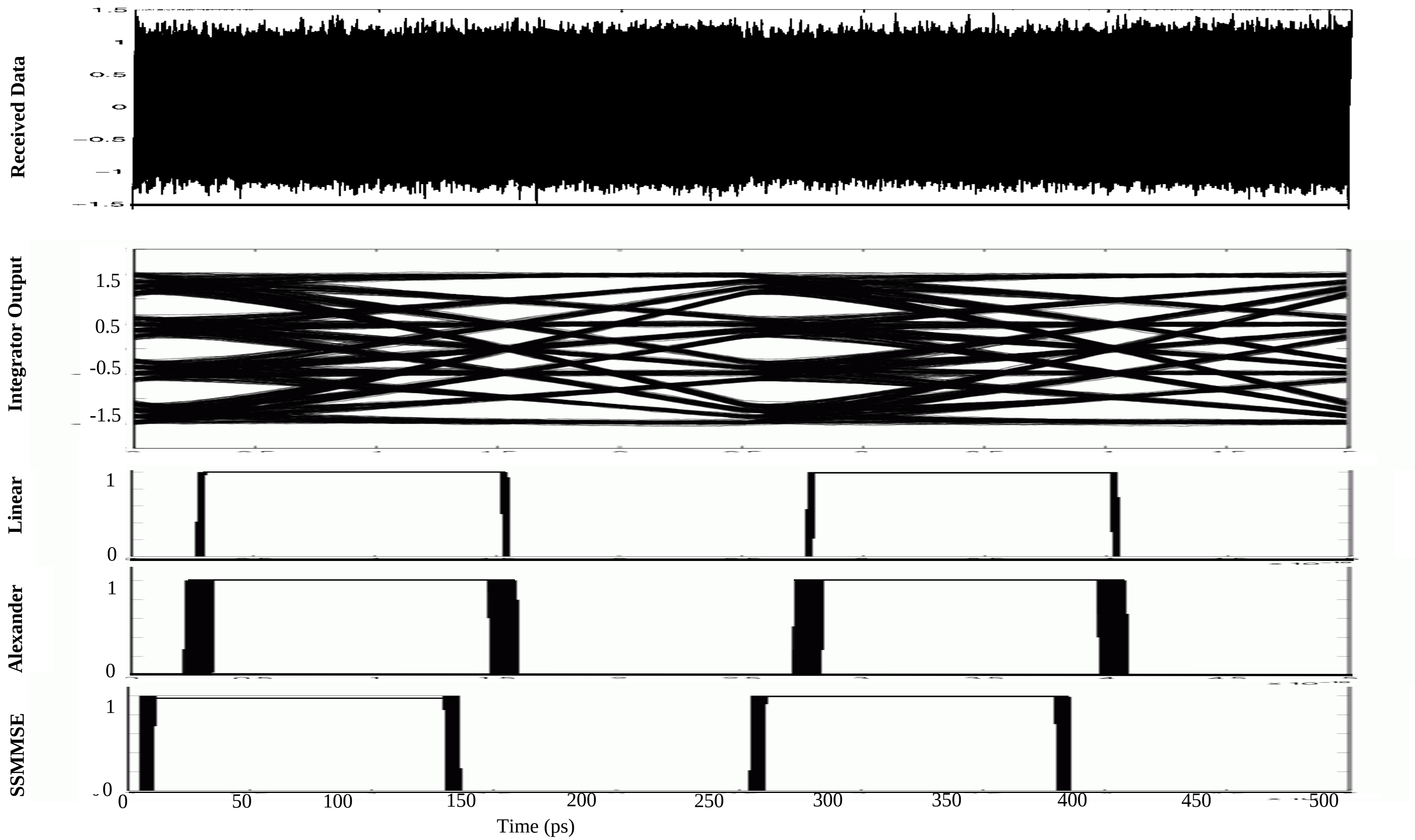
SIMULATION RESULTS (contd.)



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CONCLUSION

- *For channel with AWGN, linear CDR has the lowest jitter and Alexander CDR has the highest jitter.*
- *SSMMSE requires half the number of sampling phases compared to the other two methods.*
- *For integrate and dump receivers SSMMSE method becomes very simple to implement since no slope detector is required.*
- *Ultimate choice of the CDR method depends on the particular channel and shape of the received eye.*