CMOS Technology Scaling Considerations for Multi-Gbps Optical Receivers With Integrated Photodetectors

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***Abstract*—The integration of photodetectors for optical communication into standard nanoscale CMOS process technologies can enable low cost for emerging high volume short-reach parallel optical communication. Whereas past work has highlighted the challenges that face integrated photodetectors in highly scaled CMOS technologies, this work examines the opportunities afforded by these new technologies. First, scaling promises improved extrinsic photodetector bandwidth thanks to improved TIA performance. Second, modern advanced process features enable new photodetector structures with improved performance. A phototransistor employing deep n-wells is characterized in 65-nm CMOS and exhibits a more than ten-fold increase in responsivity over a similar structure without the buried n-well. Third, equalization techniques benefit from technology scaling and are only just beginning to be applied to CMOS integrated photodetectors. In particular, decision feedback equalization appears to offer potential for 10+ Gbps operation.**

***Index Terms*—CMOS photodetectors, decision feedback equalization, nanoscale CMOS, optical communication.**

I. Introduction

THE advantages offered by optical fiber for communication over distances of a few meters are fundamentally different than its advantages when used over longer distances. For long-haul communication the superior signal integrity of optical links is of paramount importance, but over distances of a few meters copper interconnects can be engineered to provide satisfactory signal integrity at multi-Gbps data rates. Hence, cost considerations dominate. Fortunately, advances in optics have lowered the cost and eased the installation of short fiber links by permitting tighter bend radii and (in the case of plastic optical fiber) relaxed alignment tolerances. In rack-mounted computing and storage environments, the cost of operating the equipment over its lifetime now exceeds its initial purchase cost, so optical fiber has become attractive for rack-to-rack and within-rack communication because its thin diameter and light weight permit better airflow (hence, reduced cooling costs) and easier maintenance than copper. Fiber's immunity to electromagnetic interference is attractive for automotive applications. Moreover, fibers can be routed in very tight bundles with much less crosstalk than copper wires, making it a very scalable medium. Although these new applications promise higher volumes for optoelectronic components than long-haul communication, they are more cost-sensitive. The benefits of optical communication for short-reach communication will only be exploited if optical transceivers can be made cost-competitive with copper.

A link employing 1510-nm DFB lasers and single-mode fiber is well suited to optical communication over several kilometers, but is over-designed and too expensive for most short-reach applications. The popularity of multimode fiber and 850-nm VCSELs for optical communication over 100 meters has clearly demonstrated that optical communication technologies with reduced performance and reduced cost are well-suited to shorter distances. Similarly, the use of a CMOS photodetector on the same die as the receiver circuitry permits a high level of integration, improving the economics of short-reach parallel optical communication.

There has been some success integrating the photodetector and TIA in customized manufacturing processes. For example, a SiGe BiCMOS process may be modified to permit the fabrication of PIN photodiodes combining excellent responsivity and bandwidth directly alongside the TIA [1]. A solution with the photodetector implemented on-die with CMOS circuitry is reported in [2] with excellent performance for single-mode fiber links. It relies on a germanium detector coupled to an integrated optical waveguide permitting high responsivity and low capacitance. This and other "silicon photonics" approaches generally make use of trench structures and/or silicon-on-insulator processing, and are therefore likely to benefit from process technology advancements. However, they demand proprietary process flows and the narrow integrated waveguides are not easily mated to the multimode or plastic optical fibers most common in short-reach optical applications. This paper describes large diameter ($> 50\ \mu$m) surface-illuminated photodetectors easing optical module assembly.

This paper focuses upon the growing body of work on high-speed photodetectors realized in standard CMOS processes directly alongside receiver circuitry. Time and again, the integration new functionality into standard CMOS has been commercially successful even when other manufacturing technologies appear to offer inherent performance advantages. For example, wireless technologies have recently benefitted tremen-

Manuscript received December 05, 2010; revised March 04, 2011; accepted April 08, 2011. Date of publication June 23, 2011; date of current version July 22, 2011. This paper was approved by Guest Editor Alvin Loke.

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Digital Object Identifier 10.1109/JSSC.2011.2157254

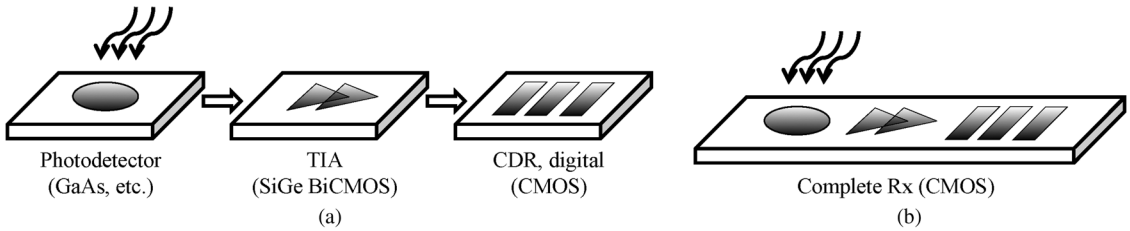


Fig. 1. (a) A typical optical receive-path solution. (b) A fully-integrated CMOS optical receiver.

dously from the wide availability of highly integrated CMOS RF transceivers. Similarly, emerging short-reach optical communication applications will demand higher volume and lower cost from optoelectronic components than previous long-reach optical communication applications, and therefore stand to benefit from standard CMOS integration. Integration of high performance germanium photodetectors onto a nanoscale CMOS platform requires additional processing steps for the deposition of pure germanium and/or creation of optical waveguides. Hence, such approaches inevitably remain a superset of standard CMOS processing and cost more than standard CMOS-only manufacturing. The use of a standard CMOS processing ensures the lowest possible cost, high volume manufacturing capacity, and the availability of second supply sources. The vision of an optical receiver fully-integrated in a standard CMOS manufacturing process is contrasted alongside the current typical optical receive-path solution in Fig. 1. Integration offers the potential for a compact and low cost receiver solution, avoiding the signal integrity challenges and yield losses associated with hybrid integration of the photodetector and TIA.

Integrated parallel optical inputs promise tremendous aggregate bandwidth, so it would seem natural to try to implement them in nanoscale CMOS where high throughput digital processing may usefully process the data. In [3], a comprehensive examination of CMOS photodiodes for multi-Gbps communication is presented focusing on a 0.18-μm technology, and more recent work has targeted 0.13-μm CMOS [4]–[6]. In this work, we consider how these integrated receivers might be implemented in nanoscale CMOS where highly-integrated optical I/O may open new applications.

II. CMOS Photodiode Background

The high-speed response of a CMOS integrated photodiode is worse than that of optimized discrete-component photodiodes, both in terms of its intrinsic limitations, and in terms of its increased capacitance leading to a lower extrinsic bandwidth when connected to a transimpedance preamplifier [7]. Nevertheless, their low cost especially in high volume production is strong motivation to consider their use for optical communication. A representative sketch of frequency response is shown in Fig. 2. Note that CMOS photodetectors typically exhibit very low intrinsic bandwidth, f_i, on the order of a few MHz or even lower. However, because the mechanisms that limit intrinsic bandwidth are not modeled by a single time constant, the magnitude responsivity rolls off at a relatively slow rate (3–10 dB/decade). Extrinsic bandwidth limitations, on the other hand, are characterized by a dominant pole. Hence, beyond some frequency f_e, extrinsic limitations dominate causing the magnitude responsivity to roll off more sharply. Finally, CMOS photodiodes are integrated in processes with many metal and contact layers, causing them to reflect and/or absorb more light before it even reaches the semiconductor surface. This section examines the impact of process technology scaling on both intrinsic and extrinsic bandwidth, as well as reflection and absorption losses.

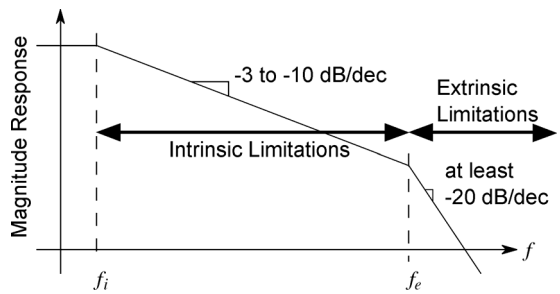


Fig. 2. Frequency response of a CMOS photodiode with integrated transimpedance amplifier.

A. Intrinsic Limitations

When incident photons are absorbed in a semiconductor, they produce electron-hole pairs. The absorption is a stochastic process governed by the Beer-Lambert law; the depth at which each photon is absorbed is a random variable with an exponentially-distributed probability density function (PDF) having a mean penetration depth, d_0. The PDF as a function of the distance below the semiconductor surface, x, is

$$p_d(x) = \frac{e^{-x/d_o}}{d_o} \tag{1}$$

The mean penetration depth d_0 depends upon the wavelength of light and the semiconductor used. The most common wavelength (λ) for short-reach optical communication is around 850 nm since low-cost VCSELs can be used as light sources at this wavelength for transmission over multimode fiber. At $\lambda = 850$ nm, the most popular semiconductors for use in photodetectors are Ge, GaAs, InGaAs, and InP, which have mean penetration depths in the range of 0.1 to 1.0 μm. By contrast, silicon has a mean penetration depth of $d_0 = 18$ μm at $\lambda = 850$ nm.

Clearly for high-speed operation, it is desirable to ensure that the depleted, high-electric-field region of the photodiode coincides with the areas where most charge carriers are generated. Hence, if a silicon photodiode is to be used for 850-nm light, the

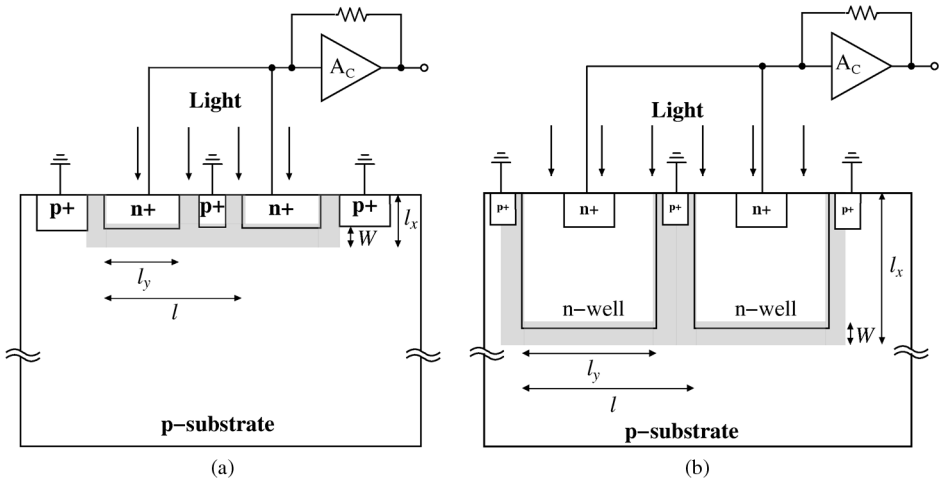


Fig. 3. Cross-section of CMOS photodiodes in standard CMOS: (a) n+/p-substrate junction; (b) n-well/p-substrate junction. The depletion region is indicated by the shaded region.

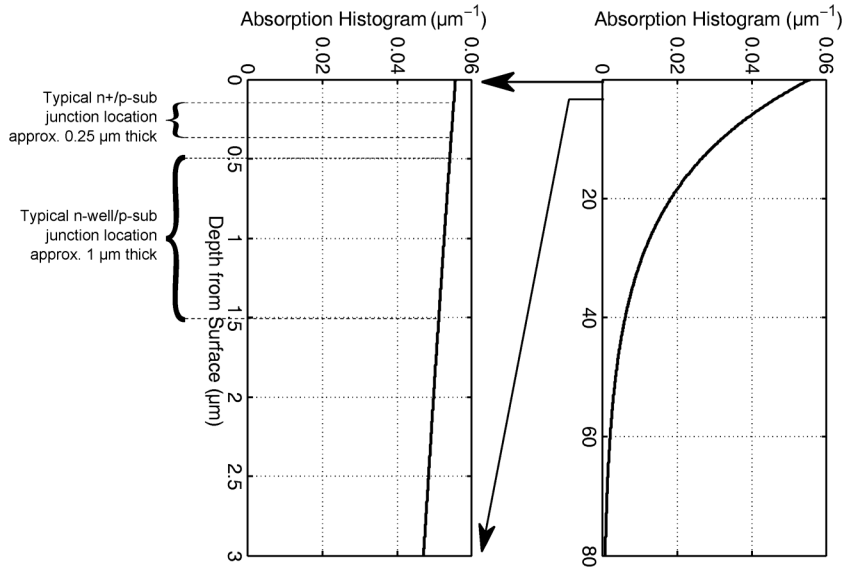


Fig. 4. Histogram of the absorption of 850 nm light in silicon.

depletion region must span 10's of μm to satisfy this requirement. This is impossible to achieve in modern standard CMOS processes. Fig. 3 shows two examples of junction photodiodes in CMOS: a n+/p-sub diode, and a n-wel/p-sub diode. The photodiode's p-type terminal is typically grounded and the n-type positively biased, in this case by the input transimpedance amplifier.

Both the width of the photodiode's depletion region, W, and its depth below the surface, l_x, influence photodetector performance. For an abrupt junction,

$$W = \sqrt{\frac{2\epsilon_{Si}}{q}\frac{N_A + N_D}{N_A N_D}(V_{bi} - V_R)} \tag{2}$$

where N_A is the dopant concentration in the p-type material, N_D is the doping in the n-type material, ϵ_{Si} is the the permittivity of silicon, q is the charge of an electron, V_{bi} is the junction's built-in potential, and V_R is the applied reverse-bias voltage. Fig. 4 illustrates the location and width of the depletion regions formed in Fig. 3 representative of a 0.18-μm CMOS process with roughly 0.6-V reverse bias, alongside the absorbtion histogram for 850-nm light in silicon given by (1). The n+/p-sub junction is closer to the surface where the absorption is maximized, but has a very narrow depletion region due to the relatively high dopant concentrations found there. The distance from the junction to the surface is much greater for the n-well/p-sub diode, but is still much less than the penetration depth d_0, so Fig. 4 illustrates there is little penalty due to this increased depth. However, the lower dopant concentrations in this junction ensure that for the same reverse bias it encompasses more total photo-generated charge carriers. In summary, the wider depletion region provided by a n-well/p-sub junction offers advantages over a n+/p-sub junction that more than offset its increased distance from the surface providing a net benefit.

A model for the response of integrated photodiodes is presented in the Appendix [8]. A representative plot is presented in Fig. 5 for a reverse bias voltage of 1.0 V where the contributions of currents due to photocarriers generated in the n-type

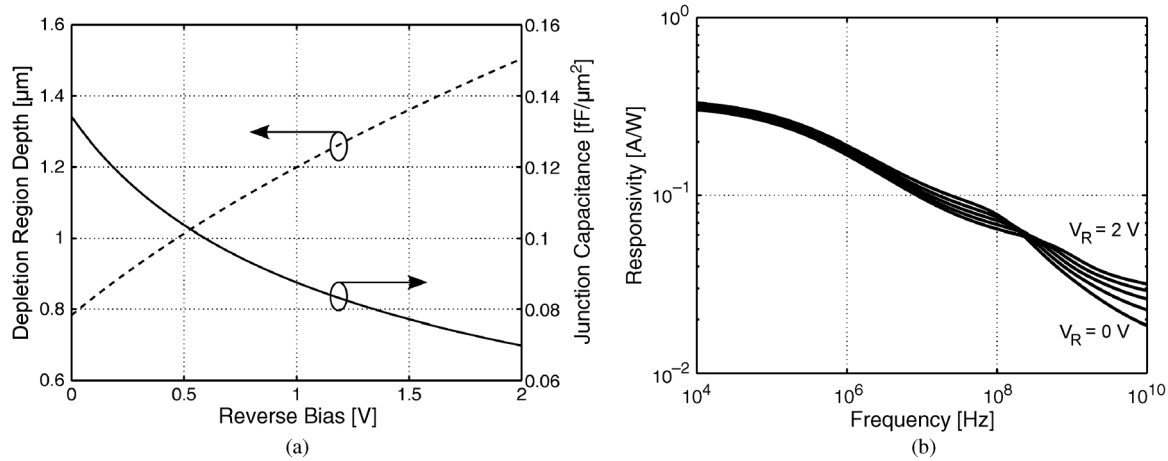


Fig. 6. The impact of voltage scaling on CMOS photodetectors based upon the model in the Appendix: (a) depletion region width and capacitance of a n-well/p-substrate junction; (b) intrinsic frequency responses for reverse bias voltages varying over the range 0–2 V.

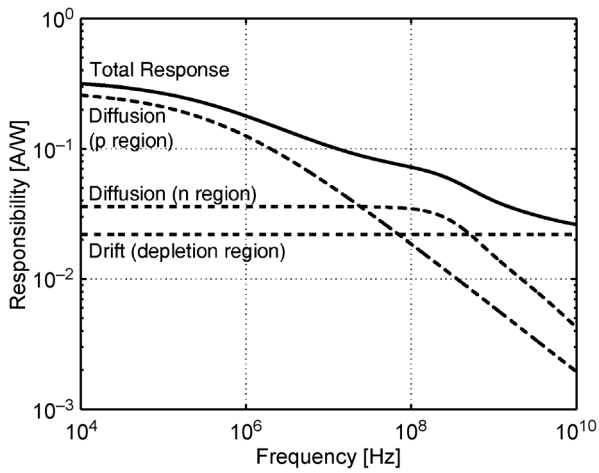


Fig. 5. A typical intrinsic frequency response of an n-well/p-substrate junction photodiode based upon the model in the Appendix with a reverse bias voltage of 1.0 V.

region, p-type region, and in the depletion region are separately identified.

As process technologies advance, the supply voltage available for reverse biasing the diode decreases, and along with it the depletion region width. With supply voltages of 0.8 V common in 22-nm CMOS, and the International Technology Roadmap for Semiconductors (ITRS) [9] indicating supply voltages as low as 0.6 V at gate lengths around 10 nm, integrated CMOS photodetectors may have only a few hundred millivolts reverse bias. Fig. 6(a) shows a plot of the width of the depletion region as a function of reverse bias voltage for a typical n-well/p-substrate diode. Increasing reverse bias voltage results in a thicker depletion region which, in turn, means that more photocarriers are generated in the depletion region and the resulting drift current has a higher contribution to the overall photodiode response. However, as shown in Fig. 5, drift current is only significant at very high frequencies where extrinsic bandwidth limitations are also of great concern. Hence, supply voltage scaling is significant both in its influence on junction capacitance as illustrated in Fig. 6(a), and on the intrinsic bandwidth of CMOS photodetectors as illustrated in Fig. 6(b).

TABLE I
JUNCTION CAPACITANCES FOR N-WELL/P-SUBSTRATE PHOTODIODES AT 0.6-V REVERSE BIAS

CMOS Technology	$C_{j,bot}$ [fF/μm^2]	$C_{j,sw}$ [fF/μm]
$0.18-\mu$m	0.101	0.47
90-nm	0.087	0.79
65-nm	0.075	0.55

The most important factor influencing the response of CMOS photodiodes at low frequencies (assuming 850-nm light) is minority carrier lifetime in the substrate, which is in turn determined by the dopant concentration N_A. Higher substrate doping levels lead to short carrier lifetimes, and the resulting increase in carrier recombination reduces dc responsivity. Under constant field scaling, one would expect dopant concentrations to increase adversely affecting intrinsic photodiode performance. However, in lightly-doped substrates $N_A < 10^{18}$ cm^{-3}, the impact is minimal and barely evident at frequencies above 1 MHz. In addition, a decreased low-frequency response can actually improve signal integrity at multi-Gbps data rates since it reduces distant post-cursor intersymbol interference (ISI). Most importantly, simulations across 0.18-μm to 65-nm technology nodes summarized in Table I suggest no clear scaling trend in the dopant concentrations beneath n-wells.

Overall, technology scaling does not appear to dramatically affect the intrinsic properties of n-well/p-substrate photodiodes.

B. Extrinsic Limitations

Although a regulated cascode front end can maximize extrinsic bandwidth by presenting a very low input resistance to the photodiode, doing so increases input-referred noise and demands a higher supply voltage [5], [10]. Instead, receiver sensitivity requirements usually dictate a direct connection between the photodiode and a shunt-feedback transimpedance amplifier (TIA) as shown in Fig. 7. The TIA's core amplifier is in turn comprised of N elementary gain stages in series; for example,

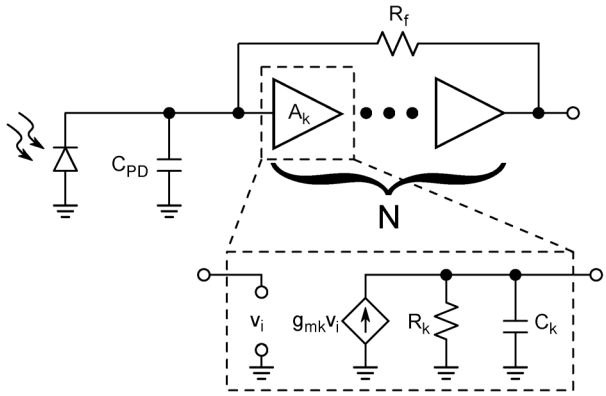


Fig. 7. A shunt-feedback transimpedance amplifier with multiple gain stages.

$N = 1$ was used in [3], [10], $N = 2$ in [5], [11] and $N = 4$ in [4].

Process technology advancements offer fundamental improvements in extrinsic bandwidth. Adopting the model of Fig. 7, the photodetector capacitance is C_{PD} and a resistor R_f appears in feedback around the TIA's N gain stages where the kth gain stage is characterized by a transconductance g_{mk}, output resistance R_k and load capacitance C_k. Assuming $R_f \gg R_k$ and each stage has a dc gain $A_k = g_{mk}R_k$, the dominant pole of the open-loop response is at the input

$$\omega_i = \frac{1}{R_f C_{PD}} \tag{3}$$

and there are N other poles at

$$\omega_k = \frac{1}{R_k C_k} = \frac{g_{mk}}{A_k C_k} \tag{4}$$

The open-loop unity gain frequency is also approximately the TIA's closed-loop 3-dB bandwidth (assuming a large phase margin is maintained).

$$\omega_0 \approx A_k^N \omega_i = \frac{A_k^N}{R_f C_{PD}} \tag{5}$$

To ensure a phase margin θ, each of the N other poles ω_k must contribute only $(\pi/2 - \theta)/N$ phase shift at ω_0.

$$\omega_k = \frac{\omega_0}{\tan\left(\frac{\pi/2-\theta}{N}\right)} \tag{6}$$

$$\frac{g_{mk}}{A_k C_k} = \frac{A_k^N}{R_f C_{PD}} \tan\left(\frac{\pi/2-\theta}{N}\right) \tag{7}$$

For example, to ensure 60 degrees phase margin, the TIA's internal poles must exceed the closed-loop bandwidth by 1.73× for $N = 2$ or 3.73× for $N = 4$. For fixed gains A_k and transconductance g_{mk} (and hence, presumably, fixed power per stage) the TIA's internal parasitic MOS capacitances C_k decrease with technology scaling. This permits bandwidth to be increased by increasing the number of stages, N, and/or increasing the gain per stage A_k while maintaining the same phase margin.

C. Reflection and Absorption Losses

The many dielectric interfaces that lie above the surface of CMOS photodiodes can account for losses of up to 90% or more in 130-nm CMOS [4]. Another significant performance limitation is the now-commonplace deposition of silicide over CMOS active regions. Silicide facilitates the formation of low-resistivity contacts, but may be optically opaque [7]. For example, a 20-nm-thick layer of Cobalt silicide, typical of 130-nm processes, can reduce optical transmission by 90–95% [12]. Low series resistance is essential to ensure high extrinsic photodiode bandwidth, so silicide must be included in contact regions, but blocked elsewhere over the photodiode.

Technology scaling is generally accompanied by a proliferation of dielectric layers above the silicon surface, tending to increase dielectric losses. Scaling also places stringent requirements on planarity, making it more difficult to exclude metal over the entire photodiode area. However, scaling can have positive consequences as well. The ITRS roadmap [9] defines several positive trends for CMOS photodetectors going from 45-nm to 22-nm CMOS. Minimum contacted metal pitch decreases by 50% and contact resistivity decreases by over an order of magnitude, both of which will permit a smaller fraction of the photodetector area to be covered by wiring and contacts, providing improved responsivity. At the same time, silicide thickness decreases from 20 nm to 12 nm, increasing optical transmission in those areas where silicide is deposited.

III. Alternative CMOS Photodetectors

Technology scaling is often accompanied by process features which may be used to advantage in the realization of CMOS integrated photodetectors. For example, it has long been known that SOI substrates may be used to shield photodetectors from substrate diffusion currents [13]. The ITRS predicts an increased prevalence of SOI substrates going forward. In addition, the reduced lateral dimensions in scaled technologies may facilitate the use of lateral junctions to perform photodetection, as in for example [14], or the use of lateral fields to collect substrate photocarriers as in [6].

Buried n-wells are another useful feature. They may be used to shield substrate photocarriers from a collecting photodiode. Alternatively, they may be used to realize a phototransistor, as illustrated in Fig. 8. In this case, the base current is provided by the photo-generated carriers in the p-type region. A positive bias is applied to the n+ implant (serving as collector) by the TIA. Alternatively, a dc bias voltage can also be applied to the base, upon which the photocurrent will be superimposed. Phototransistors have been used for high-speed detection in SiGe processes [15], [16]. Clearly the transistor gain will be much less in a CMOS processs, but lateral scaling may promise future improvements in the performance of similar structures.

IV. 65-nm Characterization

A test chip was developed to characterize the performance of photodetectors in a 65-nm CMOS technology [17]. A die photo is shown in Fig. 9. Two types of photodiodes were tested, both

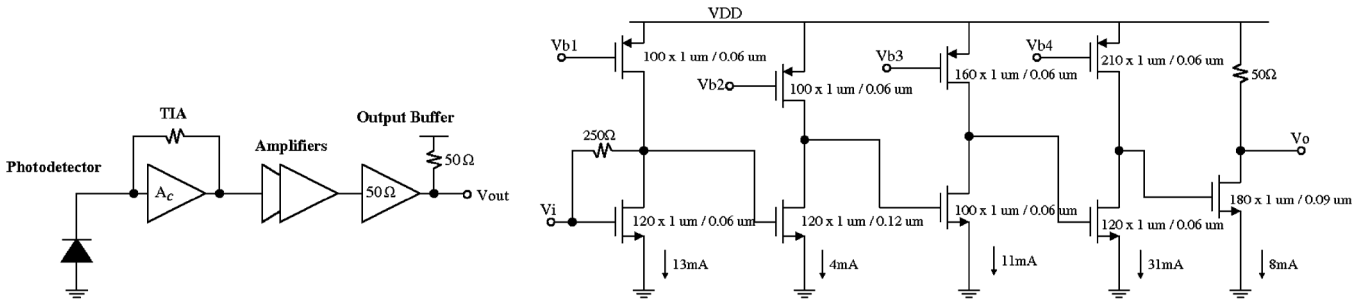


Fig. 10. (a) A block diagram of the circuit used to characterize 65-nm CMOS photodetectors. (b) The detailed schematic.

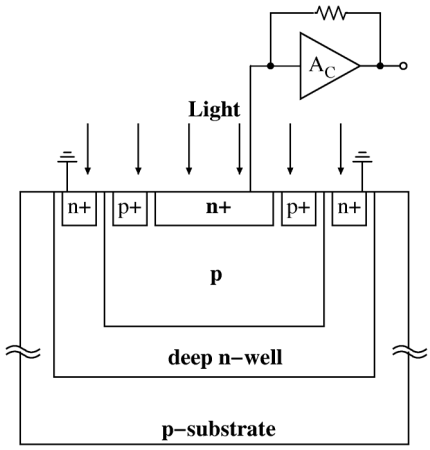


Fig. 8. A CMOS phototransistor made using a buried n-well.

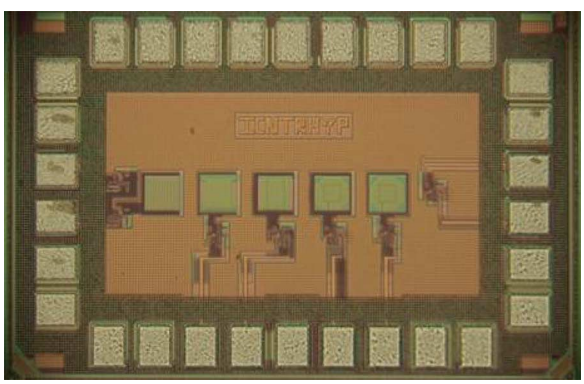


Fig. 9. Die photo of photodiodes and pre-amplifiers for characterization in 65-nm CMOS.

60 μm $\times$ 60 μm in size: a simple n+/p-substrate photodiode, as shown in Fig. 3(a), and a phototransistor as in Fig. 8.

In order to more accurately measure the responsivity and frequency response of the integrated photodetectors, an amplifier and 50-Ohm buffer is integrated alongside the test structures. An overall block diagram and schematic of the measurement circuit is shown in Fig. 10. The amplifier design is simple and not optimized for low power—much higher levels of performance are attainable in 65-nm CMOS [18]. It comprises a common source first stage with shunt-shunt feedback to provide a low input impedance, three more common-source stages for more gain, and finally a 50-Ohm output buffer to interface with test equipment. All measurements were made with a supply voltage of 1.3 V resulting in a photodetector reverse bias voltage of 670 mV.

An electrical breakout of the amplifier was included on-die so that its gain could be deembedded from the photodetector measurements. A dc transimpedance gain of 1 kΩ and a 3-dB bandwidth of 2 GHz were measured. Since this bandwidth far exceeds that of the measured photodetectors, a flat magnitude response was assumed when plotting the frequency response.

The photodetectors were characterized by illuminating them from above with a 850-nm source coupled into a multimode fiber manually aligned above the die. The voltage swing observed at the amplifier output was then input-referred dividing by the amplifier's measured transimpedance gain. The resulting photodetector current was divided by the input optical power measured using an optical power meter to yield the photodetector responsivity.

Measurement results from the standard n+/p-substrate photodiode are plotted in Fig. 11(a). A dc responsivity of just over 0.03 A/W, a 3-dB bandwidth of 2.5 MHz and a high-frequency rolloff of 5 dB/decade are observed. The relatively low responsivity compared with previously reported results in other technologies may be partly attributable to increased carrier recombination, but is mostly attributable to the layer of silicide deposited across the surface of this entire photodiode. Silicides are known to be optical opaque with transmission in the range of 20-2% reported for silicide layers between 9 and 60 nm thick [12]. This is consistent with the observed 0.03 A/W considering a typical CMOS photodiode responsivity of 0.2–0.3 A/W [7]. The photodiode model described in the Appendix is applicable to this structure, and a plot of the frequency response predicted by the model is superimposed in Fig. 11(a) using model parameters representative of a 65-nm process and assuming 5% of the incident optical power penetrates through the dielectric stack and into the silicon photodiode.

Measurements of the 65-nm npn (n+/p-tub/deep n-well) phototransistor are shown in Fig. 11(b). It exhibits of 3-dB bandwidth of only 150 kHz and a rolloff of 9 dB/decade, but a much-improved dc responsivity of 0.34 A/W, comparable to the very best obtained from any standard CMOS photodetectors, in spite of the layer of silicide. The effect of silicide over the phototransistor is the same as in the photodiode. We may assume the photo-generated current in the phototransistor is at the same low level as in the photodiode, but it is magnified by the npn

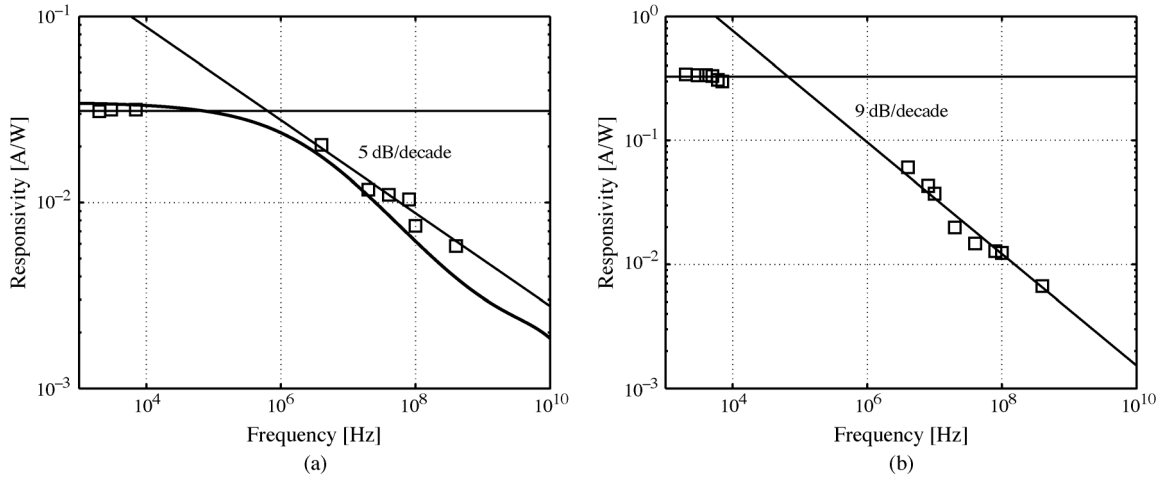


Fig. 11. Measured frequency response of a (a) n+/p-substrate photodiode with model predictions superimposed, and (b) a n+/p/buried-n-well phototransistor in 65-nm CMOS.

TABLE II
SUMMARY OF 65-nm CMOS PHOTODETECTOR MEASUREMENTS

Photodetector	**DC Responsivity** [A/W]	**3-dB Bandwidth** [MHz]	**Rolloff** [dB/dec]
n+/p-substrate photodiode	0.03	2.5	5
n+/p-tub/deep n-well phototransistor	0.34	0.15	9

bipolar transistor's current gain providing an order-of-magnitude increase in responsivity. Unfortunately, these n+/p-sub/n-well transistors have low speed because they are parasitic devices whose dopant profile is not optimized for speed. Hence we see increased responsivity, but only at low frequency. A shallower buried n-well would narrow the base region and should therefore improve the current gain and base transit time (hence, bandwidth) of the phototransistor. If the deposition of silicide was blocked over most of the photodiode surface, responsivities far exceeding 1 A/W would be achievable. Hence, multi-Gbps operation should be possible using either photodetector, but only if the improved transistor speed available in 65-nm CMOS can be leveraged to provide adequate equalization.

A summary of the results is provided in Table II. The improved low-frequency responsivity of the phototransistor can be beneficial for applications where extrinsic bandwidth limitations predominate. For example, plastic optical fiber (POF) has a core diameter of up to 1 mm and therefore demands a large photodetector. Current POF transceivers are currently in the range of 0.1–1 Gbps [19] where the primary challenges are sensitivity and extrinsic bandwidth limitations.

V. EQUALIZATION OF CMOS PHOTODETECTORS

Many wireline communication applications benefit from technology scaling by enabling more efficient signal processing circuits (analog and/or digital) to improve signal integrity. This is a promising direction for receivers employing integrated photodetectors since only relatively simple signal processing has been thus far attempted.

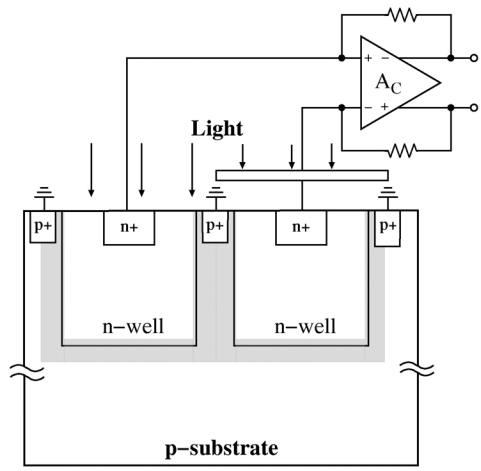
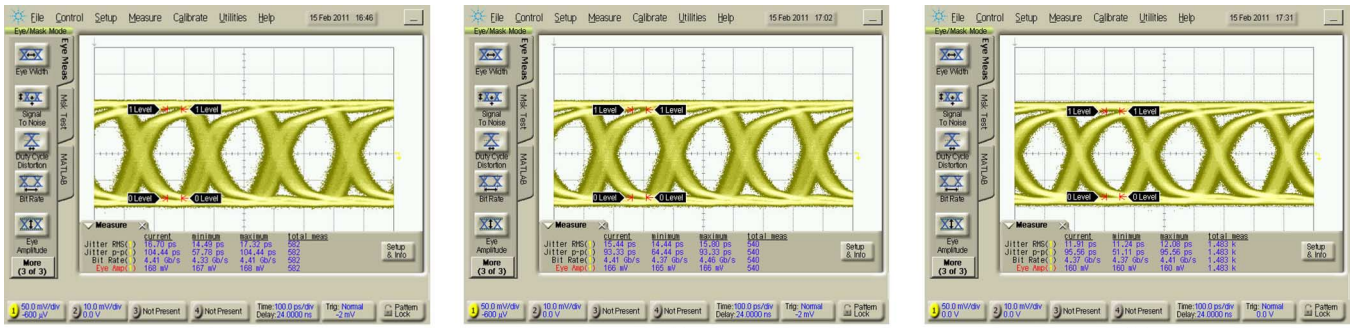


Fig. 12. Cross-section of a CMOS spatially modulated light (SML) detector showing the differential amplifier required to cancel slow diffusing carrier currents.

For example, spatially modulated light (SML) detectors measure and cancel substrate photocurrents electronically using neighboring matched photodiodes, one covered and the other illuminated as illustrated in Fig. 12 [20]. The principle is that deeply-penetrating photons give rise to the slowest diffusing photocarriers, but these are equally likely to arrive at either the covered or illuminated pn junctions in Fig. 12. Hence, by subtracting the resulting photocurrents using a differential amplifier, only the fast photocurrents generated in the illuminated photodiode appear at the amplifier output. They are very effective at mitigating intrinsic bandwidth limitations. Some of the highest speed integrated CMOS receivers reported to date have made use of SML detectors [5], [11], [21]. However, since much of the signal content is either reflected away or canceled electronically, SML detectors generally have low responsivity, with 0.05 A/W reported in [5], [22], resulting in receivers with poor sensitivities on the order of -5 to -2 dBm, an exception being sensitivities of -9.5 to -8.5 dBm at 2.5–3.125 Gbps and a bit error rate of 10^{-12} reported in [22]; those results



(a) (b) (c)

Fig. 13. Measured eye diagrams for the receiver of [22] with a 4.25-Gbps PRBS $2^{31}-1$ pattern and fixed equalizer settings at (a) 0°C, (b) 25°C, and (c) 85°C.

were enabled by a TIA with a very low input-referred noise of 0.19 $\mu A_{\rm rms}$ and thus necessitated a relatively high power consumption.

With the possible exception of SML detectors under extremely high reverse bias voltage [21], photodetectors in standard CMOS processes require equalization to achieve data rates of 5+ Gbps. Linear equalization has been applied to both a standard CMOS photodetector [3] and SML detectors [4], [5], [10], [11]. The equalizer compensates for both intrinsic and extrinsic bandwidth limitations, particularly when combined with a SML or other bandwidth-enhanced photodetector [6]. There has been some disagreement in the literature with regards to whether such linear equalizers require continuous adaptation to guarantee performance in the presence of temperature variations, with [3] indicating that adaptation is not necessary and [5] indicating that adaptation in needed. Measured eye diagrams at 0°C, 25°C, and 85°C are shown in Fig. 13 for the receiver of [22] which, like [3], [5], has a CMOS integrated photodetector followed by a TIA and linear equalizer. Those measurements show only ±5% variation in jitter over temperature while keeping the equalizer setting fixed. In this work, decision feedback equalization (DFE) is considered.

Rather than only using a linear equalizer to provide amplification at frequencies where CMOS photodetectors inherently provide poor SNR, a DFE can be used to compensate for frequency-dependent losses without noise enhancement. To study the potential for this approach, the standard CMOS n-well/p-substrate photodiode model in the Appendix, and a SML variant of it [8] are each incorporated into the model in Fig. 14. Shown in Fig. 15 are normalized 5-Gbps pulse responses for the standard and SML detectors. For these plots, a TIA input resistance of 160 Ω is assumed, along with $C_{PD} = 1$ pF for the standard photodiode and $C_{PD} = 1$ pF for the SML detector (since the active area is split between the covered and uncovered photodiodes). Analog equalizers are also included. For the standard photodiode, three first-order equalizers were connected in parallel [3]. For the SML detector, a simpler equalizer with 1 zero and 2 poles was assumed [11]. In both cases the pole and zero locations were chosen to provide a maximally-flat overall link response.

The pulse responses in Fig. 15 include markers at time intervals of 1 UI at 5 Gbps, for reference. Notice that the ISI is mostly postcursor, and in the case of the standard photodiode persists over many symbol periods in spite of the equalizer. Transmit

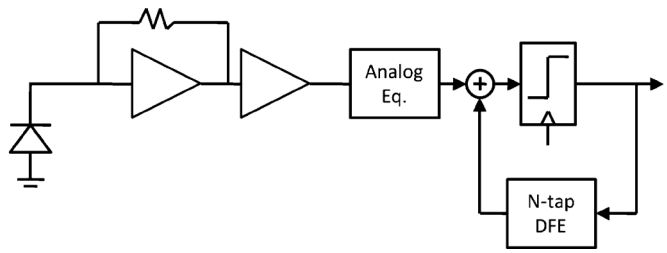


Fig. 14. The receiver model used to evaluate the efficacy of a DFE with a CMOS integrated photodetector.

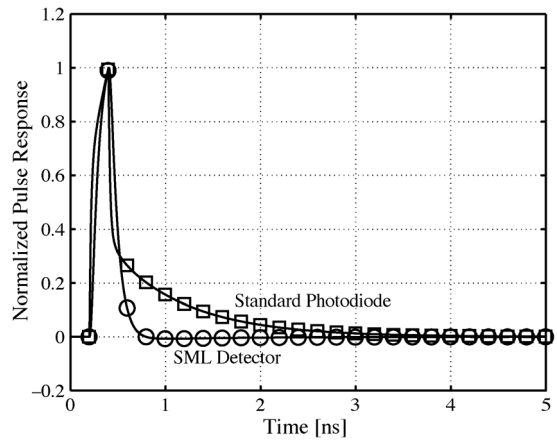


Fig. 15. Pulse responses used to evaluate equalization for receivers at 5 Gbps employing CMOS n-well/p-substrate photodetectors.

pre-emphasis in these links is useful for combating the bandwidth limitations of the interconnect between transmitter and laser and of the laser itself [23], but cannot be straightforwardly applied to equalize the intrinsic and extrinsic bandwidth limitations of a CMOS photodetector due to the nonlinear response of the laser. Hence, performance continues to improve steadily as the number of DFE taps is increased. However, for the SML detector with analog equalization, only 1 post-cursor ISI term is significant, increasing to 2 when the data rate is doubled to 10 Gbps. Hence, the data rate can exceed 10 Gbps with only 2 DFE taps. However, note that the amplitude of the plotted pulse responses are normalized; since SML detectors have inferior dc responsivity, they demand a more sensitive (lower-noise) TIA. Recently-reported DFEs with many taps have achieved sub-mW/Gbps power efficiency at data rates exceeding 10 Gbps

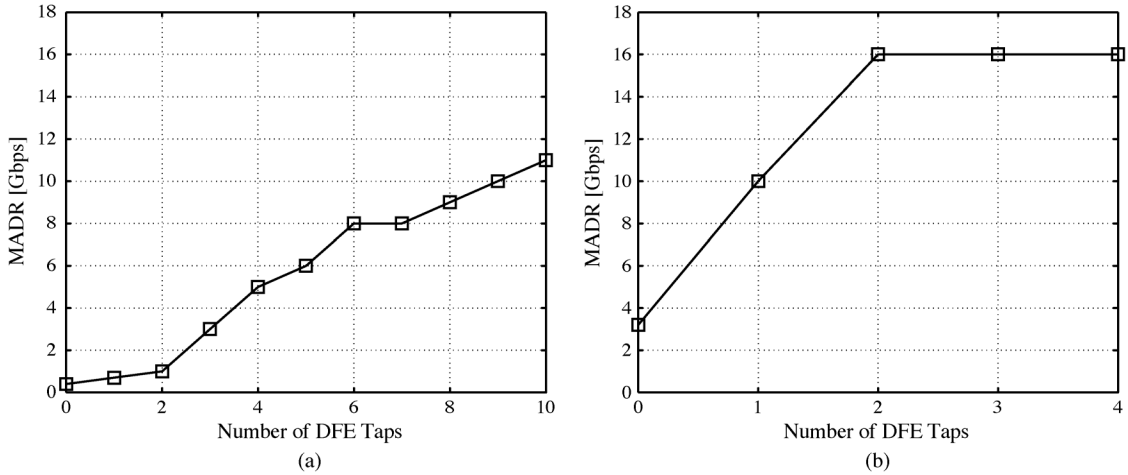


Fig. 16. The simulated maximum achievable data rate (MADR) for (a) n-well/p-substrate photodiode, and (b) a SML photodetector. Each is followed by an analog equalizer and DFE.

(e.g. [24]) so it is expected that the TIA and subsequent amplification stages will continue to dominate the power consumption of optical receivers. For example, in [23] a TIA alone consumes approximately 1 mW/Gbps but has a much higher input resistance and input-referred noise than would be required here.

The maximum achievable data rate (MADR) is plotted in Fig. 16(a) and (b) for the standard and SML detectors respectively when followed by a DFE with a varying number of taps. The MADR is the data rate at which data dependent jitter (DDJ) for a PRBS $(2^7 - 1)$ pattern is 0.3 $\mathrm{UI_{pp}}$ after application of the DFE. DDJ is determined in the presence of the DFE by sweeping receiver sampling phase with constant tap weights. It is assumed that main cursor of the pulse response has an amplitude of at least 5 mA/W, the optical input has an average power of -3 dBm with a high extinction ratio, and the receiver's input referred noise is 0.35 $\mu\mathrm{A_{rms}}$. Since the standard photodiode has a longer pulse response, more taps are required to effect a significant improvement. A SML detector, on the other hand, has the potential operate above 10 Gbps with only a few taps of DFE, although at lower sensitivities.

VI. Conclusions

Integration of photodetectors for optical communication in standard CMOS enables lower cost than modified CMOS or customized optoelectronic process technologies, especially for high volume applications. Moreover, ICs fabricated in nanoscale CMOS technologies are capable of processing data with tremendous throughput and therefore stand to benefit from integrated parallel high-speed optical receive paths more than older CMOS technologies. Whereas past work has highlighted the challenges that face integrated photodetectors in highly scaled CMOS technologies, this paper has attempted to more closely examine the opportunities afforded by these new technologies. Firstly, assuming the use of n-well photodetectors in low-ohmic substrates, scaling promises improved extrinsic photodetector bandwidth thanks to improved TIA performance. Secondly, modern advanced process features may enable new photodetector structures with improved performance. The potential for one such structure (a phototransistor employing deep n-wells) was characterized in 65-nm CMOS and exhibited a more than tenfold increase in responsivity over a similar structure without the buried n-well. Finally, equalization techniques benefit from technology scaling, yet are only just beginning to be applied to CMOS integrated photodetectors. In particular, the DFE appears to offer potential for 10+ Gbps operation.

Appendix

A model for the response of integrated photodiodes is obtained by summing the drift current in the depletion region and the diffusion currents in both the n- and p-type regions:

$$J_{total} = (1 - R)(J_{drift} + J_{n,diff} + J_{p,diff}) \tag{8}$$

where $R < 1$ is that fraction of light reflected and/or absorbed by the dielectric and metallic layers above the semiconductor surface. Closed-form expressions for each current component are obtained in [8] assuming the photodiode is illuminated from above the n-type region, and the p-type region is of infinite depth (approximating the substrate in a bulk CMOS process). The photodiode is interrupted with spatial periodicity l to contact the bottom p-type region. For the drift current,

$$J_{drift}(jw) = \frac{\Phi_0(jw) q W A_I}{d_0 A_T} \tag{9}$$

where

$$\Phi_0(jw) = \frac{p}{hc/\lambda} \tag{10}$$

Φ_0 is the incident optical flux, p the incident optical power, A_I the area below the immediate diffusion or well contact, and A_T the total detector area.

For the diffusion currents,

$$J_{p,diff} = \Phi_0(jw) q \alpha L_n e^{-\alpha l_x} \frac{1}{\sqrt{1 + jw\tau_n} + \alpha L_n} \tag{11}$$

where

$$L_n = \sqrt{D_n \tau_n} \tag{12}$$

TABLE III
REPRESENTATIVE MODEL PARAMETERS FOR A CMOS N-WELL/P-SUBSTRATE PHOTODIODE

D_n	10 cm^2/s
D_p	5 cm^2/s
τ_n	10^{-4}s
τ_p	10^{-5}s
l_y	$2.6\mu\text{m}$
l	$4.0\mu\text{m}$
l_x	$2\mu\text{m} + W$
N_A	$1.6 \cdot 10^{15}\text{cm}^2$
N_D	$1.6 \cdot 10^{17}\text{cm}^2$

is the diffusion length of the minority carrier electrons in the p-region, D_n is the diffusion coefficient, τ_n is the minority carrier lifetime, and l_x the distance between the top surface of the photodiode and the bottom of the space charge region.

$$J_{n,diff}(jw) = \Phi_0(jw) q \frac{L_p^2}{l} \frac{32}{\pi^2} \frac{(1 - e^{-\alpha l_x})}{l_x} \times \sum_{n=1}^{\infty} \sum_{m=1}^{\infty} \frac{\frac{2l_x}{l_y}\left(\frac{1}{2n-1}\right)^2 + \frac{l_y}{2l_x}\left(\frac{1}{2m-1}\right)^2}{\left(\frac{(2n-1)\pi L_p}{2l_x}\right)^2 + \left(\frac{(2m-1)\pi L_p}{l_y}\right)^2 + 1 + jw\tau_p} \quad (13)$$

where

$$L_p = \sqrt{D_p \tau_p} \quad (14)$$

is the diffusion length of the minority carrier holes in the n-type region, D_p the diffusion coefficient, τ_p the carrier lifetime, l_y the width of the n-type region, and l the lateral periodicity of the structure. The model parameters presented in Table III are representative of a n-well/p-substrate photodiode in 0.18-μm CMOS and are used for modeling in this paper, unless otherwise specified.

ACKNOWLEDGMENT

Many thanks to Alain Rousson for taking measurements.

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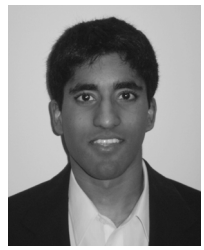

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