Practical Challenges for Electronic Dispersion Compensation in CMOS

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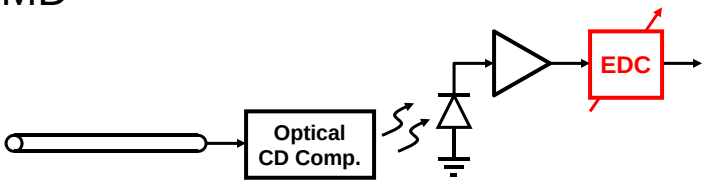
Outline

- Architectures for CMOS EDC
- Linear equalizer implementations
- Feedback equalizer implementations
- Towards 40-Gb/s DSP-based EDC
- Conclusions

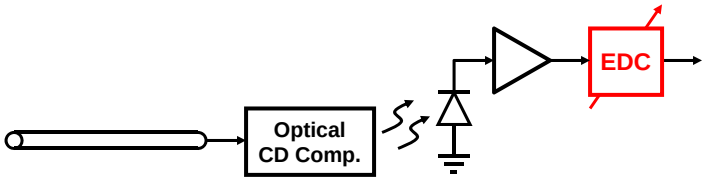
Electronic Dispersion Compensation

- Perform CD compensation optically
- PMD compensation must be adaptive to track changes over milliseconds
- ➢ Fewer taps than EDC for both CD & PMD

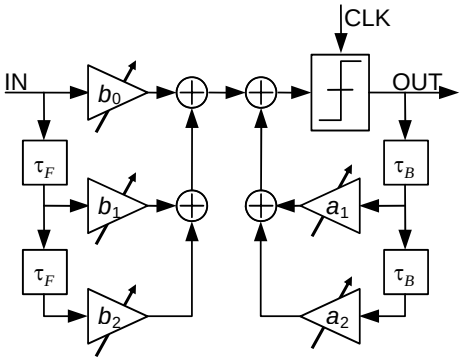


Electronic Dispersion Compensation

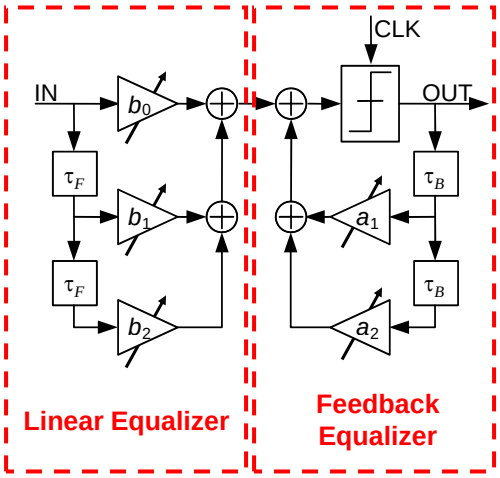
- Possibilities
  - Linear equalization
  - Decision feedback equalization
  - MLSE



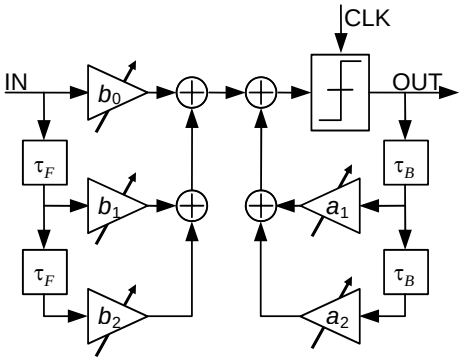
DFE Design Parameters



DFE Design Parameters



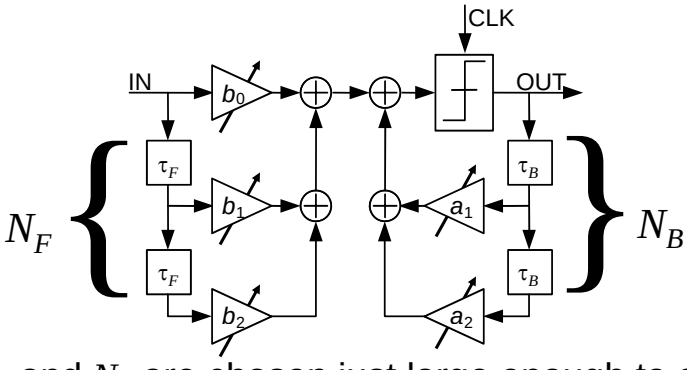
DFE Design Parameters



Challenges:

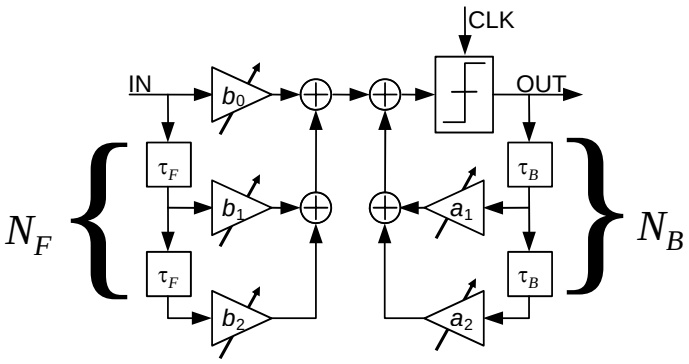
- **Inherent delay-bandwidth-gain tradeoffs**
- **Timing critical path in the feedback equalizer**
- **Extendibility of analog/mixed-signal approaches to long impulse responses**

DFE Design Parameters



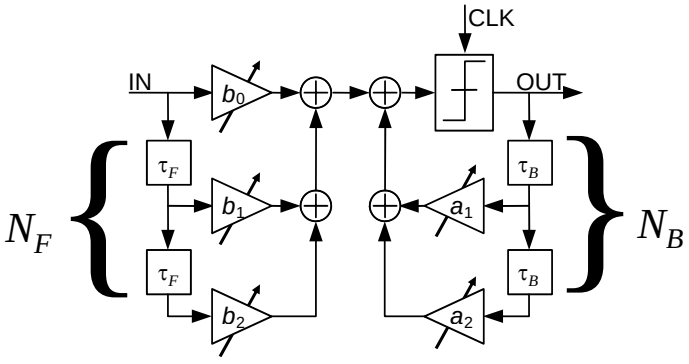
- N_F and N_B are chosen just large enough to cover the worst-case (i.e. longest) fiber pulse response

DFE Design Parameters



- τ_B is generally equal to one bit period since OUT is updated by the clock

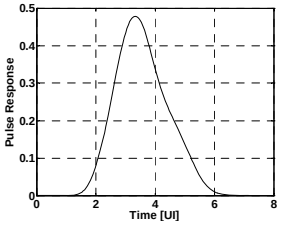
DFE Design Parameters

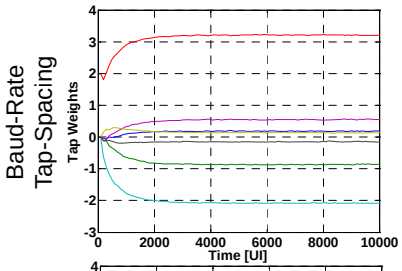


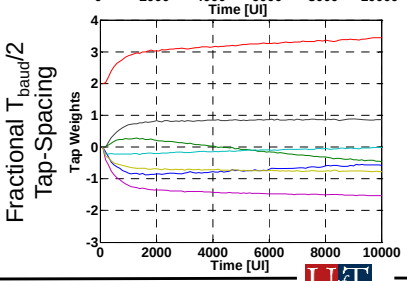
- τ_F can either be one bit period or a fraction thereof

Fractional vs. Baud-Rate Tap-Spacing

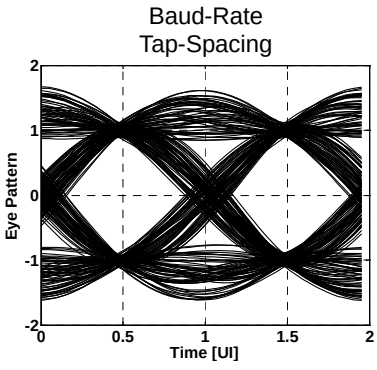
- Fractional tap-spacing introduces correlation between neighboring tap signals
- ➢ This can cause the adaptation engine to become "confused" and to converge slowly, or diverge
- Example:
  - 7-tap linear equalizer
  - Ideal LMS adaptation

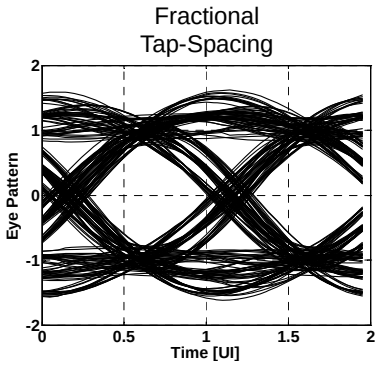






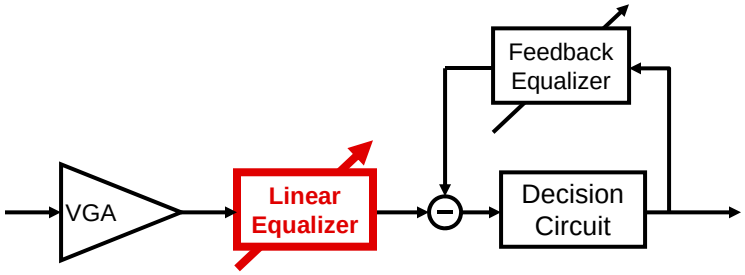
Fractional vs. Baud-Rate Tap-Spacing



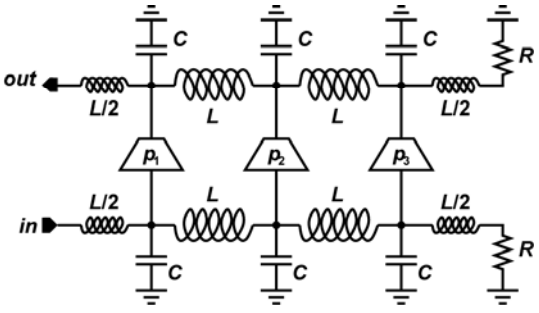


➢ Negligible difference in performance

Implementation of Linear Equalizer

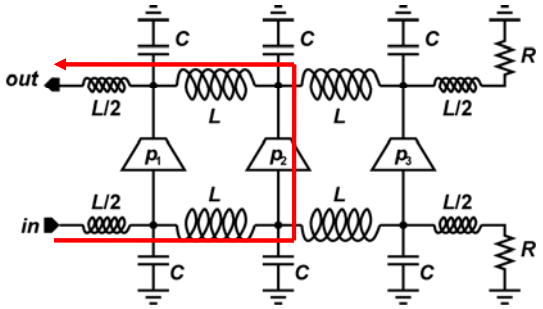


3-Tap Traveling Wave Filter

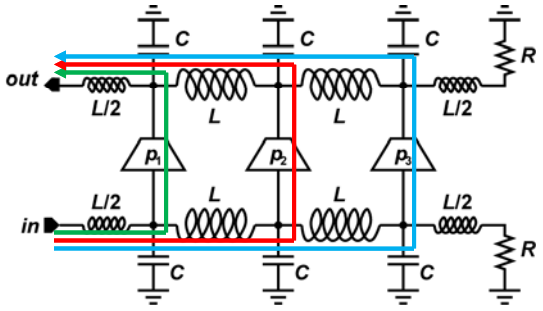


Passive delay lines consume no power

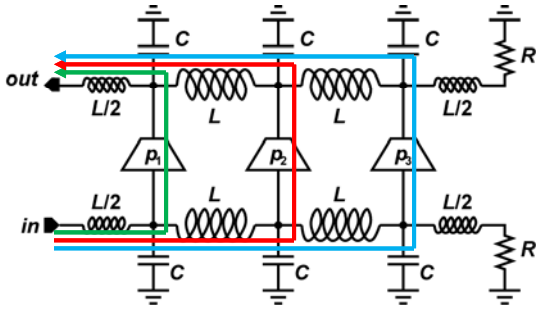
3-Tap Traveling Wave Filter



3-Tap Traveling Wave Filter



3-Tap Traveling Wave Filter



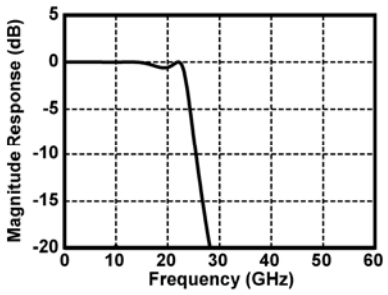
$$\text{Tap spacing}: \quad \tau = 2\sqrt{LC}$$

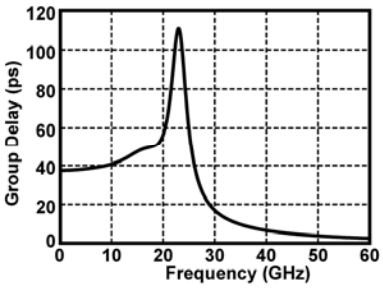
$$\text{Delay Line Bandwidth}: \quad f_{3\text{dB}} = \frac{1}{\pi\sqrt{LC}} = \frac{2}{\pi\tau}$$

$$\text{Maximum gain per tap} \propto C$$

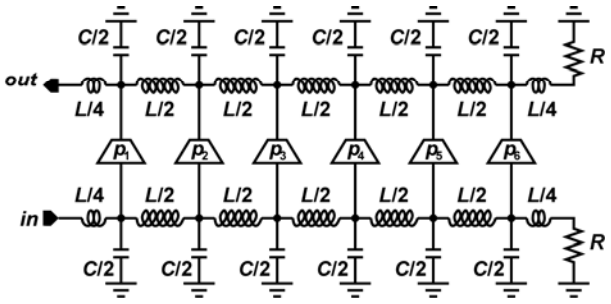
3-Tap Traveling Wave Filter

- Example: Simulated 3-section lumped-LC delay line designed for 25-ps tap spacing (baud-rate tap spacing at 40 Gb/s)





6-Tap Traveling Wave Filter



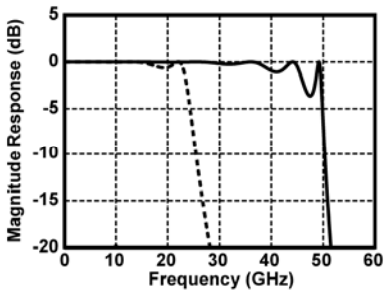
$$\text{Tap spacing}: \quad \tau = \sqrt{LC}$$

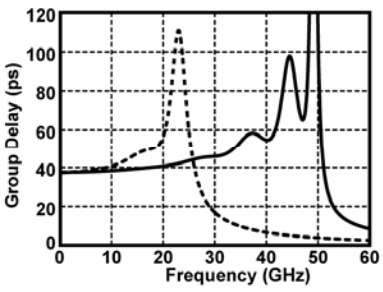
$$\text{Delay Line Bandwidth}: \quad f_{3\text{dB}} = \frac{2}{\pi\sqrt{LC}} = \frac{2}{\pi\tau}$$

$$\text{Maximum gain per tap} \propto C/2$$

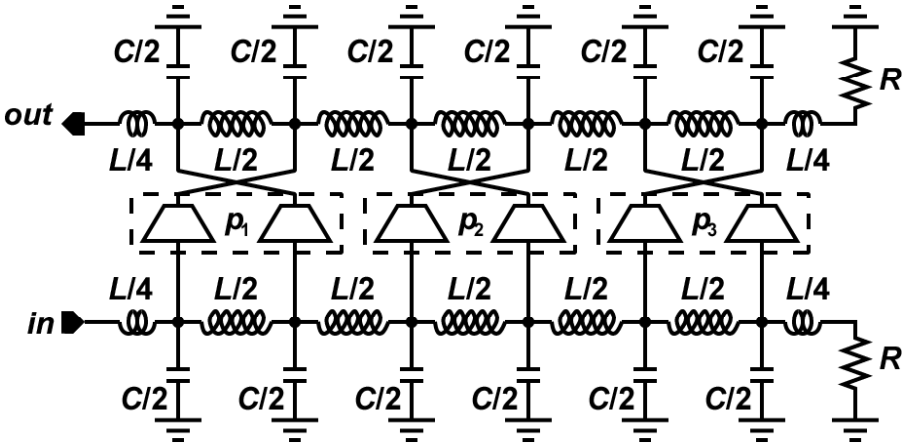
6-Tap Traveling Wave Filter

- Example: Simulated 6-section lumped-LC delay line designed for the same total delay

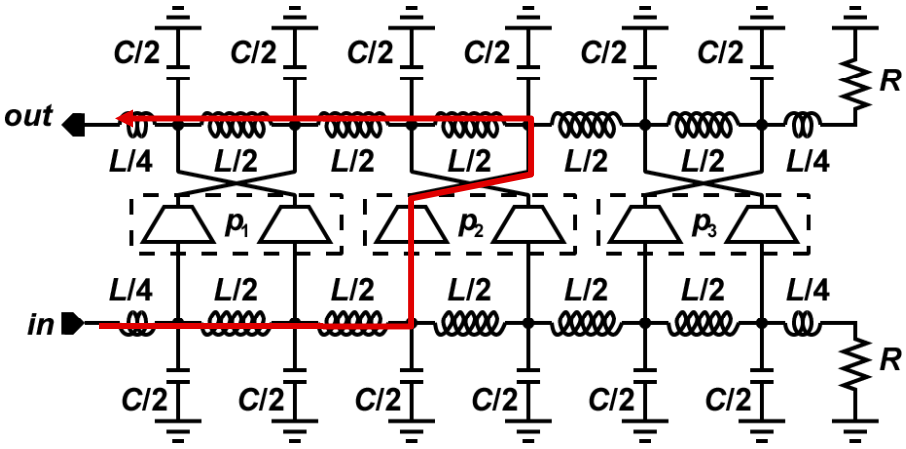




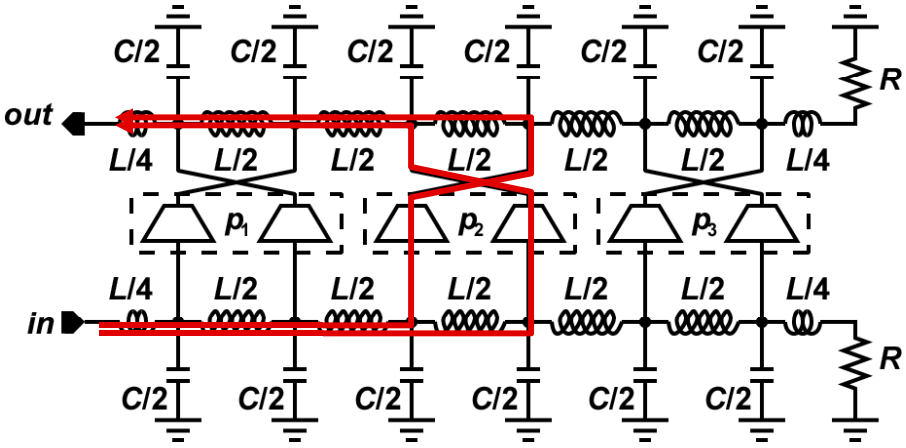
3-Tap Crossover TWF



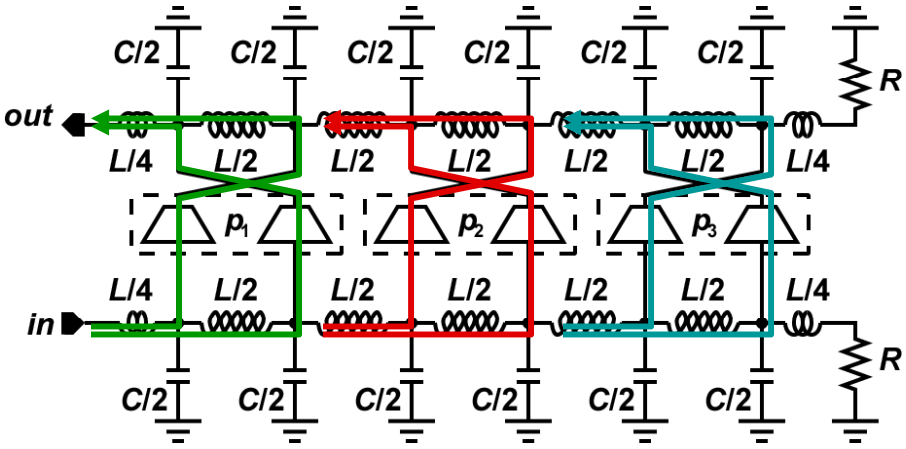
3-Tap Crossover TWF



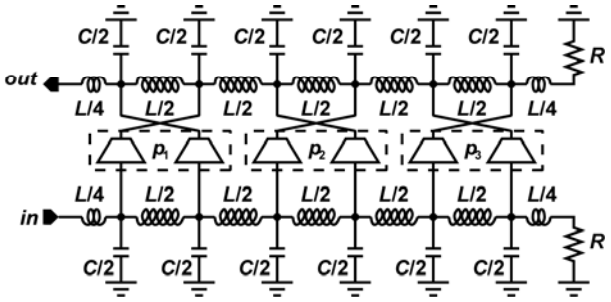
3-Tap Crossover TWF



3-Tap Crossover TWF



3-Tap Crossover TWF



Tap spacing : $\tau = 2\sqrt{LC}$

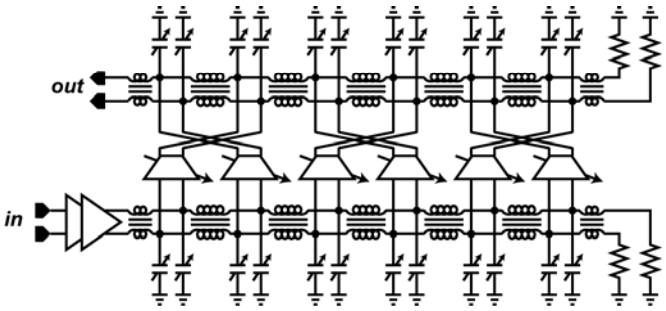
Delay Line Bandwidth : $f_{3\text{dB}} = \frac{2}{\pi\sqrt{LC}} = \frac{4}{\pi\tau}$

Maximum gain per tap $\propto C$

Summary

	Tap spacing	***Delay line bandwidth***	***Max. gain per tap***
3-tap TWF	$2\sqrt{LC}$	$\frac{1}{\pi\sqrt{LC}}$	$\propto C$
6-tap TWF	$\sqrt{LC}$	$\frac{2}{\pi\sqrt{LC}}$	$\propto C/2$
3-tap CTWF	$2\sqrt{LC}$	$\frac{2}{\pi\sqrt{LC}}$	$\propto C$

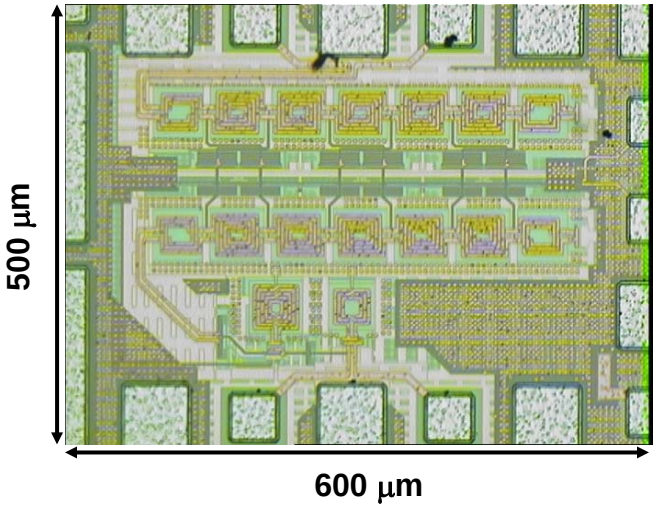
Prototype Implementation



- 90-nm CMOS process
- 24 mW from 1-V supply

30-Gb/s Equalizer in 90-nm CMOS

Jonathan Sewter, M.A.Sc.



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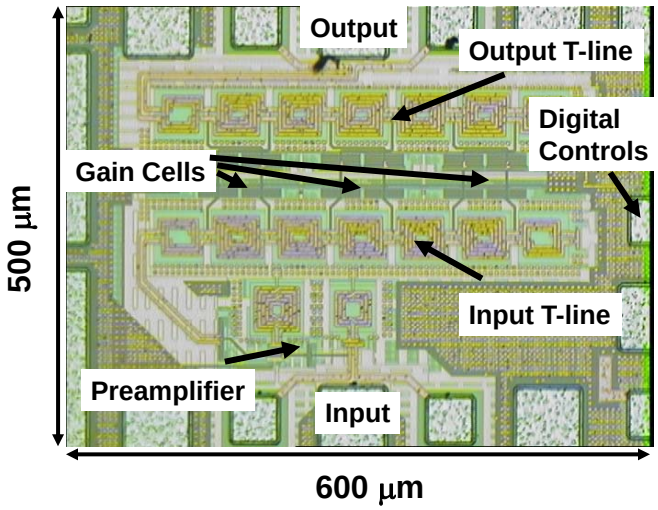
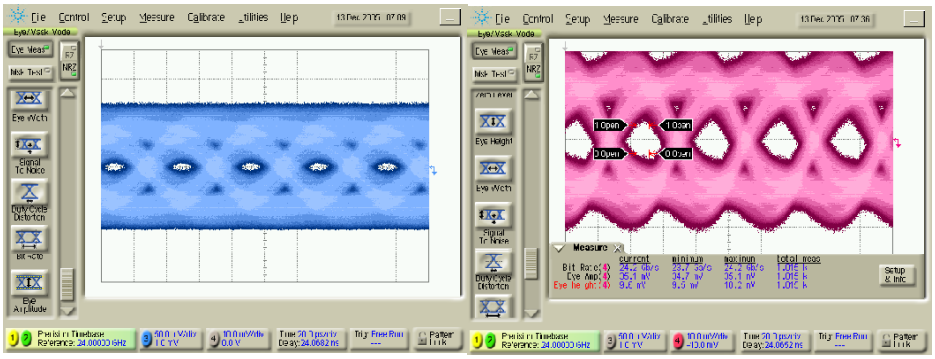
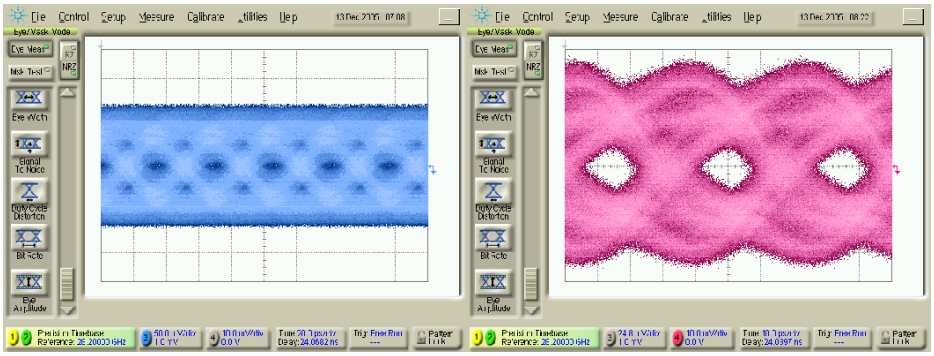


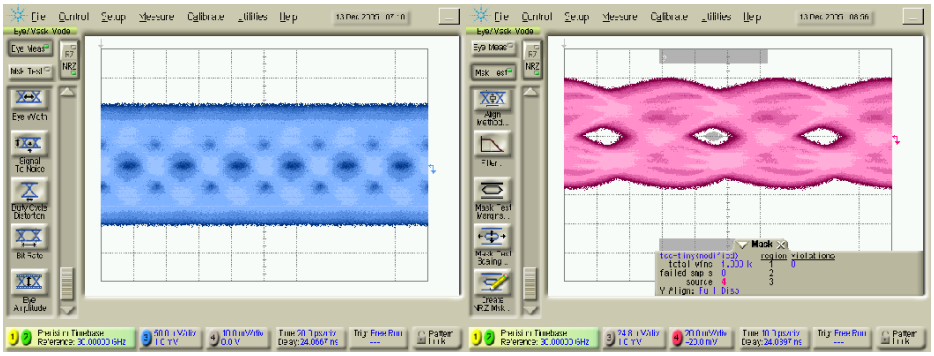
Input and output eye diagrams at 20 Gb/s over 12-dB loss channel



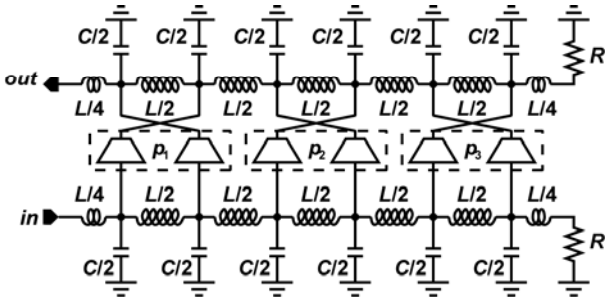
Input and output eye diagrams at 25 Gb/s over 13-dB loss channel



Input and output eye diagrams at 30 Gb/s over 14-dB loss channel



3-Tap Crossover TWF

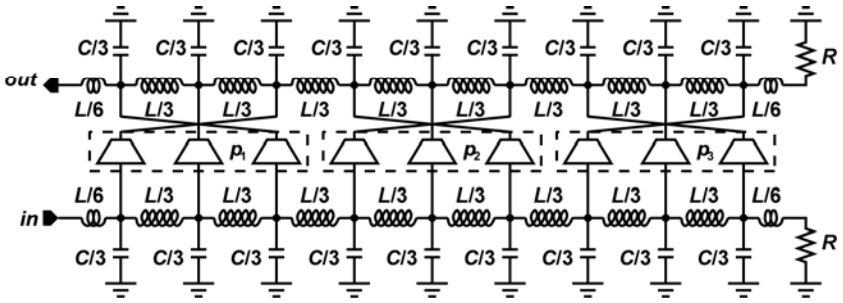


Tap spacing : $\tau = 2\sqrt{LC}$

Delay Line Bandwidth : $f_{3\text{dB}} = \frac{2}{\pi\sqrt{LC}} = \frac{4}{\pi\tau}$

Maximum gain per tap $\propto C$

3-Tap Crossover TWF

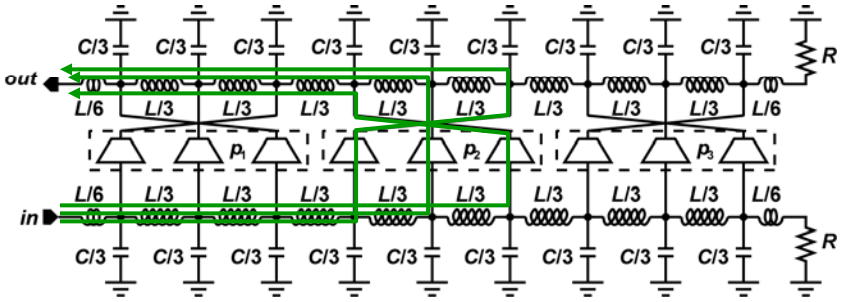


Tap spacing : $\tau = 2\sqrt{LC}$

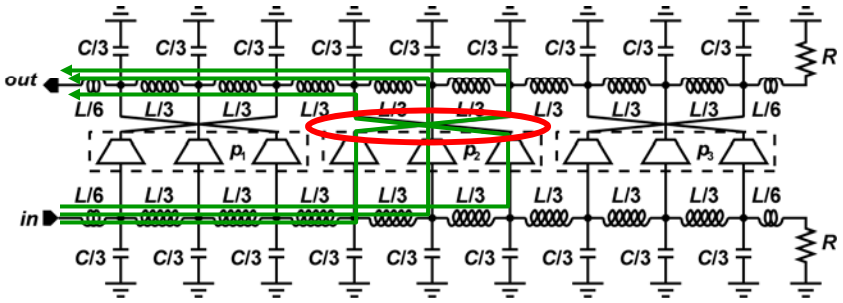
Delay Line Bandwidth : $f_{3\text{dB}} = \frac{3}{\pi\sqrt{LC}} = \frac{6}{\pi\tau}$???

Maximum gain per tap $\propto C$

3-Tap Crossover TWF

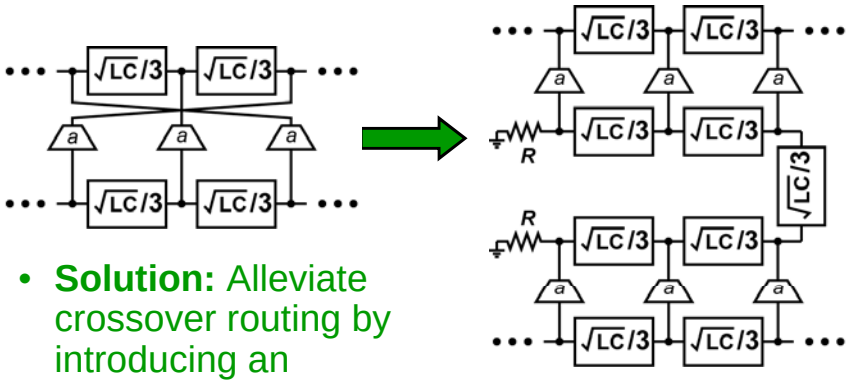


3-Tap Crossover TWF



- **Problem:** The crossover routing could introduce skew and crosstalk between paths that must be matched

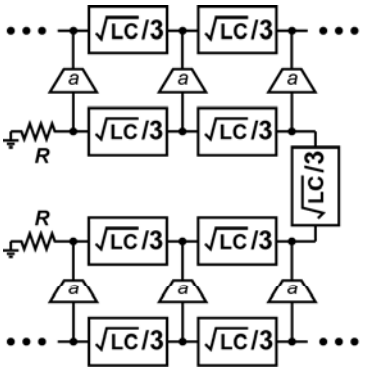
Folded-Cascade TWF



- **Solution:** Alleviate crossover routing by introducing an intermediate "folded" transmission line

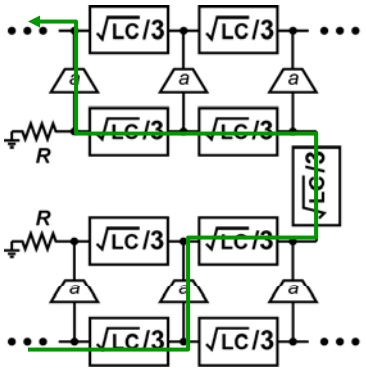
Folded-Cascade TWF

- Each path through this network goes through 5 delay sections and 2 amplifiers



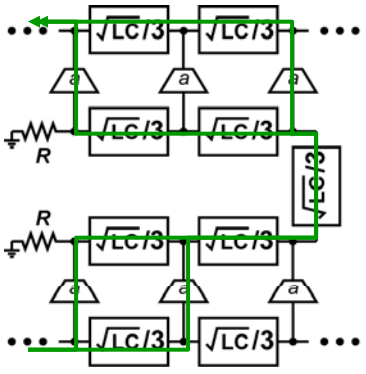
Folded-Cascade TWF

- Each path through this network goes through 5 delay sections and 2 amplifiers
- Each path has a gain of a^2 (assuming lossless delay elements)



Folded-Cascade TWF

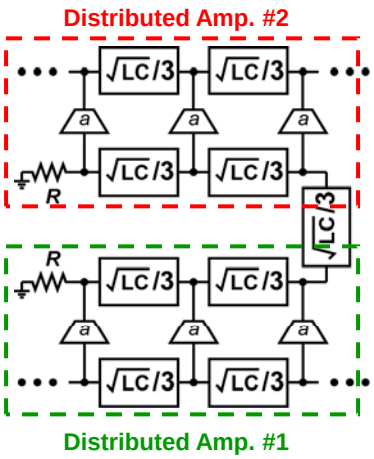
- Each path through this network goes through 5 delay sections and 2 amplifiers
- Each path has a gain of a^2 (assuming lossless delay elements)
- There are 9 such paths
- ➢ Total gain through this tap is $9a^2$



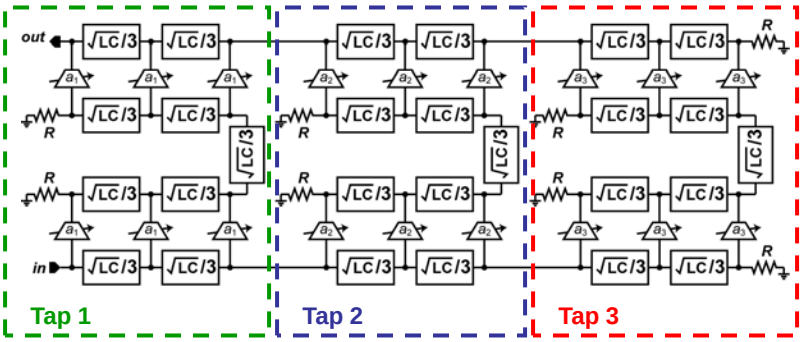
Folded-Cascade TWF

- **Alternate interpretation:** This is a cascade of 2 distributed amplifiers
- Each has a gain of 3*a* (assuming lossless delay elements)

➢ Total gain is $9a^2$



3-Tap Folded-Cascade TWF

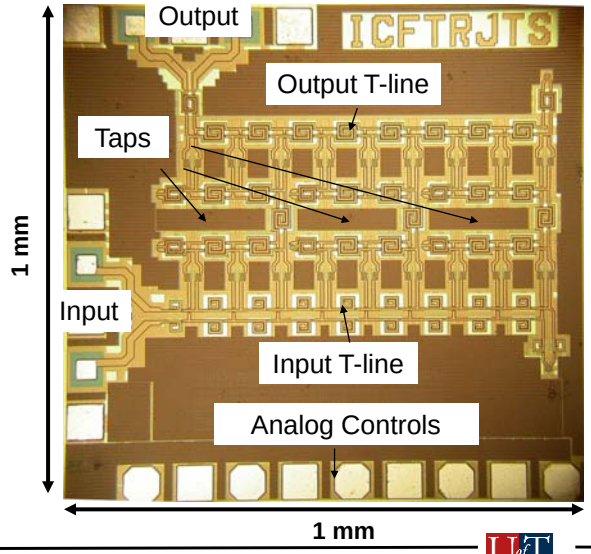


- Example: 3-tap FIR filter

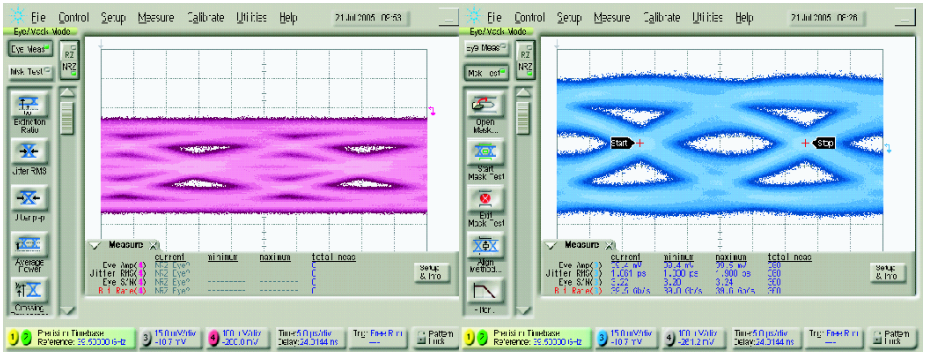
40-Gb/s Equalizer in 0.18-μm CMOS

Jonathan Sewter, M.A.Sc.

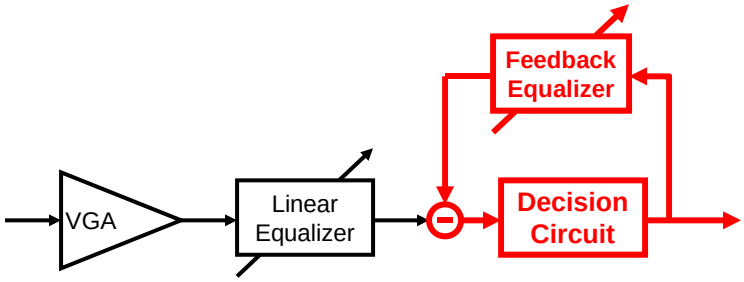
- 0.18 μm CMOS (f_T = 45 GHz)
- 3-tap filter
- Fully differential
- Analog control of tap weights
- 70 mW from a 1.8 V supply



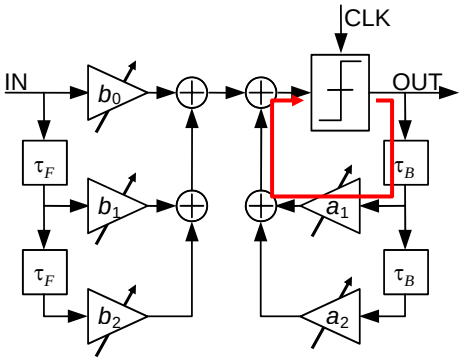
Input and output eye diagrams at 40 Gb/s over 15-dB loss channel



Implementation of Feedback Equalizer

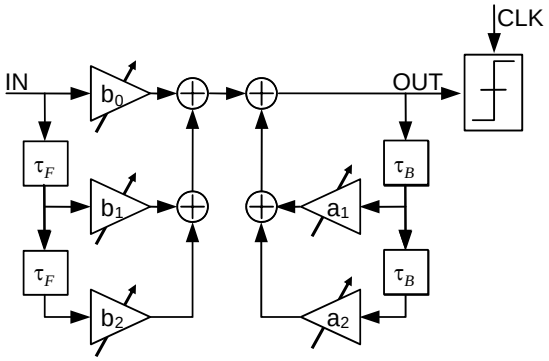


DFE Critical Path



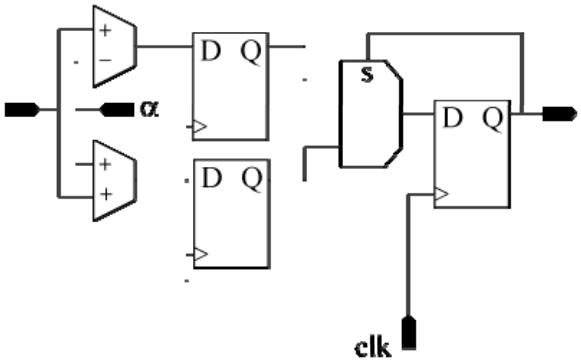
Infinite Impulse Response Filter

George Ng, M.A.Sc. candidate

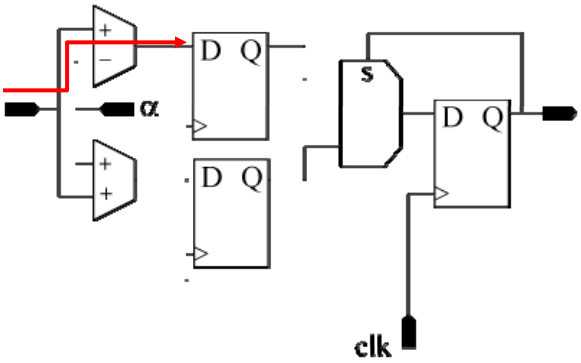


- ✓ Eliminates timing critical path
  ⇒ Broadband operation possible in CMOS
- × Possible instability of the filter
- × Complicates the adaptation algorithm

Lookahead DFE

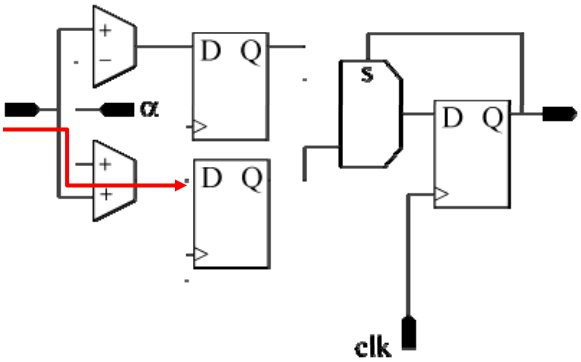


Lookahead DFE



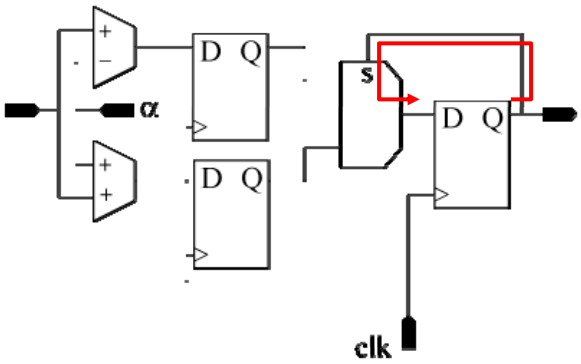
- Make a decision assuming the last bit was +1

Lookahead DFE



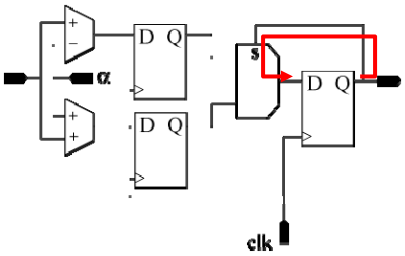
- Make a decision assuming the last bit was –1

Lookahead DFE



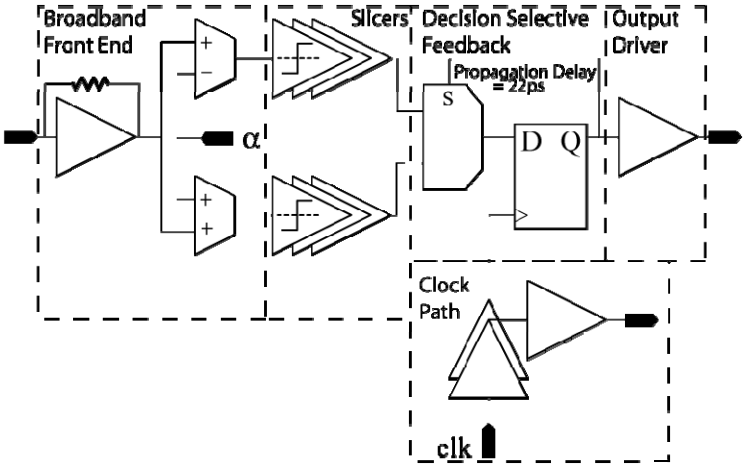
- Choose between the two digitally

Lookahead DFE

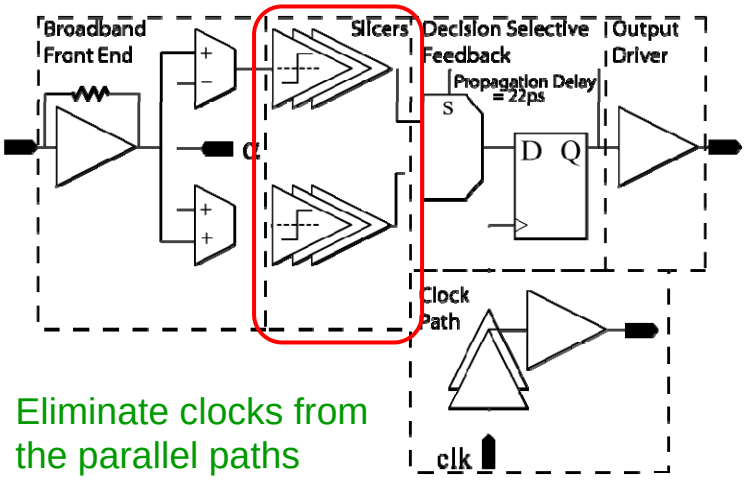


- ✓ Shortened critical path
- ✗ Parallelism demands more power consumption
- ✗ Clock distribution is a challenge

Lookahead DFE Implementation



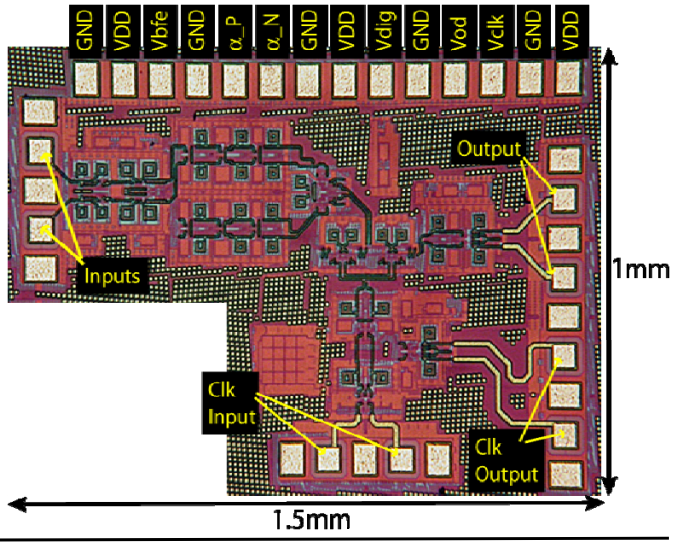
40-Gb/s 1-tap DFE Implementation



✓ Eliminate clocks from the parallel paths

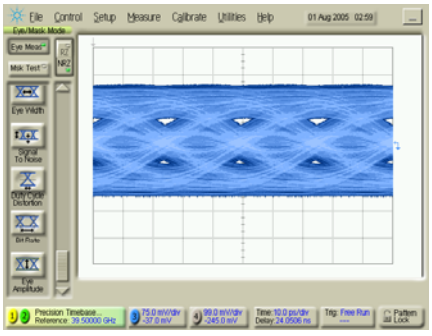
40-Gb/s Decision-Feedback Eq.

Adesh Garg, M.A.Sc. (with Prof. S. Voinigescu)

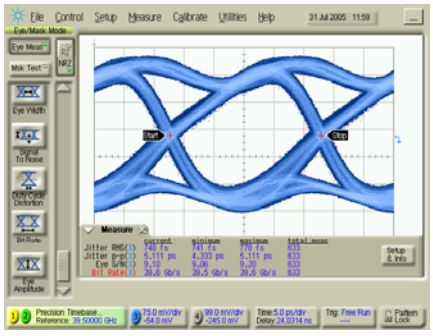


40-Gb/s Eye Diagrams

Input Eye – 9-ft Electrical Cable



Equalized Output Eye

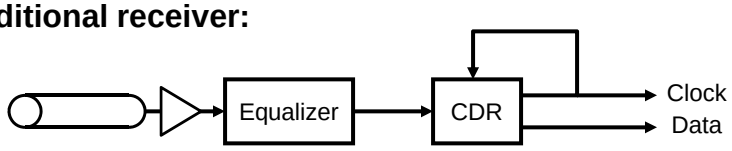


$Jitter_{pp}$ = 5.11ps; SNR = 9.1

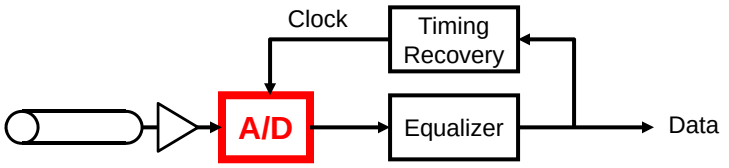
Rise time = 13.67ps; Vpp = 320mV

Towards 40-Gb/s DSP-based Receivers

Traditional receiver:

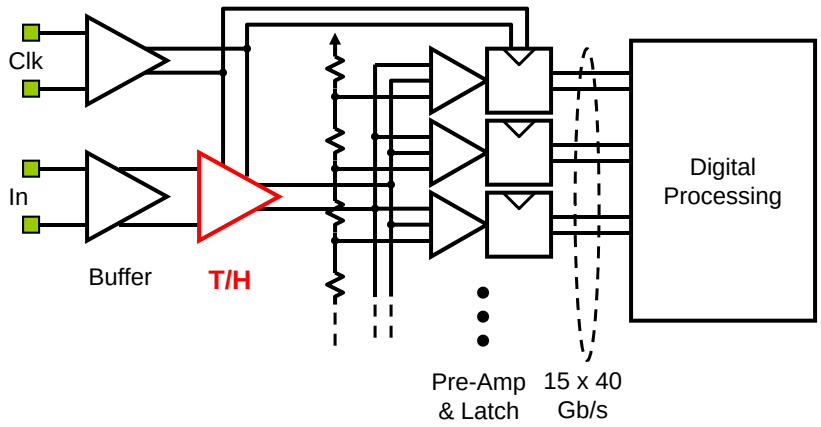


DSP-based receiver:



- **Requires 40-Gsample/sec A/D converter**

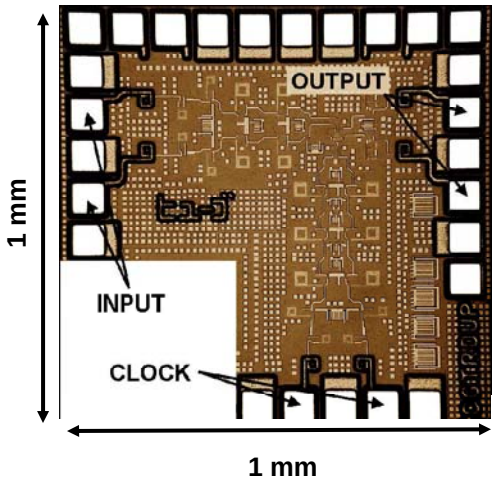
Ultra High Speed A/D Conversion



CMOS 30-GS/s Track & Hold

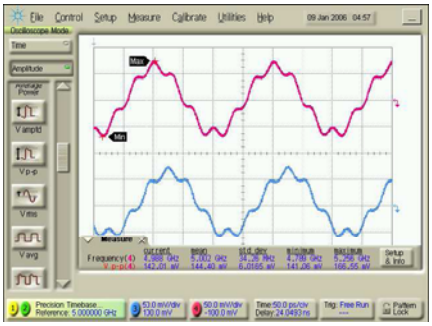
Shahriar Shahramian, Ph.D. Candidate (with Prof. S. Voinigescu)

- 0.13-μm CMOS process
- 270-mW from 1.8-V supply
- 6.5 ENOB over 7-GHz bandwidth

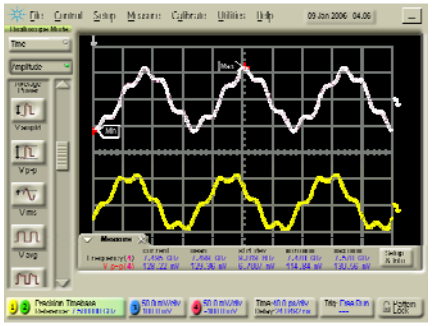


30-GSample/sec Operation

5-GHz input



7-GHz input



Summary

- Baud-rate tap-spacing in equalizers are amenable to robust adaptation
- Techniques to alleviate the inherent delay-bandwidth-gain tradeoffs in linear equalizers
- Techniques to alleviate the timing bottleneck in the feedback equalizer
- Progress towards 40-GSample/sec DSP-based equalizer