# A 3-Tap Digitally Programmable Transversal Filter in 90 nm CMOS for Equalization up to 30 Gb/s

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***Abstract*— This paper describes a fully-differential 3-tap transversal filter in 90 nm CMOS capable of equalizing NRZ data up to 30 Gb/s. A traditional traveling wave filter structure is modified to increase the filter's bandwidth. Digital programmability is provided for the tap gains, an integrated pre-amplifier, and tuning varactors. The design is 600 $\mu$m $\times$ 500 $\mu$m and draws 25 mA from a 1 V supply. It is the first reported CMOS transversal filter operating above 10 Gb/s.**

**Keywords: equalization, traveling wave filter, CMOS**

## I. Introduction

Programmable traveling wave filters (TWFs) are important building blocks in high speed communication integrated circuits. They have been used on their own and as part of decision feedback equalizers in integrated circuits for chip-to-chip [1] and optical fibre communication [2] at data rates up to 49 Gb/s. Generally, these designs have been performed in InP/InGaAs or SiGe technologies consuming several hundred mW. At 10 Gb/s, TWFs have been implemented with lower power consumption including a 7 tap (50 ps tap spacing) design in 0.18 $\mu$m SiGe BiCMOS consuming 40 mW [3] and a 4 tap equalizer with 33 ps tap spacing in 0.18 $\mu$m CMOS consuming only 7.3 mW [4].

This paper describes a fully-differential 3-tap transversal filter in 90 nm CMOS capable of equalizing NRZ data up to 30 Gb/s. A traditional traveling wave filter structure is modified so that each tap gain is comprised of the two gain circuits whose outputs superimpose with the same group delay, similar to a distributed amplifier. This greatly increases the bandwidth of the filter for a given tap spacing and gain. Differential (coupled) inductors are used to implement the delay lines passively with low power (25 mW from a 1 V supply) and relatively low area (600 $\mu$m $\times$ 500 $\mu$m). This is the first reported CMOS transversal filter operating above 10 Gb/s.

## II. Crossover Traveling Wave Filter Topology

The basic TWF topology is shown in Figure 1 (single-ended). It implements a transversal filter using transmission lines as passive delay elements. To achieve the delays required for a 10 – 40 Gb/s equalizer, the transmission lines used must be very long (on the order of several millimeters). As a result, the circuit area can become prohibitively large. In addition, long transmission lines may introduce significant series loss. By using artificial transmission lines made up of lumped inductors and capacitors, the total wirelength required to achieve a given delay is reduced. Thus, the chip area and resistive losses may be reduced.

The delay $\Delta T$ of each lumped LC section is approximately equal to:

$$\Delta T = \sqrt{L'C'} \tag{1}$$

where $L'$ and $C'$ are the inductance and capacitance per section of the transmission line. The 3-dB bandwidth of a lumped LC transmission line section is equal to:

$$f_{3\text{dB}} = \frac{1}{\pi\sqrt{L'C'}} \tag{2}$$

For a TWF, the tap spacing is equal to the delay through two LC sections.

$$\tau = 2\Delta T = 2\sqrt{L'C'} \tag{3}$$

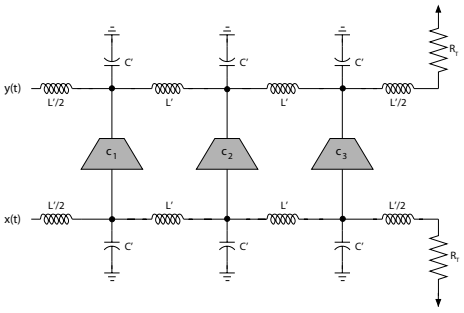


Fig. 1. A 3-tap traveling wave filter (TWF).

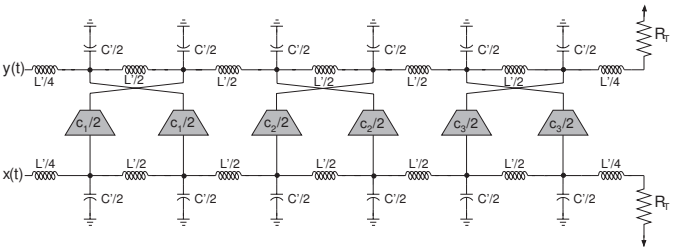


Fig. 2. A 3-tap TWF using a crossover topology.

In Figure 2 each LC section is replaced with two sections having component values of $L'/2$ and $C'/2$ to maintain the same characteristic impedance. Hence, the delay through each section is halved while the bandwidth is increased. At data rates that push the technology's limits, the capacitances $C'$ are comprised mostly of the transconductors' parasitic input and output capacitances. Therefore, reducing these capacitances to $C'/2$ implies scaling the size and gain of each transconductor by one-half. Fortunately, by crisscrossing the outputs of consecutive transconductors, their gains add with equal group delay effectively forming a distributed amplifier. Furthermore, each tap delay is now formed by four LC sections (instead of two) giving the same tap spacing as the conventional TWF topology.

$$\tau_{\text{crossover}} = 4\Delta T_{\text{crossover}} = 4\sqrt{\frac{L'}{2}\frac{C'}{2}} = 2\sqrt{L'C'} = \tau \tag{4}$$

Hence, the crossover TWF topology in Figure 2 maintains the same tap spacing and gain as in the traditional traveling wave topology in

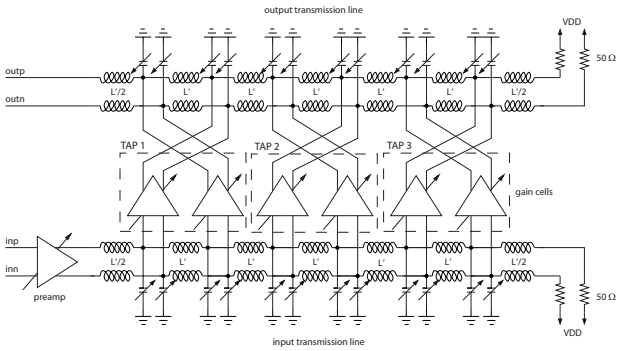


Fig. 3. Symbolic top-level schematic of the fabricated 90-nm equalizer IC.

Figure 1, but with greater bandwidth.[1]

## III. Circuit Design

A block diagram of the entire circuit is given in Figure 3. The circuit is fully-differential and has been designed for use with a 100 Ω (differential) system impedance.

A lumped preamplifier stage accepts differential inputs and performs a variable gain function to condition the input signal so as to maximize the dynamic range of the equalizer. It also performs a single-ended to differential conversion function when the circuit is driven by an unbalanced input.

The preamplifier drives the differential input transmission line. Three gain cells tap this transmission line at intervals and drive an output differential transmission line. All transmission lines are made up of lumped capacitors and differential inductors.

Not shown in Figure 3 is the digital control path. Each of the variable elements shown in Figure 3 is controllable through a set of registers which can be loaded serially.

### A. Preamplifier

A schematic of the lumped preamplifier stage is given in Figure 4. The preamplifier consists of two cascaded differential pairs. The inputs of the first differential pair are terminated by 50 Ω loads for input matching to the 100 Ω (differential) system impedance. A differential inductor is placed in series with the 50 Ω loads to partially compensate for the large input capacitance, allowing a better input match over a larger bandwidth. The first differential pair is loaded with 100 Ω resistors, which allow it to provide reasonable gain. Another differential inductor is used in series with the 100 Ω resistors to extend the bandwidth of the first stage to over 30 GHz (simulated). The second differential pair acts as an open-drain line driver, driving the input signal onto the input transmission line. The gain of the preamplifier stage is digitally-controllable. This gain control is provided both to allow tuning of the preamplifier bias currents for performance optimization and to allow compensation for possible variations in input power. The current source of each differential pair in the preamplifier is controlled by a single digitally-controllable 6-bit switched-resistor current mirror.

### B. Gain Cell

A schematic of the gain cell is given in Figure 5. Two of the gain cells shown in Figure 5 are combined using the crossover technique to implement a single tap of the filter.

[1]If the transconductor outputs were not crisscrossed, the result would be a 6-tap filter with one-half the tap spacing and 6 dB less gain per tap.

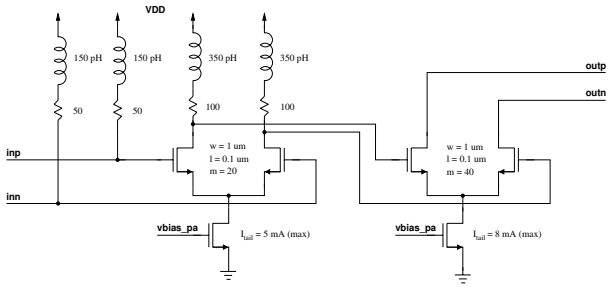


Fig. 4. Circuit schematic of preamplifier block.

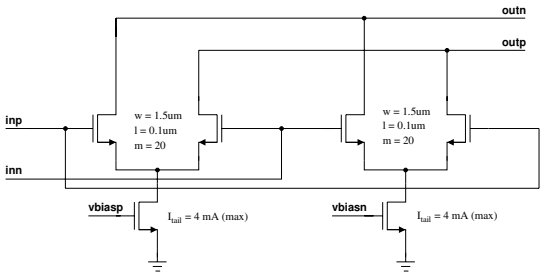


Fig. 5. Circuit schematic of variable gain cell.

Each of the gain cells is composed of two differential pairs. The two differential pairs are connected with opposite polarity. This allows the filter to implement both positive and negative tap weights. For instance, to implement a positive tap weight, the bias current for the differential pair connected with negative polarity is zeroed leaving only the positive path from input to output. The tap weights are controlled digitally with 6 bits in the same manner as the preamplifier gain is controlled.

The size of the differential pair transistors has been chosen such that a balance is reached between the competing objectives of maximum gain and maximum tuning ability. The capacitance at each node is fixed for a given characteristic impedance and tap spacing, and is made up of the device capacitances, wiring capacitances and a variable capacitance which is added to the node to allow tuning of characteristic impedance and delay. For large gain, the transistors should make up a large portion of the node capacitance. However, the varactors should also be made large to maximize the tuning ability. For this circuit, the transistors are sized to provide approximately 65% of the total node capacitance, with the remainder provided by the varactors.

The maximum current that can be drawn by all three taps is limited to 8 mA by the requirement that the output common-mode voltage must not drop below approximately 0.8 V. Therefore, the current through any particular gain cell can range from 0 when the tap is off to 4 mA when the tap is fully on (two gain cells drawing 4 mA each).

### C. Input and Output Transmission Lines

An inductance of 312.5 pH per side and a capacitance of 125 fF per side was chosen to provide a 100 Ω differential characteristic impedance and a nominal tap spacing of 25 ps. The inductances are implemented by differential spiral inductors. These reduce the area dramatically compared to designing two separate paths with uncoupled inductors. They also reduce the wirelength required for a given inductance, thereby reducing series losses along the transmission line.

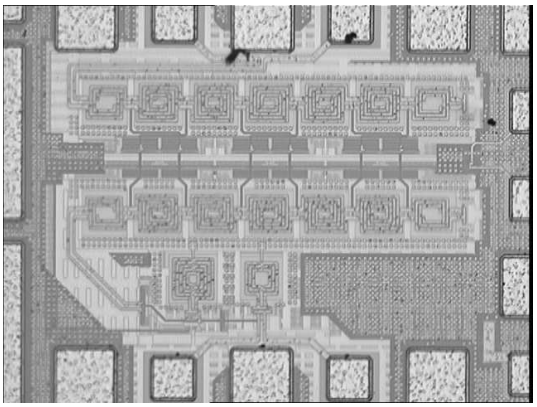

Fig. 6. Equalizer die photo.

The capacitances at each node are composed of the device capacitances attached to the node supplemented by a digitally-controllable varactor to allow tuning of the transmission line characteristic impedance and delay. These varactors are composed of switched capacitors built using the top four metal layers of the IC process. On each layer, two interdigitated structures form the two capacitor plates. Between each consecutive layer, the orientation of the two plates is reversed. This capacitor achieves high capacitance per unit area because it makes use of both the horizontal capacitance between interdigitated structures, and the vertical capacitance between adjacent metallization layers [5]. A binary weighted array of these capacitors provides 5 bits of control for the input and output transmission lines separately. Each side of the differential transmission lines are terminated using fixed 50 $\Omega$ poly resistors.

### *D. Circuit Layout*

The circuit was fabricated in a TSMC 90 nm CMOS process. A die photo of the circuit layout is provided in Figure 6. The two transmission lines are easily discerned, with the tap gains appearing between them. The differential input enters at the bottom of the circuit and the output is taken from the top, with power and digital control provided from the right. The overall dimensions of the equalizer IC are 600 $\mu$m x 500 $\mu$m.

## IV. Measurement Results

All circuit measurements were made on-wafer. The digital varactors were manually tuned to achieve a 100 $\Omega$ differential characteristic impedance by looking at the circuit's output return loss. The best match was achieved by minimizing the capacitance of all digital varactors, indicating that the internal node capacitances were greater than accounted for during simulation. Figure 7 shows the input and output return losses measured after tuning. It shows an input return loss better than -16 dB and the output return loss is better than -9 dB up to 30 GHz. The digital varactors were then fixed for the remainder of the testing.

Figure 8 shows the tap delays measured with a 10 GHz sinusoidal input. The tap spacings are 37 ps. This is larger than the 25 ps designed for, also indicating that the internal node capacitances were underestimated during simulation.

Figure 9 shows the magnitude response of each tap measured with a two-port network analyzer. Since the measurements are single-ended, the differential gains would be 6 dB greater than shown here. The increase in tap gains near dc is due to the transmission lines' series losses which appear as an additional resistive load in series with the termination resistors at low frequencies.

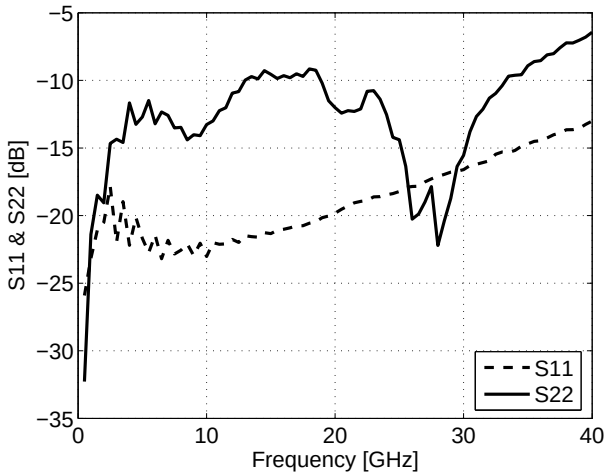


Fig. 7. Measured input and output return loss of the equalizer.

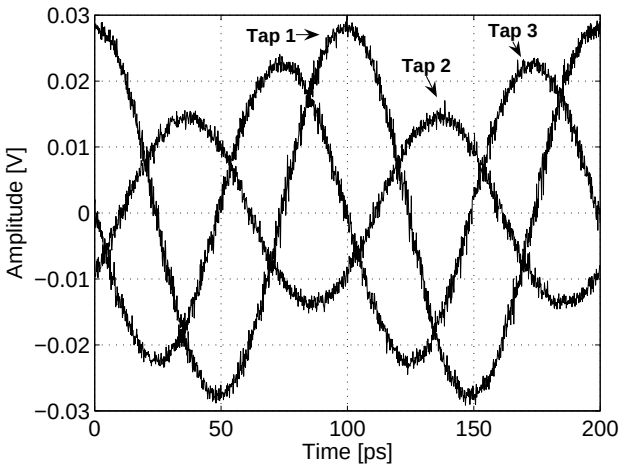


Fig. 8. Measured tap delays with a 10 GHz sinusoidal input.

Figures 10, 11 and 12 show the filter being used to equalize NRZ PRBS $2^{31}-1$ data transmitted over 4 meters of an SMA cable at 20 Gb/s, 25 Gb/s and 30 Gb/s. In each case, the tap gains were manually adjusted to open the eye at the equalizer output. No adaptation circuitry was integrated in the design. Again, the testing was performed with single-ended inputs and outputs.

## V. Conclusion

The design of a fully-differential 3-tap transversal filter in 90 nm CMOS was described. A traditional traveling wave filter topology was modified to increase the filter's bandwidth. A tap spacing of 37 ps is achieved using a passive LC delay line with differential inductors and digitally programmable capacitors for tuning. The tap weights and an integrated pre-amplifier have individually digitally programmable gains. The input return loss is better than -16 dB and the output return loss is better than -9 dB up to 30 GHz. The design is 600 $\mu$m $\times$ 500 $\mu$m and draws 25 mA from a 1 V supply. This is the first reported CMOS transversal filter operating above 10 Gb/s. Equalization of

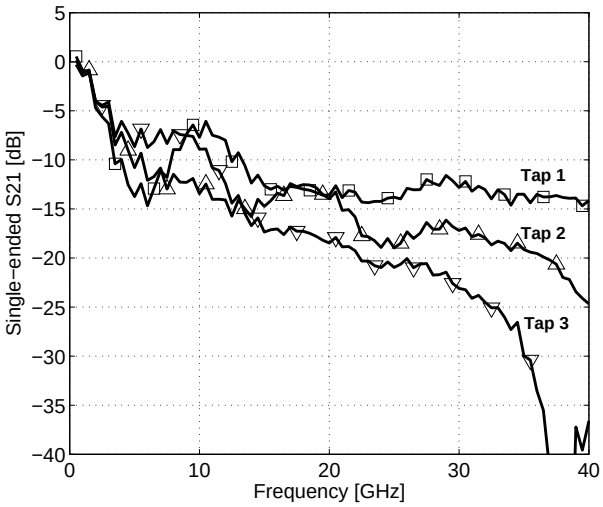


Fig. 9. Single-ended $S_{21}$ measurements. (For differential $S_{21}$, add 6 dB.)

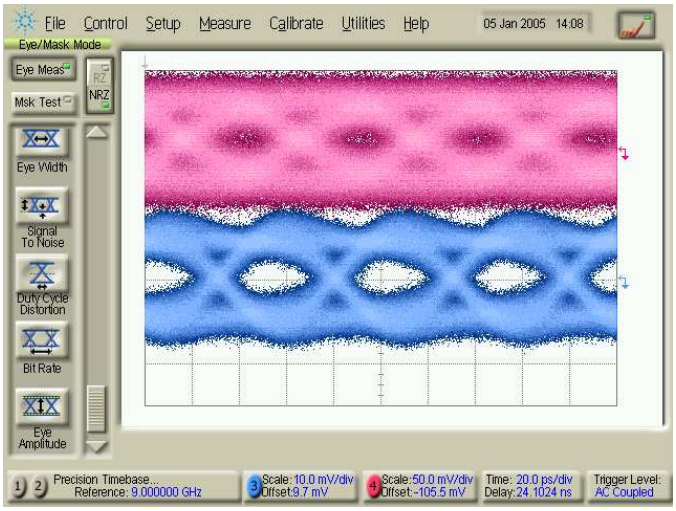


Fig. 10. Eye diagrams for 20 Gb/s data transmitted over 4 meters of SMA cable (top) and at the equalizer output (bottom).

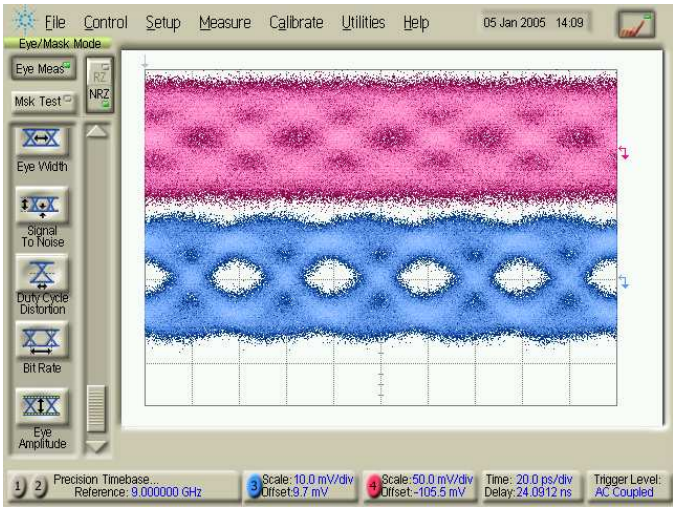


Fig. 11. Eye diagrams for 25 Gb/s data transmitted over 4 meters of SMA cable (top) and at the equalizer output (bottom).

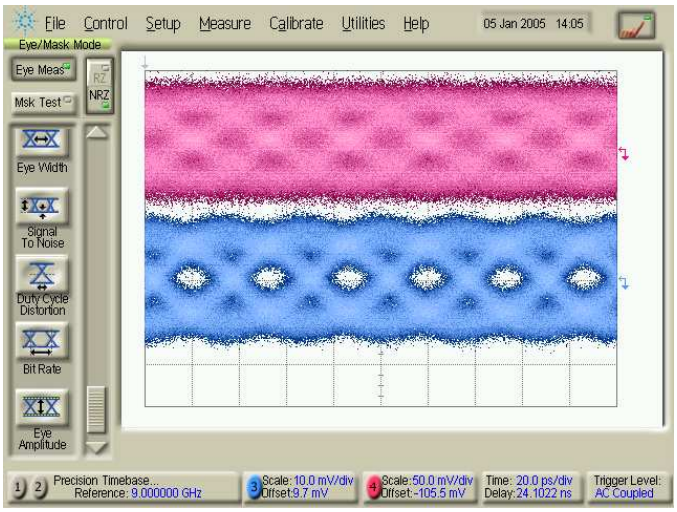


Fig. 12. Eye diagrams for 30 Gb/s data transmitted over 4 meters of SMA cable (top) and at the equalizer output (bottom).

NRZ data over a 4 meter SMA cable was demonstrated up to 30 Gb/s making it faster than any previously reported CMOS equalizers.

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