A 3-Tap Digitally Programmable Transversal Filter in 90-nm CMOS for Equalization up to 30 Gb/s

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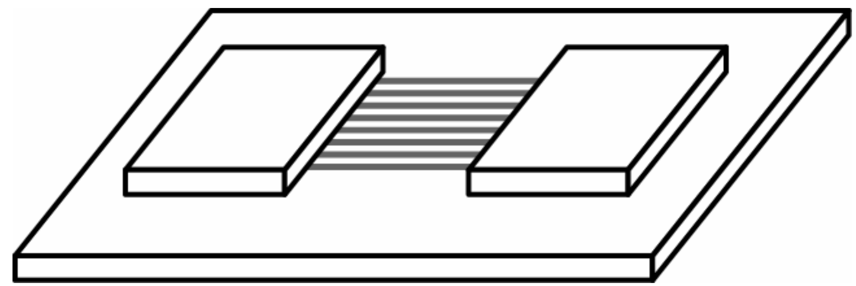
Outline

- Background on lumped-LC traveling wave filters
- “Crossover” traveling wave filter topology
- Prototype design in 90-nm CMOS
- Measurements
- Conclusions

Applications

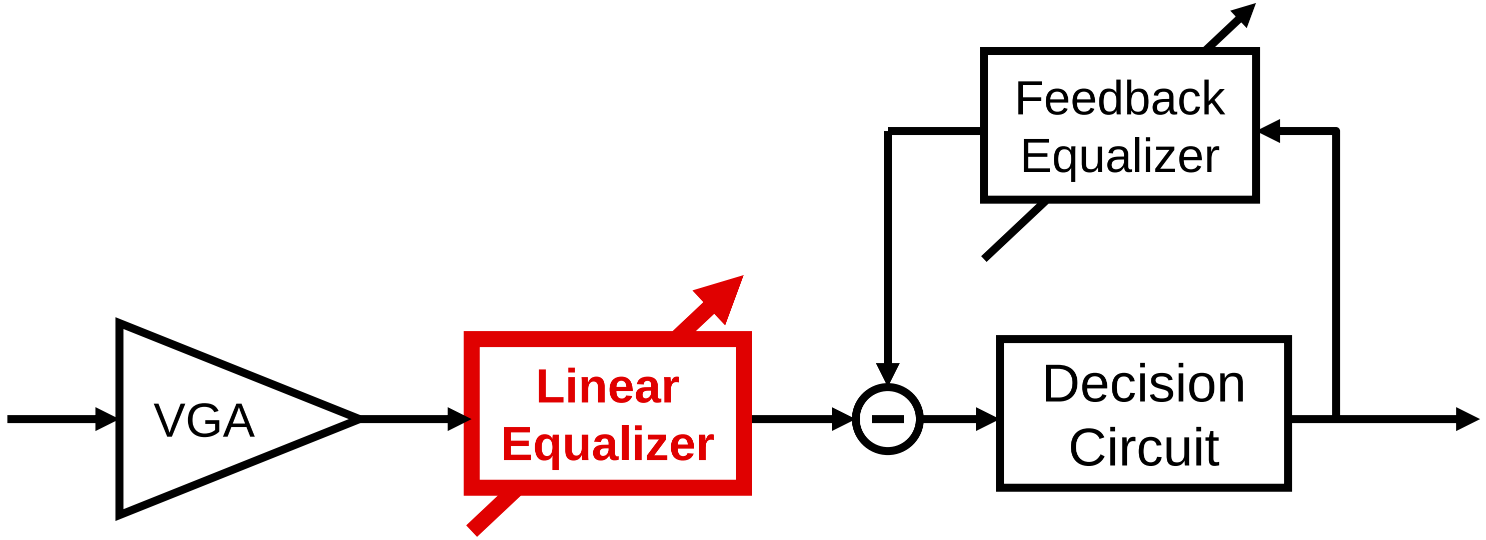
- Chip-to-chip communication
  - losses and reflections



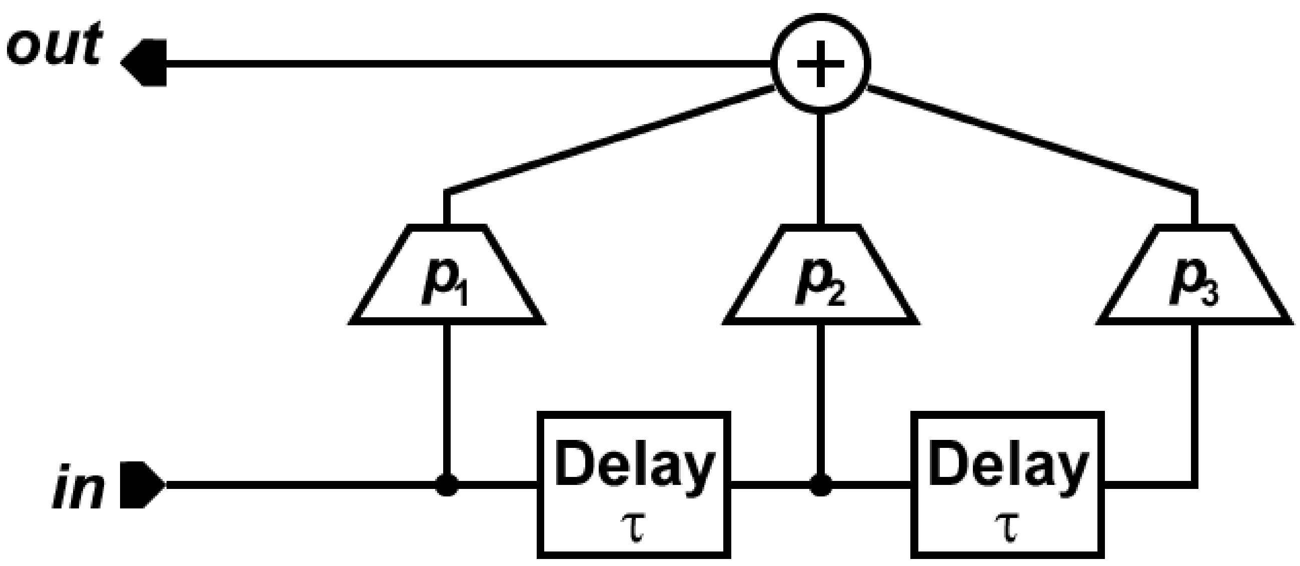
- Optical fibre
  - dispersion

Equalization

- This work focuses on the programmable filter required for linear equalization at a receiver

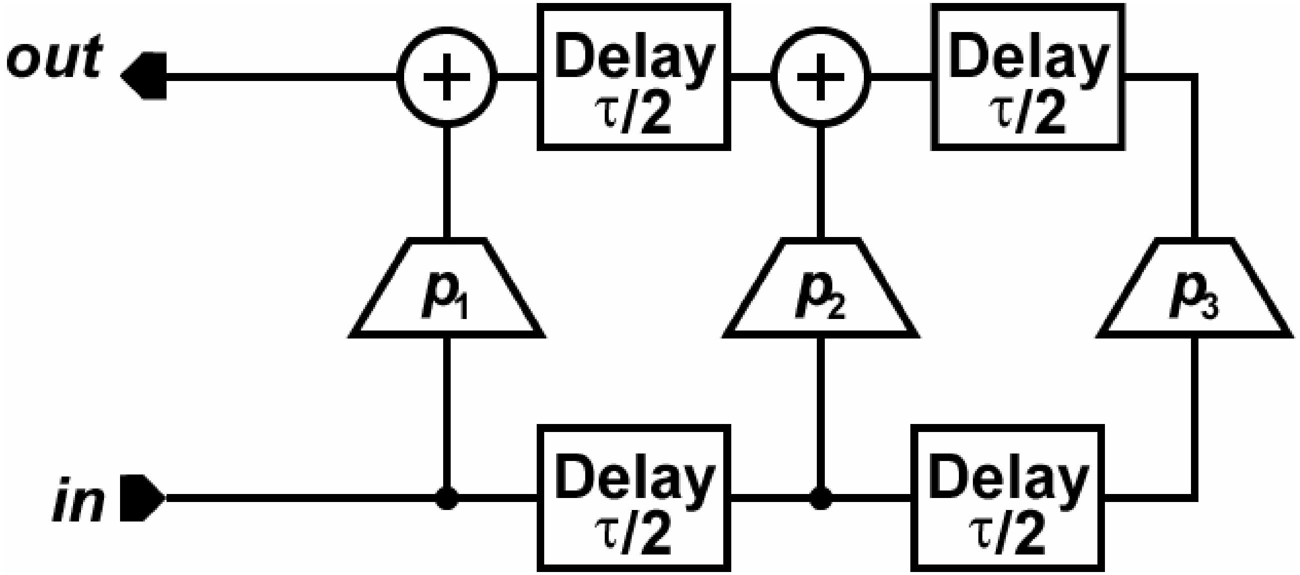


Transversal Filter



- Challenges:
  - Routing the outputs together
  - Bandwidth of the output summing node

Traveling Wave Filter



- Challenge: Implementation of the delays

Delay Implementation

Active:

- Buffer or active filter with constant gain & group delay

✘ Power consumption

Passive:

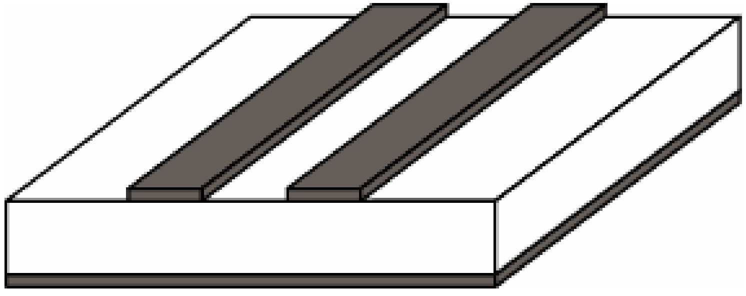
- Transmission line or lumped-LC

✘ Area

✘ Losses

Passive Delays

Transmission lines

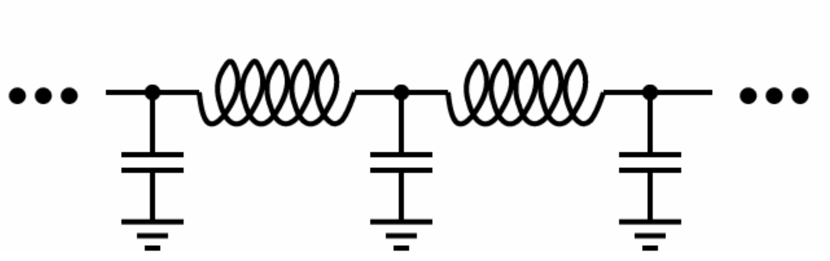


- Several mm needed to achieve the required delays

✗ Large area

✗ Series losses

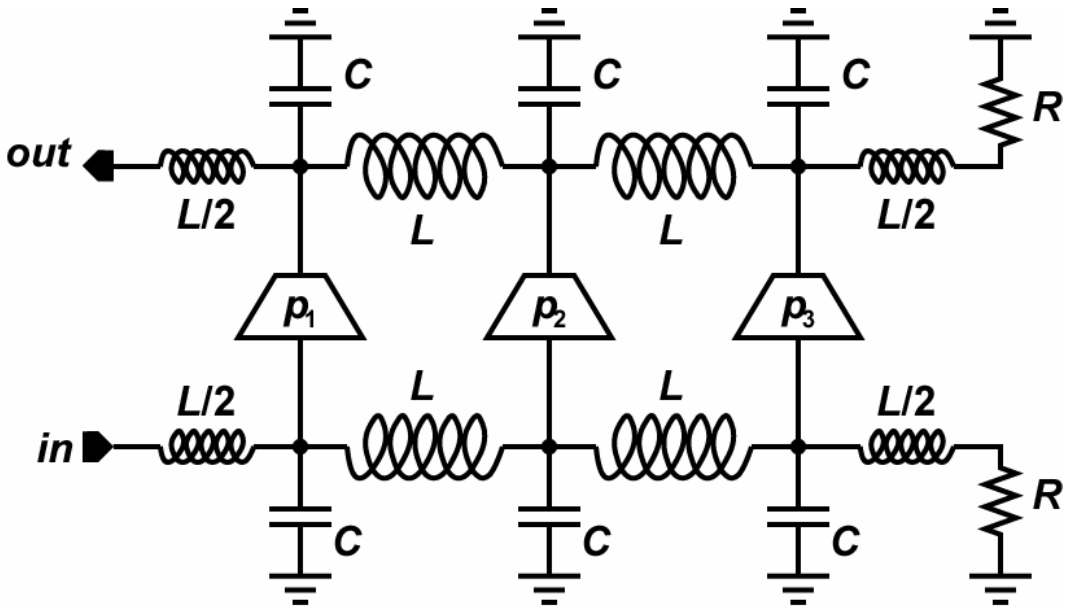
Lumped-LC



- Forms a lowpass network

✗ Limited bandwidth

3-Tap Traveling Wave Filter



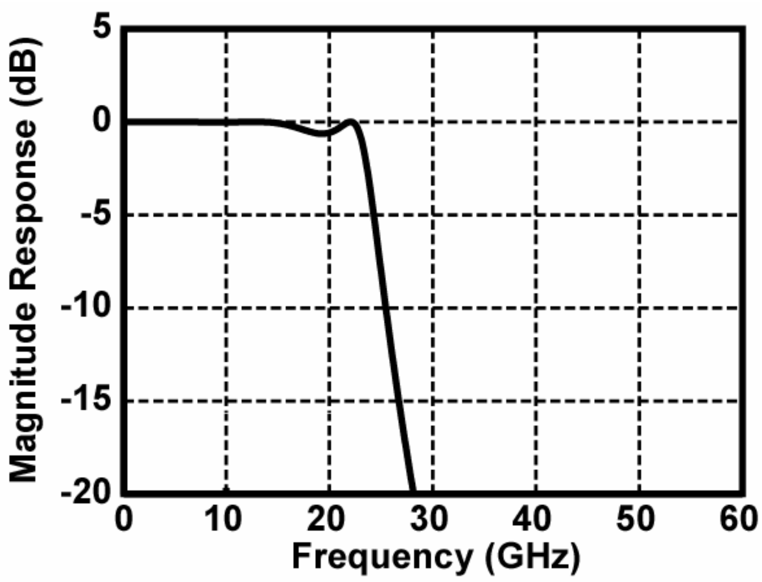
$$\text{Tap spacing: } \quad \tau = 2\sqrt{LC}$$

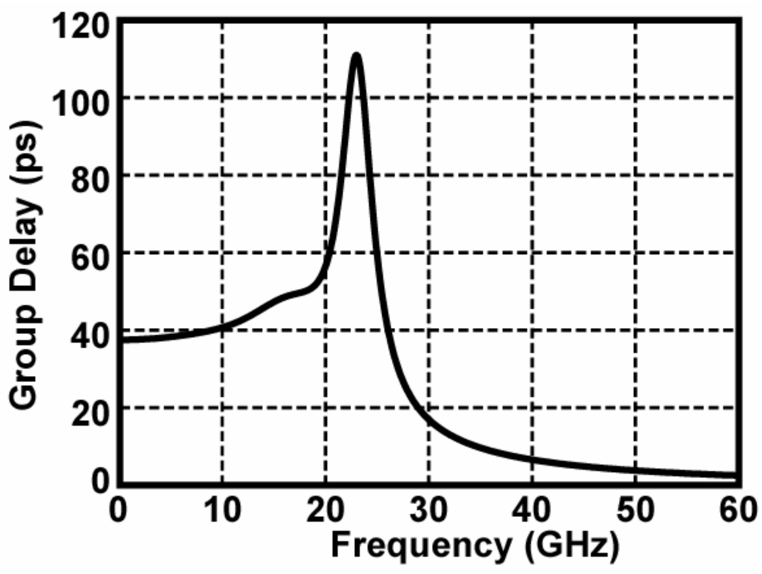
$$\text{Delay Line Bandwidth: } \quad f_{3\text{dB}} = \frac{1}{\pi\sqrt{LC}} = \frac{2}{\pi\tau}$$

$$\text{Maximum gain per tap } \propto C$$

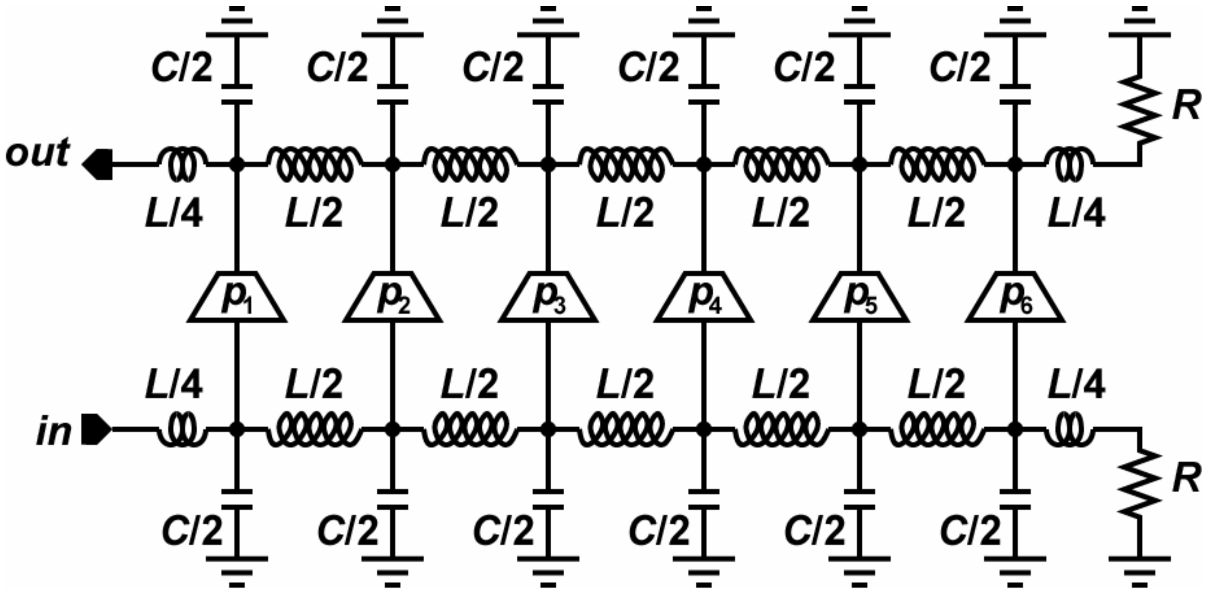
3-Tap Traveling Wave Filter

- Example: Simulated 3-section lumped-LC delay line designed for 25-ps tap spacing





6-Tap Traveling Wave Filter



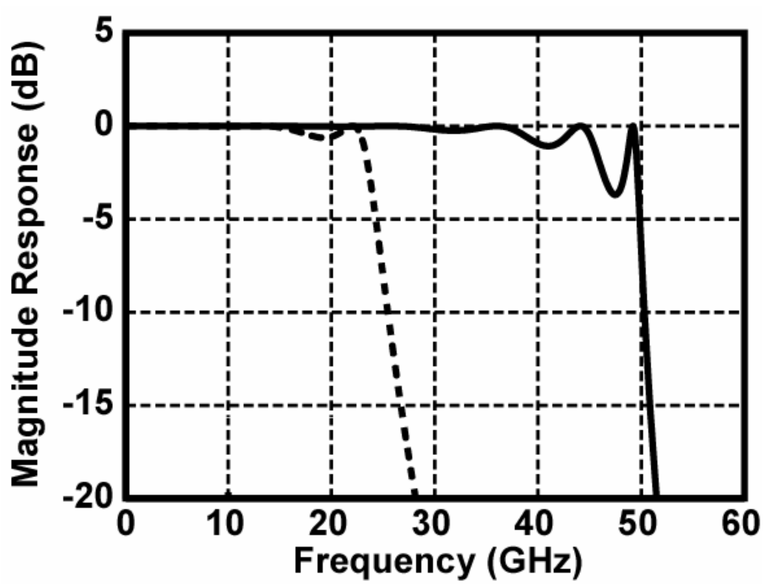
$$\text{Tap spacing:}\quad \tau = \sqrt{LC}$$

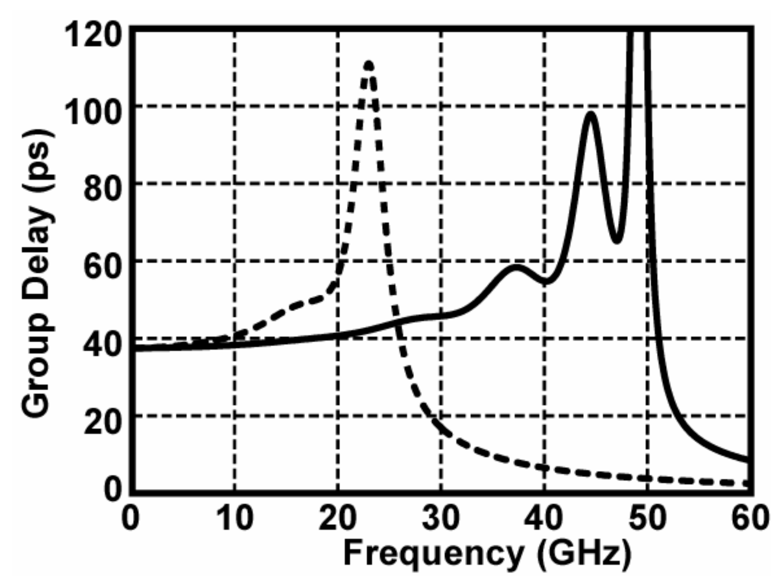
$$\text{Delay Line Bandwidth:}\quad f_{3\text{dB}} = \frac{2}{\pi\sqrt{LC}} = \frac{2}{\pi\tau}$$

$$\text{Maximum gain per tap} \propto C/2$$

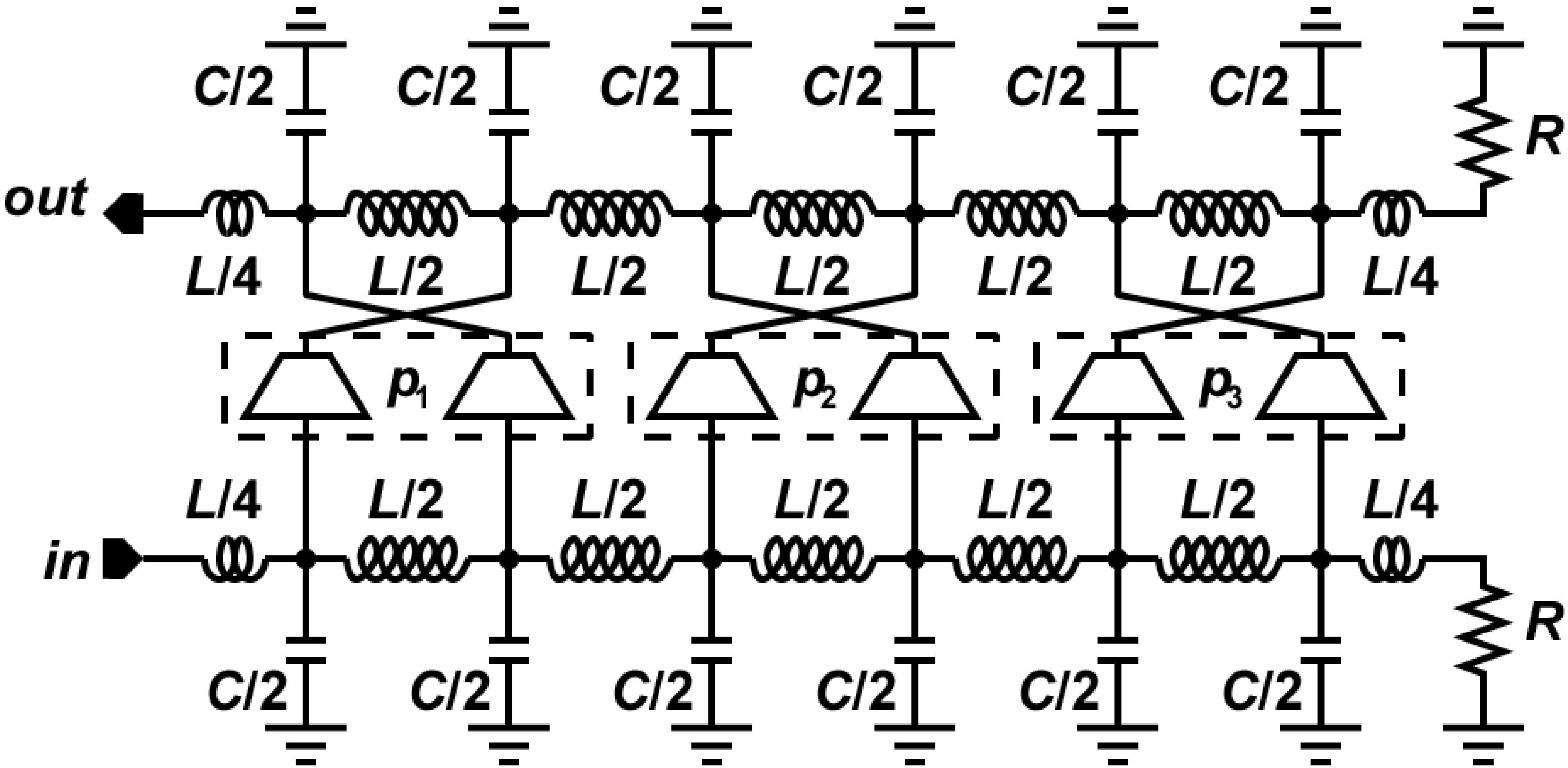
6-Tap Traveling Wave Filter

- Example: Simulated 6-section lumped-LC delay line designed for the same total delay

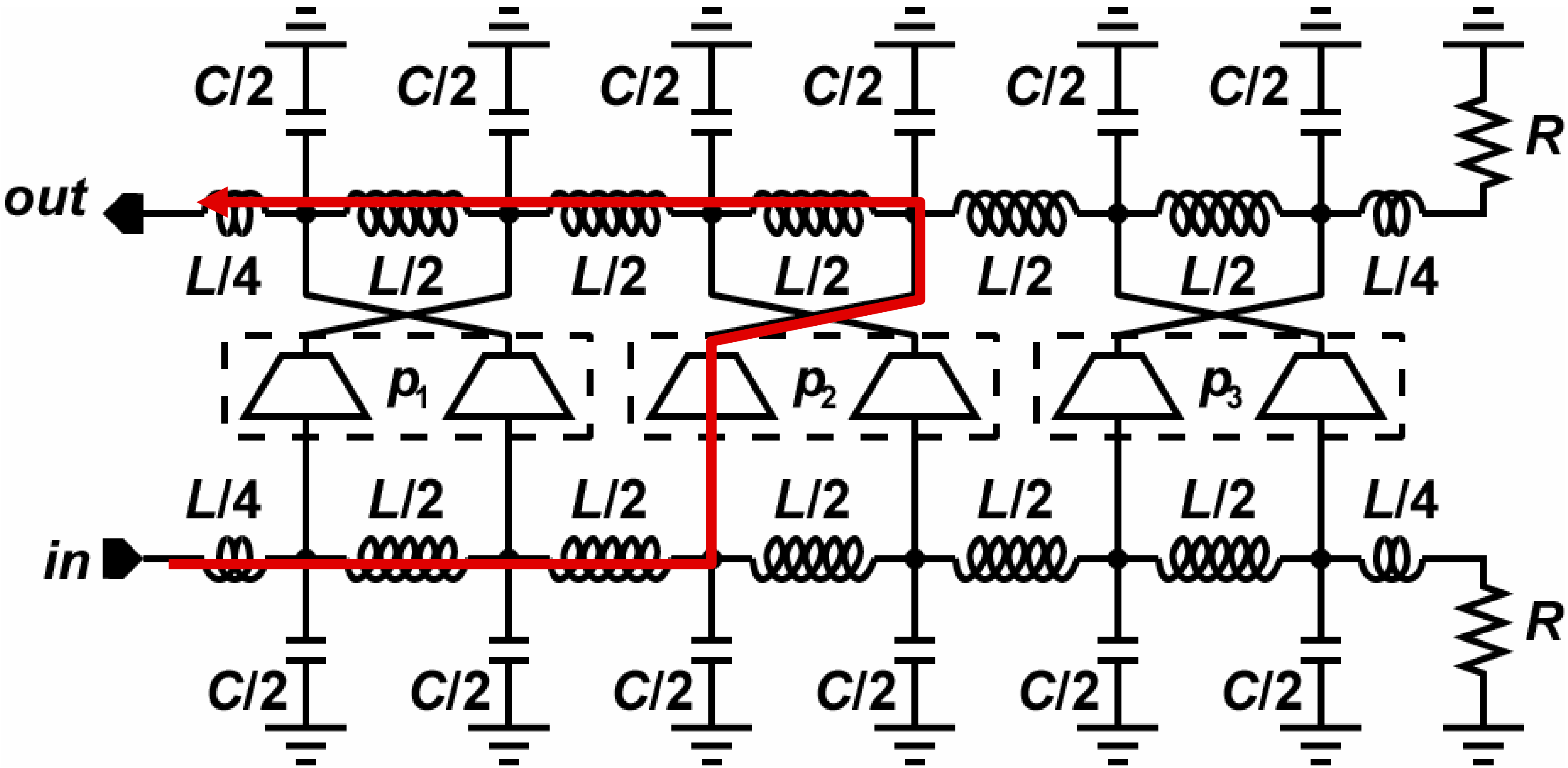




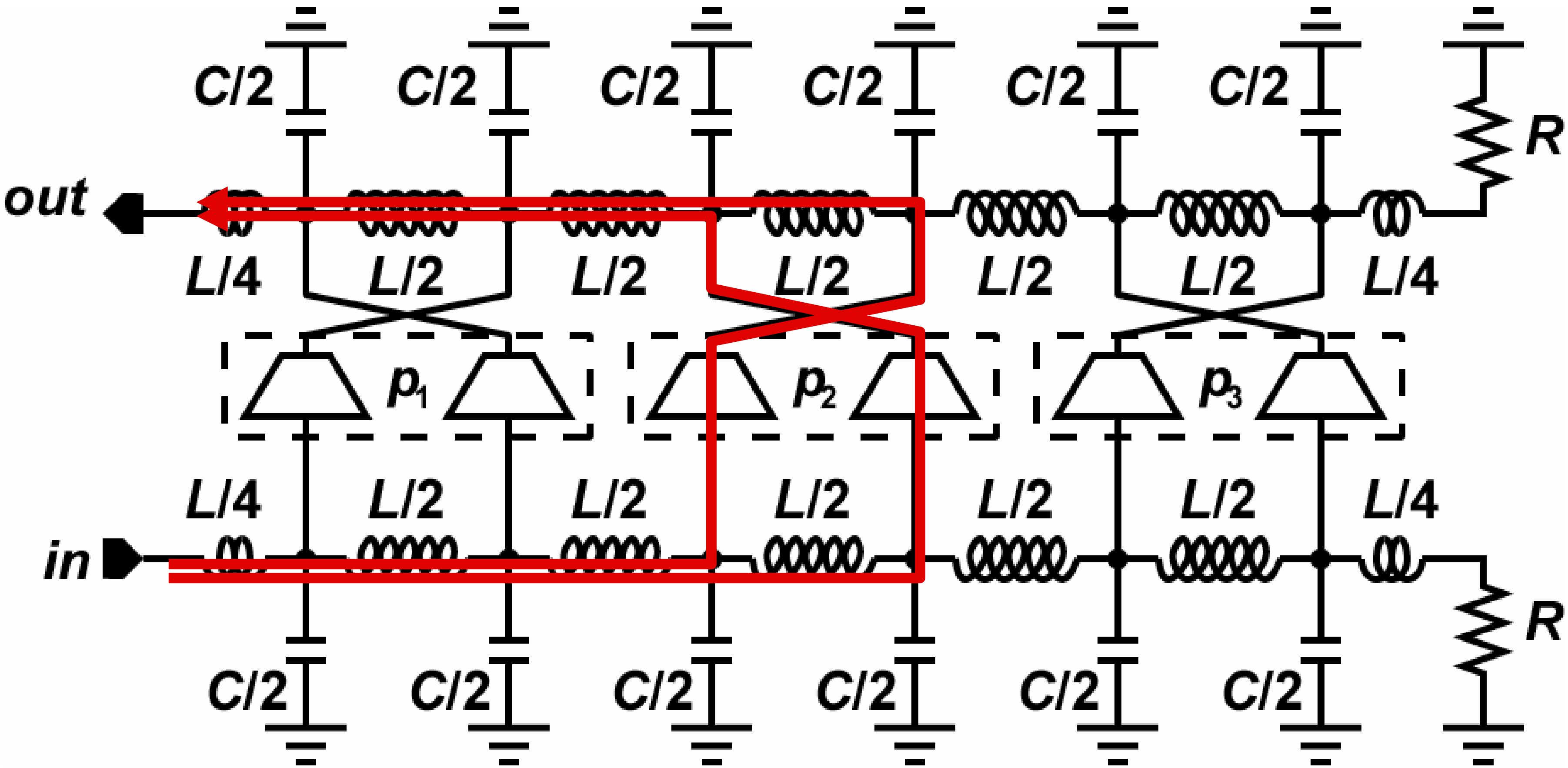
3-Tap Crossover TWF



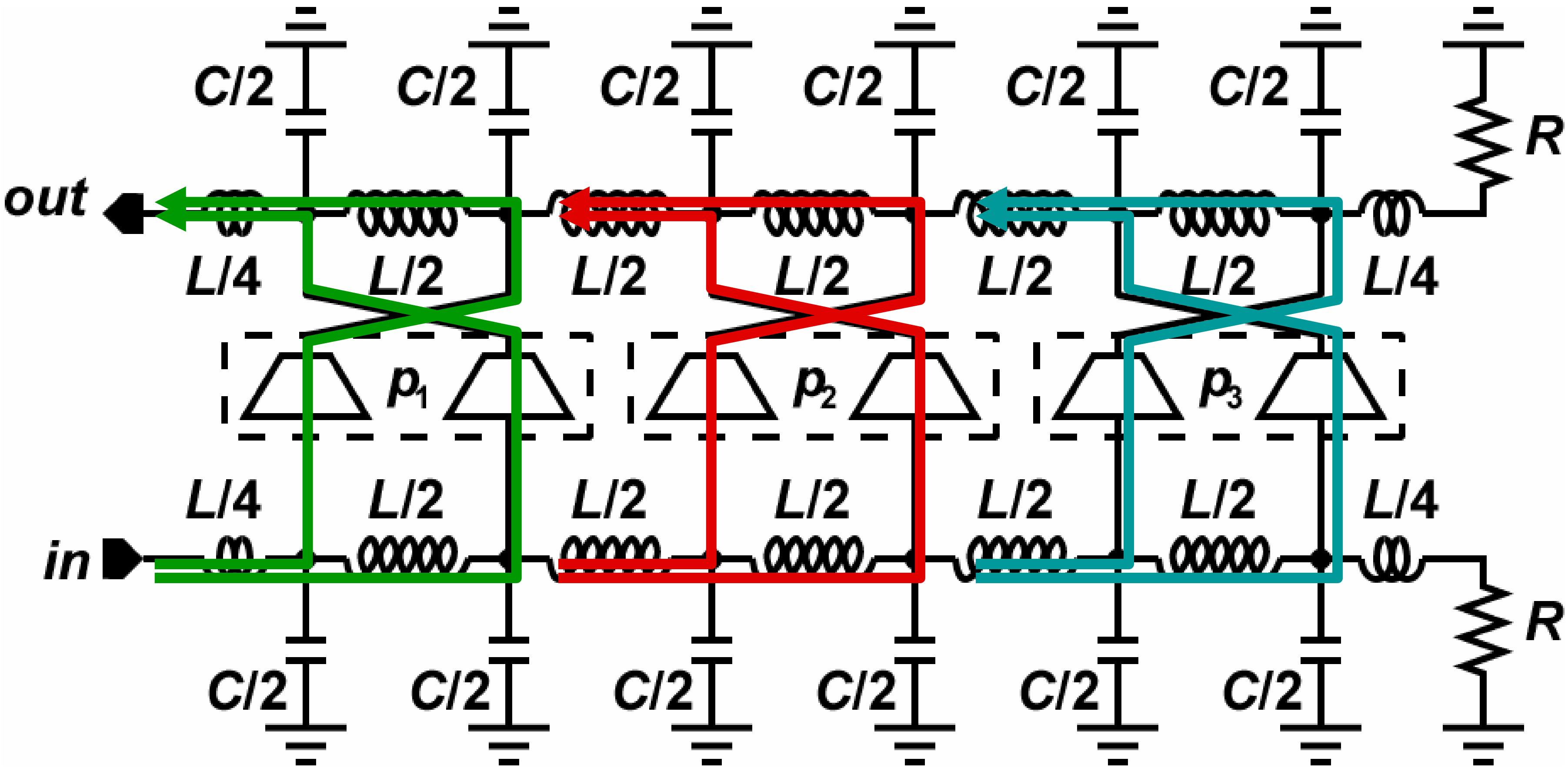
3-Tap Crossover TWF



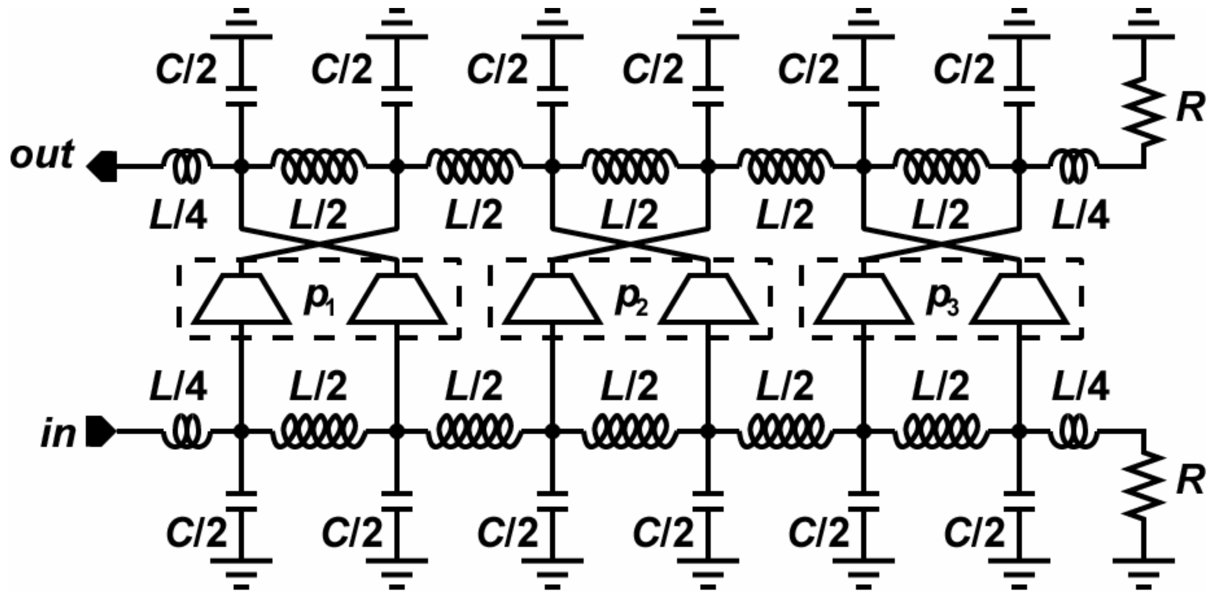
3-Tap Crossover TWF



3-Tap Crossover TWF



3-Tap Crossover TWF



$$\text{Tap spacing}: \quad \tau = 2\sqrt{LC}$$

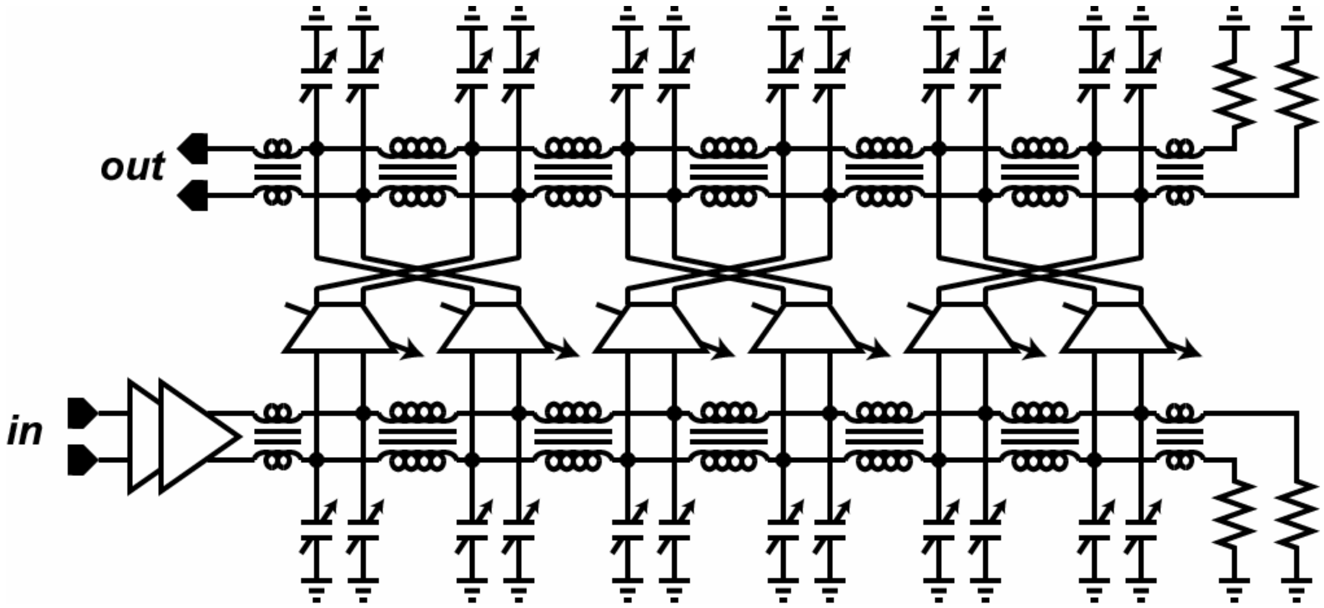
$$\text{Delay Line Bandwidth}: \quad f_{3\text{dB}} = \frac{2}{\pi\sqrt{LC}} = \frac{4}{\pi\tau}$$

$$\text{Maximum gain per tap} \propto C$$

Summary

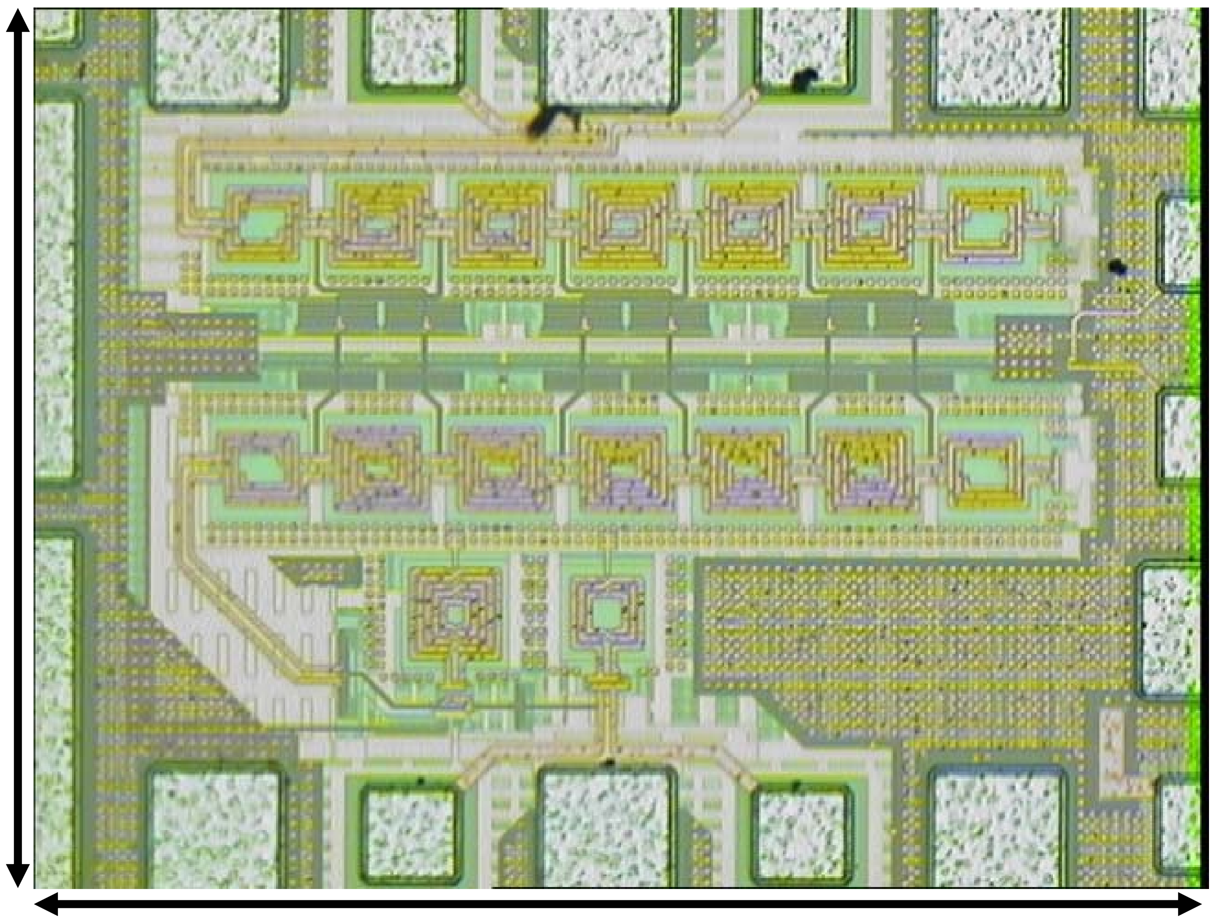
	Tap spacing	***Delay line bandwidth***	***Max. gain per tap***
3-tap TWF	$2\sqrt{LC}$	$\frac{1}{\pi\sqrt{LC}}$	$\propto C$
6-tap TWF	$\sqrt{LC}$	$\frac{2}{\pi\sqrt{LC}}$	$\propto C/2$
3-tap CTWF	$2\sqrt{LC}$	$\frac{2}{\pi\sqrt{LC}}$	$\propto C$

Prototype Implementation



- 90-nm CMOS process
- 24 mW from 1-V supply

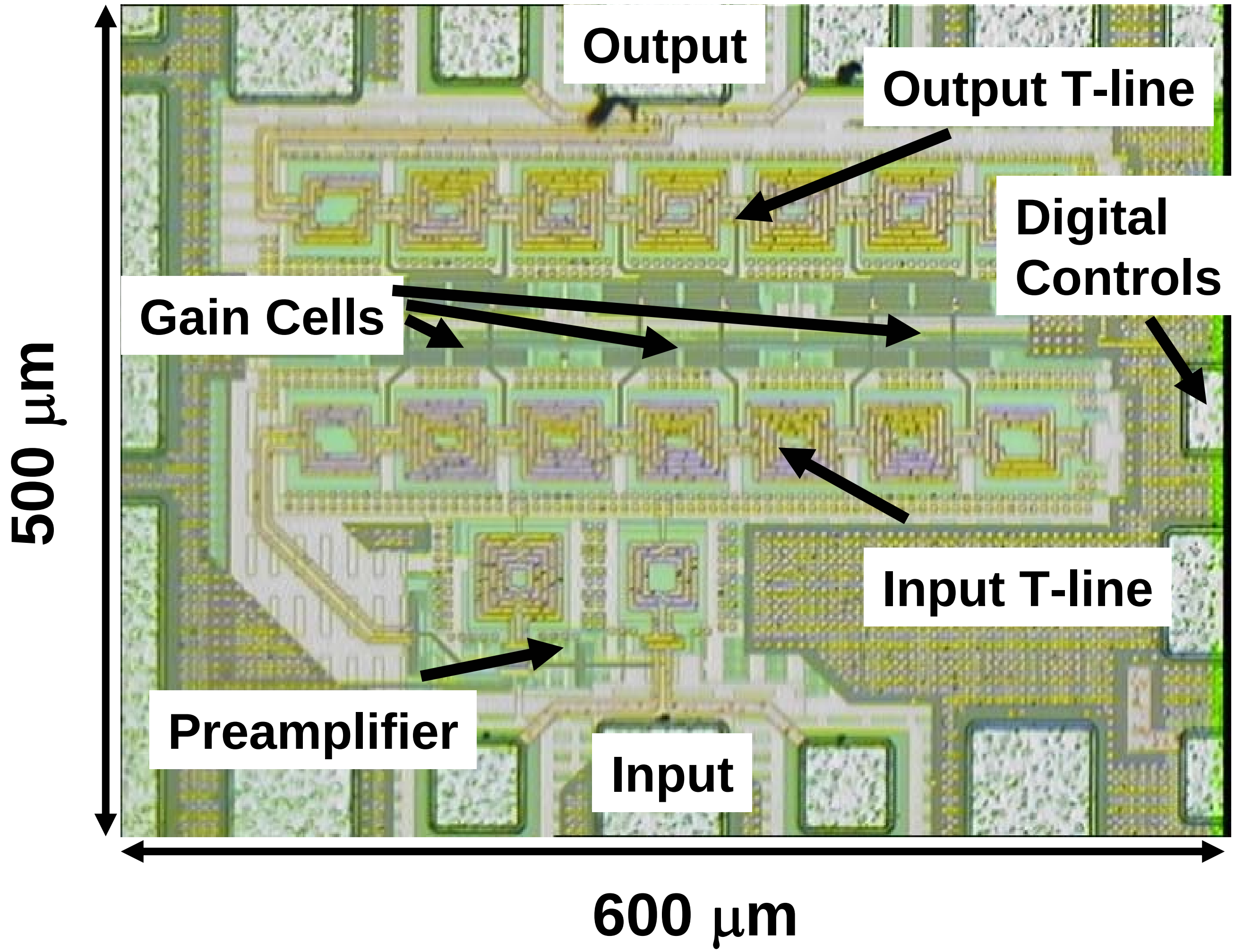
Die Photo



500 μm

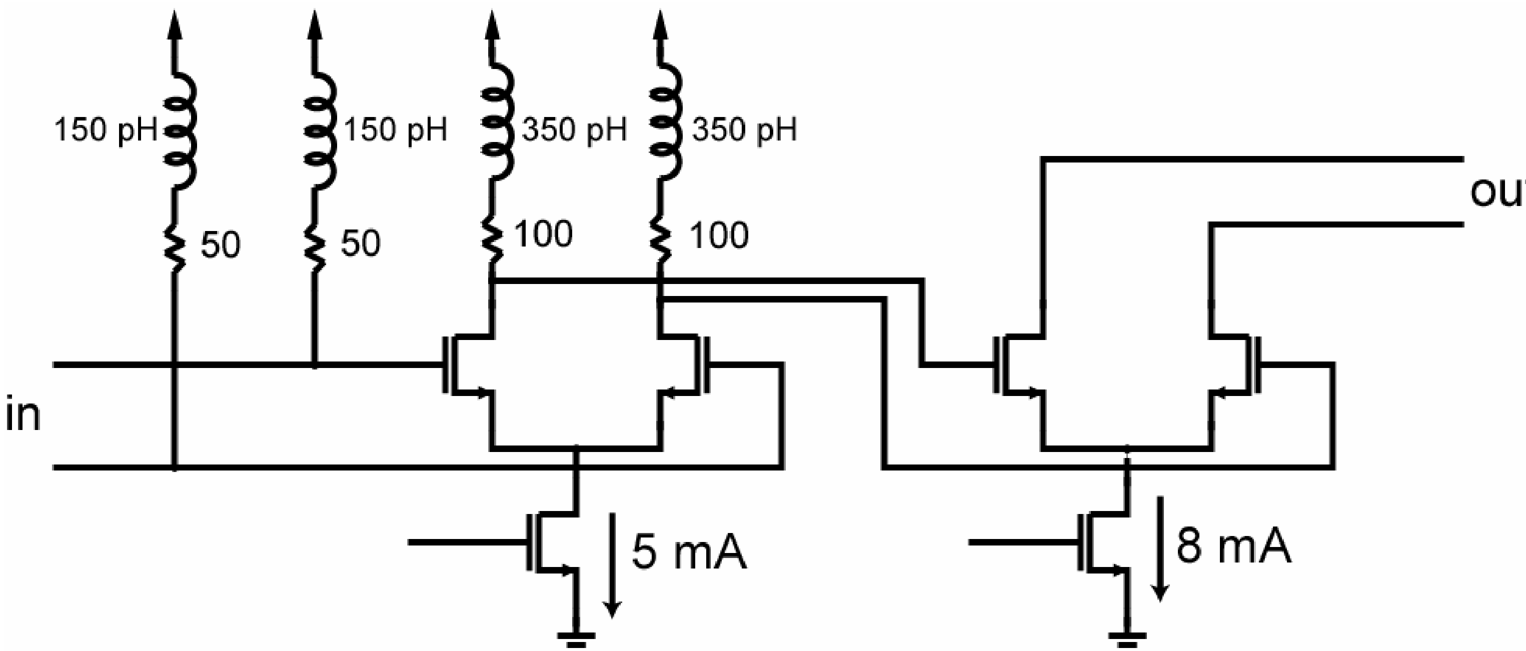
600 μm

Die Photo



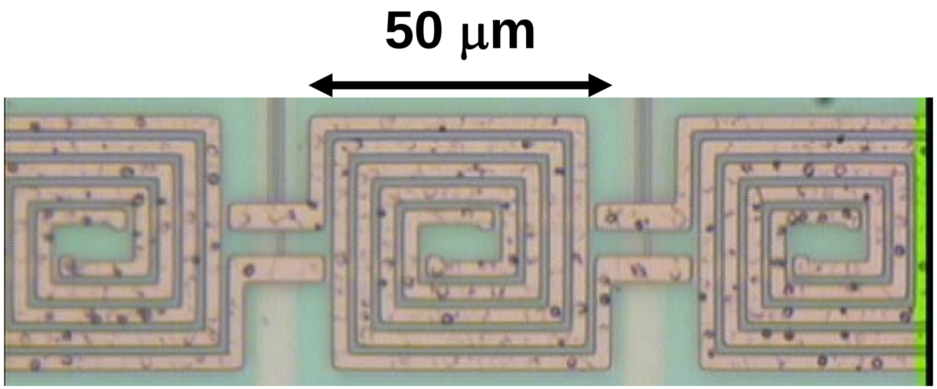
Output
Output T-line
Digital Controls
Gain Cells
Input T-line
Preamplifier
Input
500 μm
600 μm

Pre-amplifier



- Resistive termination for input matching
- Open-drain 2nd stage
- Common mode rejection facilitates single-ended testing

Passive delay line



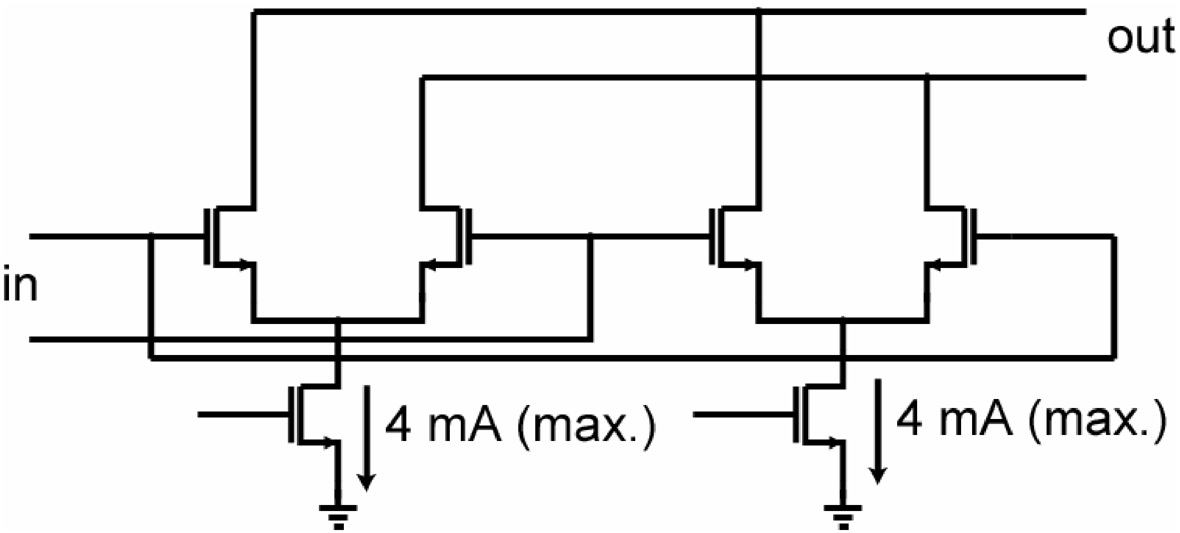
- Differential spiral inductor, $L/2 \approx 300$ pH (per side)
- Capacitance, $C/2 \approx 125$ fF (per side)
  - Tap amplifier input/output capacitance & parasitics (approx. 2/3rds of total capacitance)
  - Digitally-controlled (5-bits) switched MiM capacitors (approx. 1/3rd of total capacitance)

➢ Nominal tap spacing of 25 ps

➢ Differential characteristic impedance, $Z_0 \approx 100$ Ohms

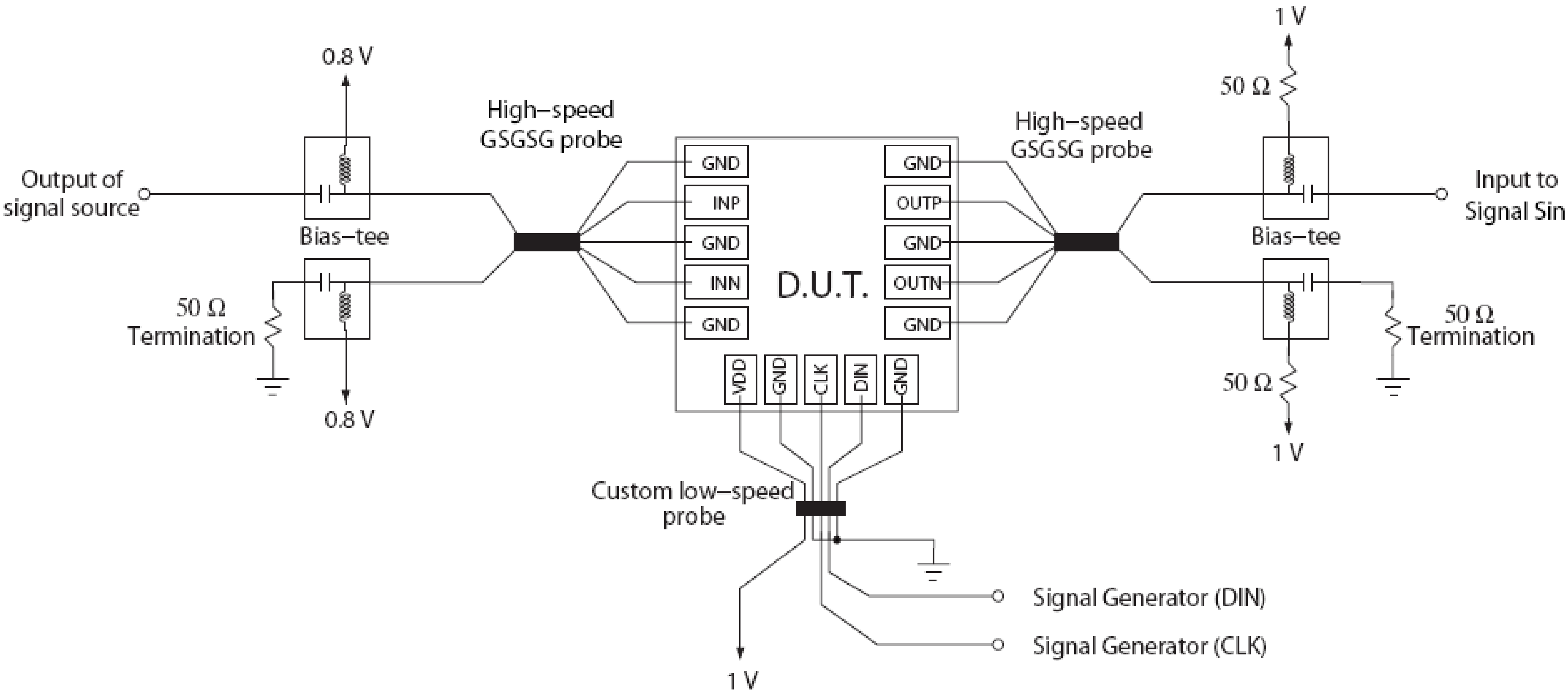
➢ Terminated by two 50-Ohm resistors to V_{DD}

Tap amplifiers



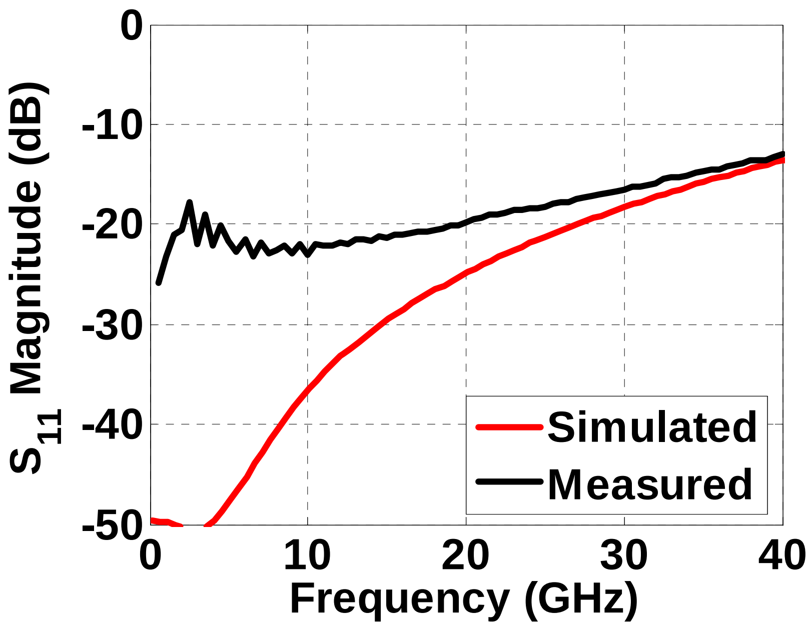
- Each tap amplifier is comprised of two amplifiers with opposing polarity to provide sign control for each tap gain
- The tail currents are digitally controlled (6 bits)

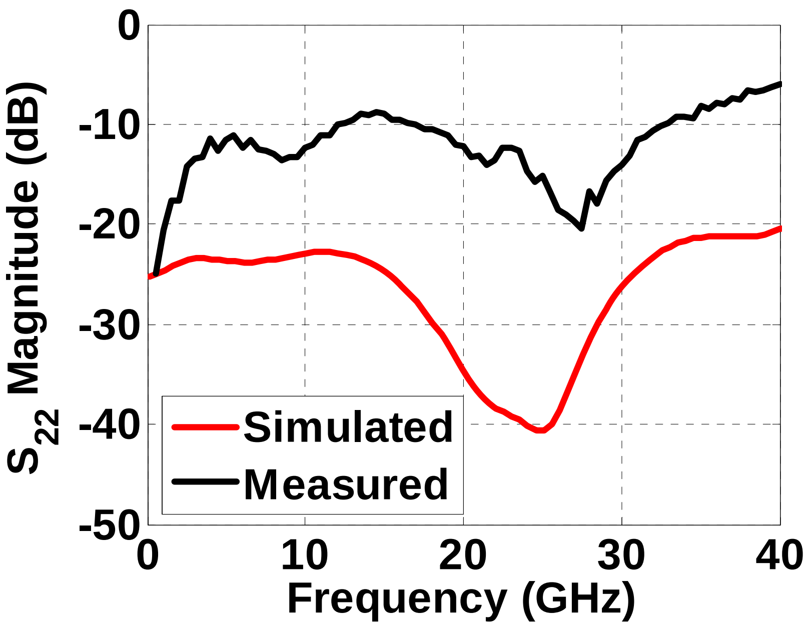
On-wafer test setup



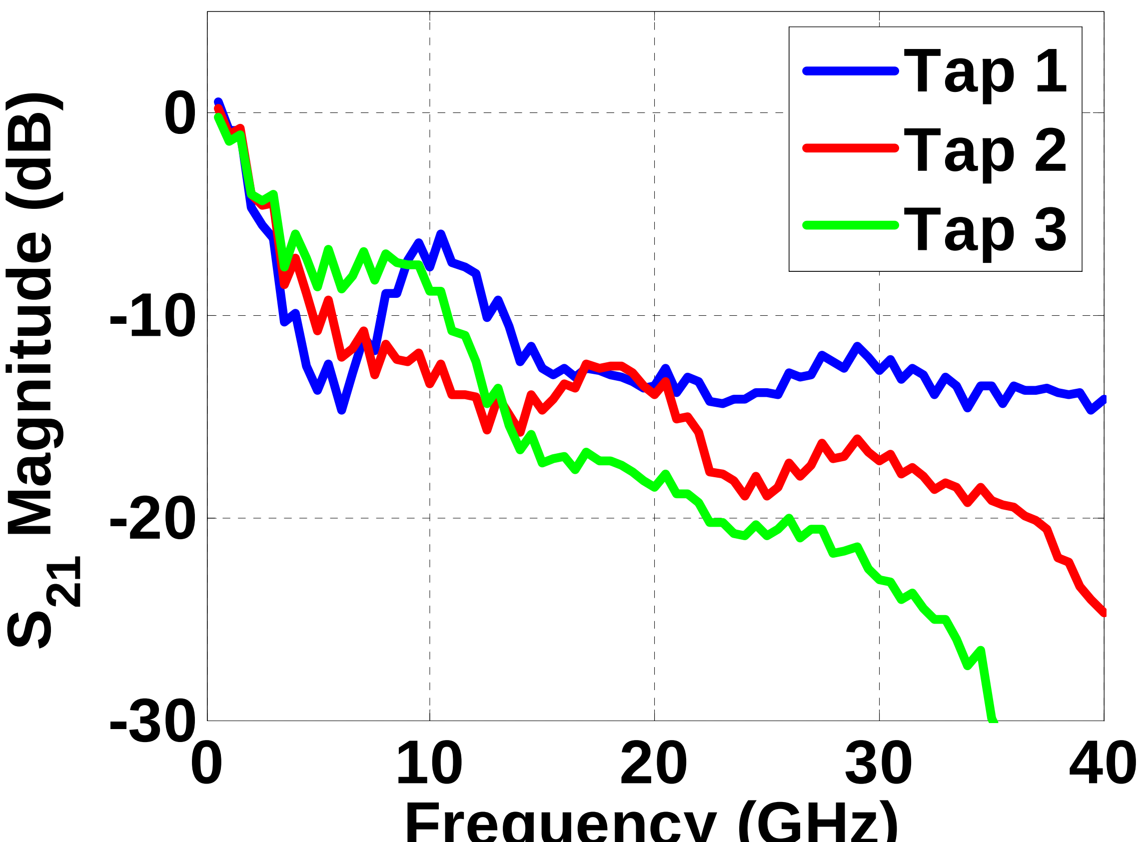
Note: 6 dB loss introduced due to single-ended testing

Input and Output Matching



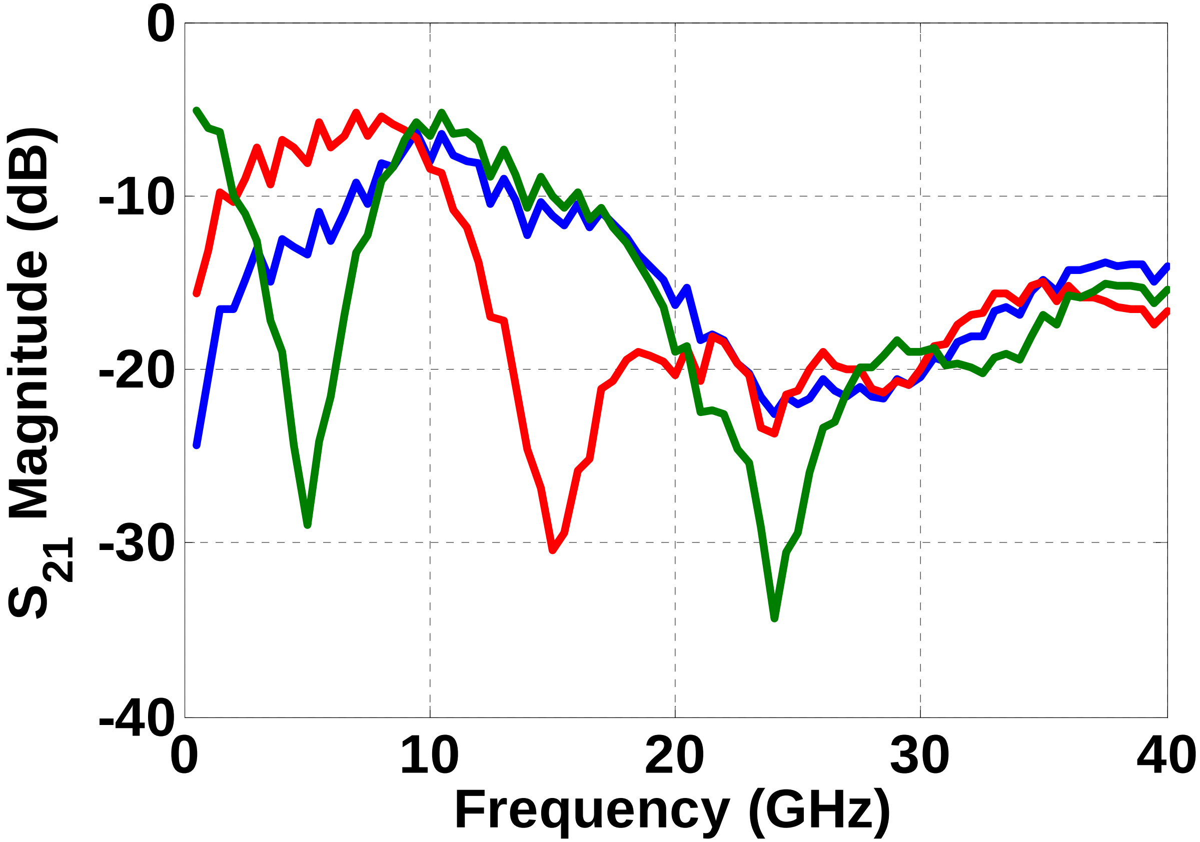


Tap Frequency Response



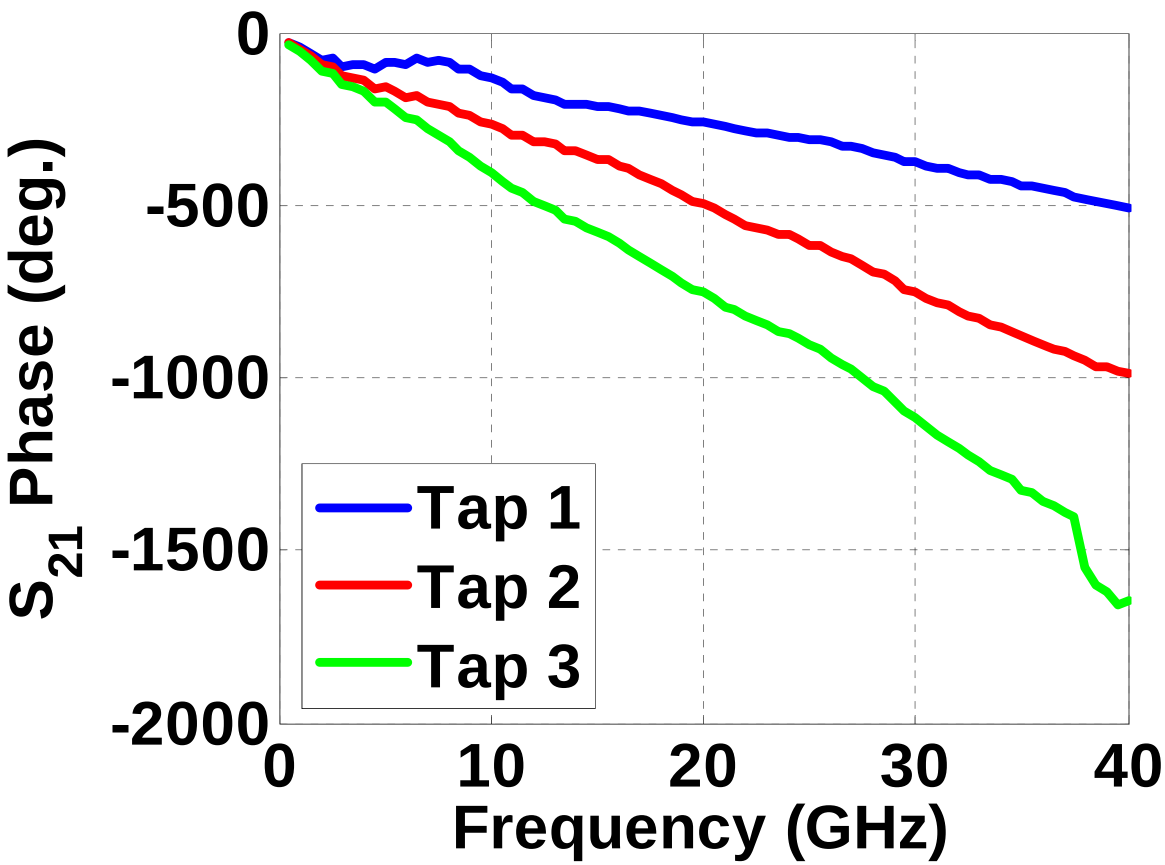
- Single ended measurements made with a 2-port network analyzer
  - Differential measurements would be +6 dB greater

Frequency Response



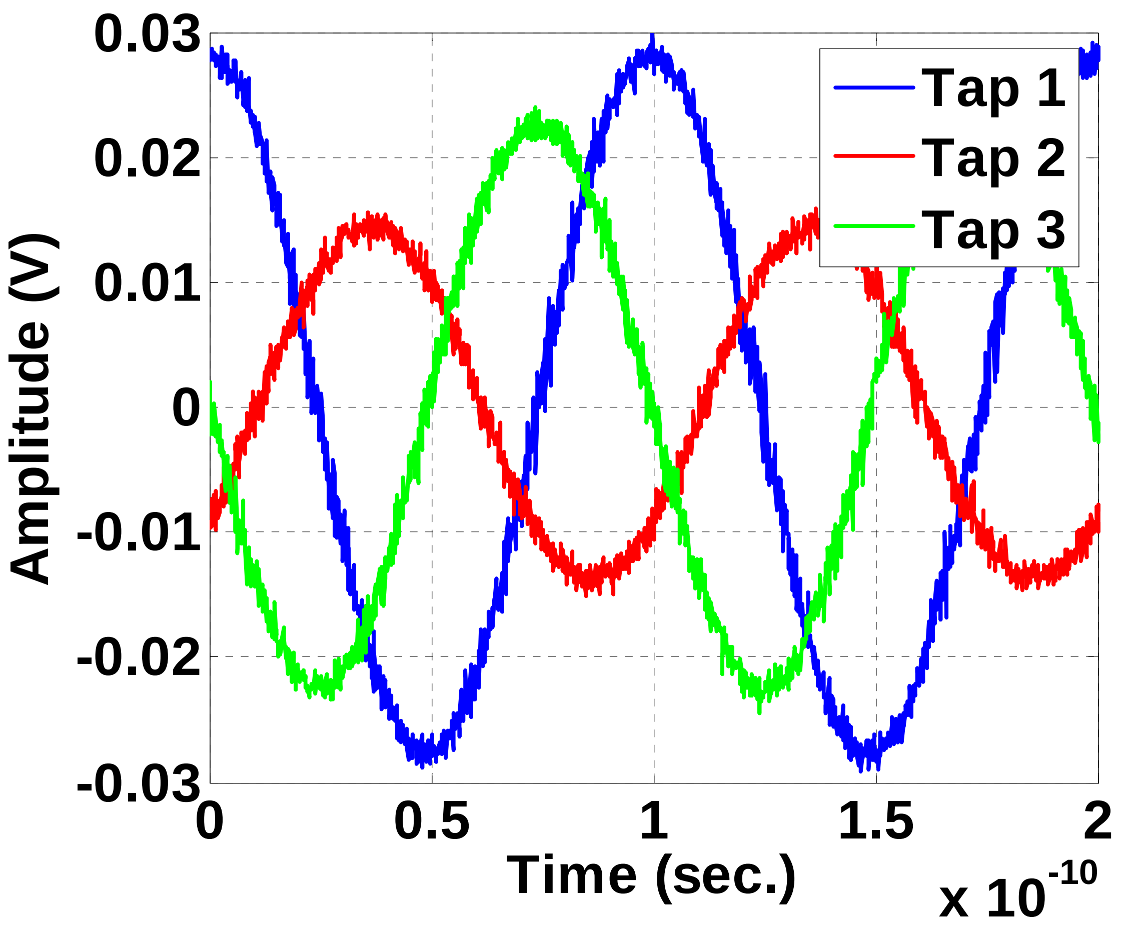
- Taps can be combined to provide a variety of frequency responses

Tap Frequency Response



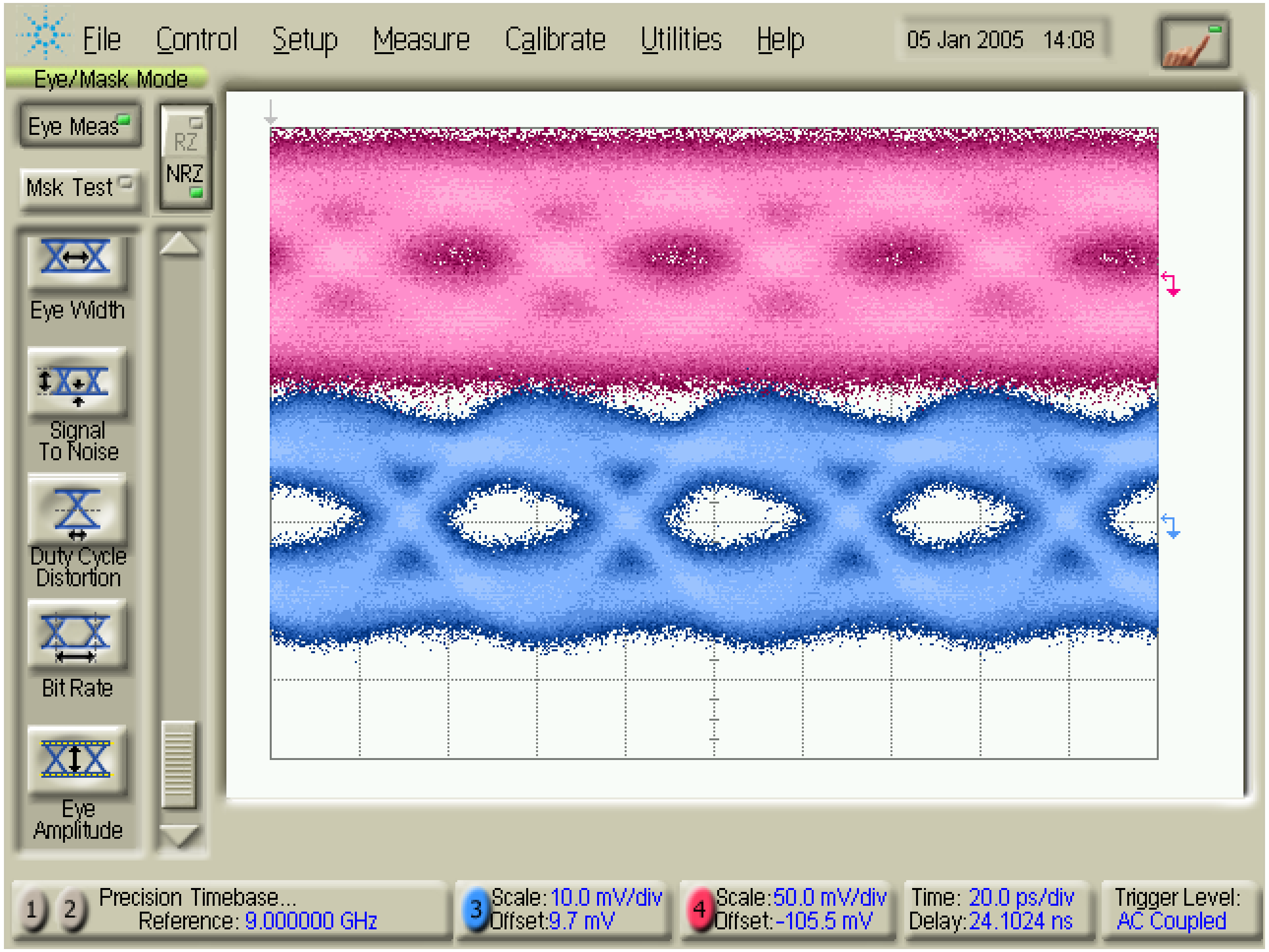
- The slope of the phase response corresponds to a tap spacing of approx. 35 ps

Individual tap responses at 10 GHz

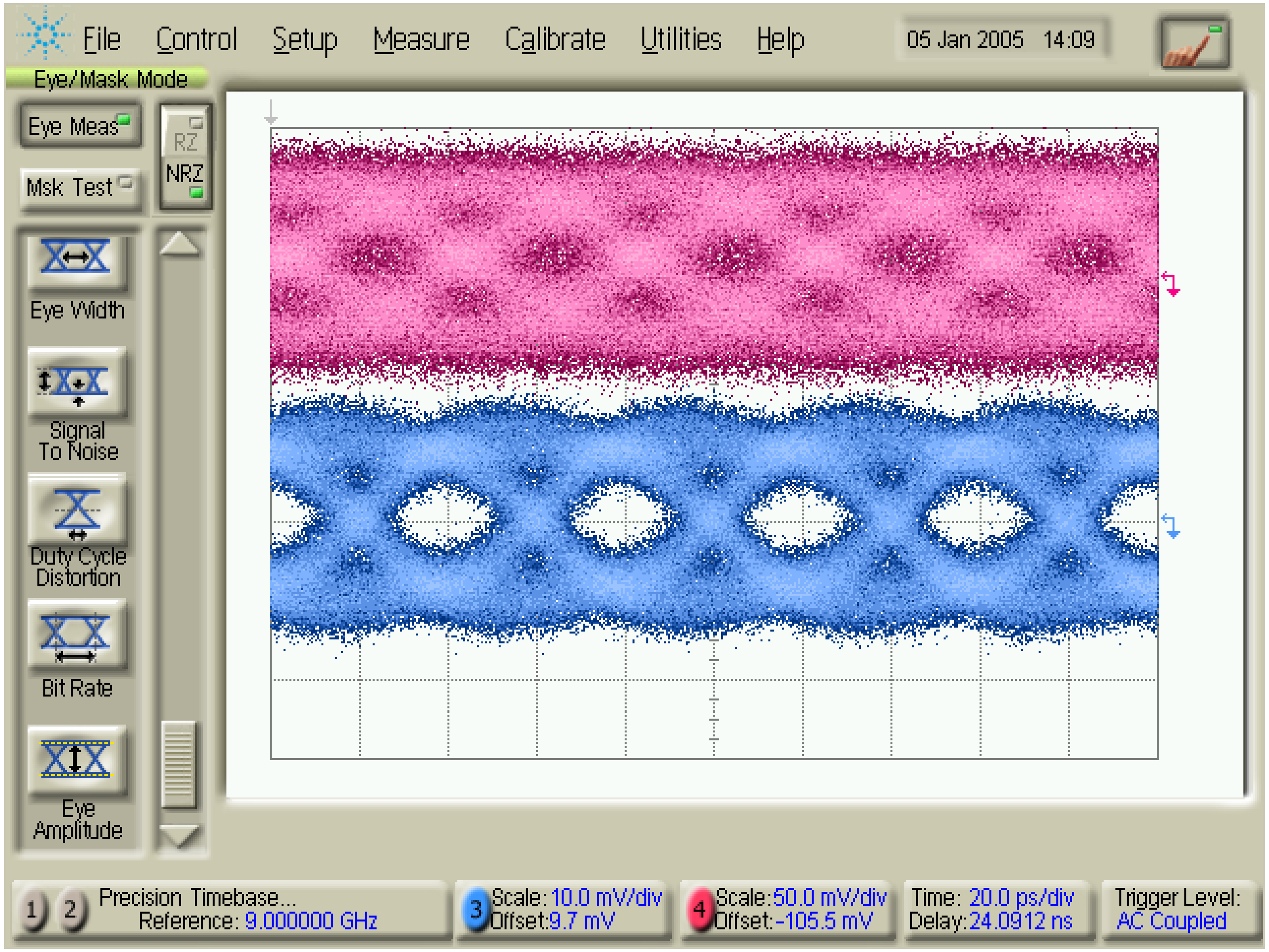


- Confirms a tap spacing of approx. 35 ps

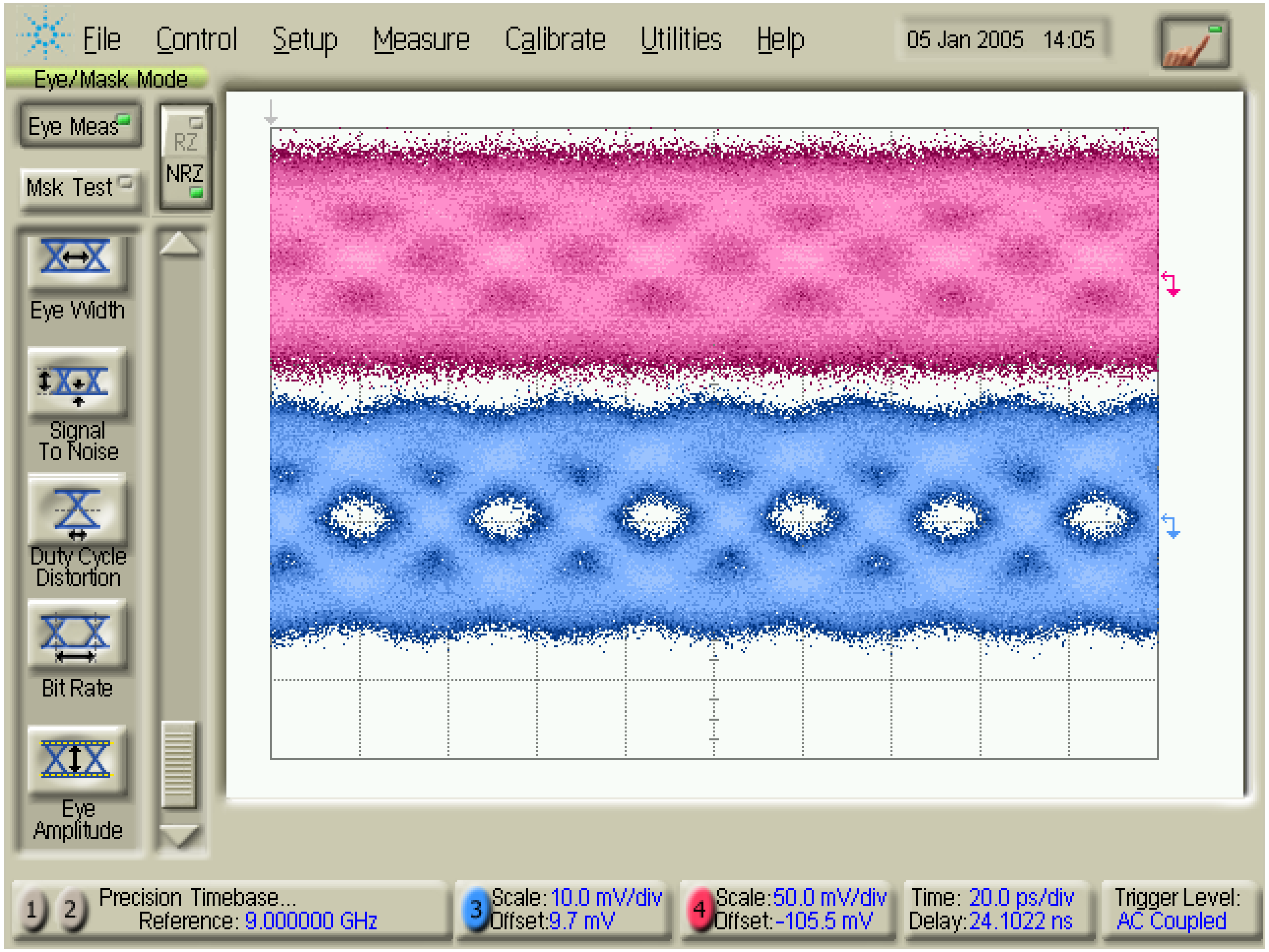
Input and output eye diagrams at 20 Gb/s over 4 m of SMA coax



Input and output eye diagrams at 25 Gb/s over 4 m of SMA coax



Input and output eye diagrams at 30 Gb/s over 4 m of SMA coax



Conclusions

- A crossover traveling wave filter topology was introduced to alleviate the delay·bandwidth tradeoffs in traditional traveling wave filters
- Differential lumped-LC delay lines are used to reduce the area and series losses
- The topology was demonstrated in a 3-tap 90-nm CMOS filter capable of equalization up to 30 Gb/s (the fastest known CMOS FIR filter to date)

Acknowledgements

- Test support:
  - Timothy Dickson
  - Quake Technologies
- CAD tools:
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  - Gennum Corp.