A 1-1-1-1 MASH Delta-Sigma Modulator Using Dynamic Comparator-Based OTAs

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***Abstract*—A 1-1-1-1 MASH delta-sigma modulator with dynamic comparator-based OTAs as replacements for conventional OTAs is presented. The proposed OTA asynchronously alternates between input comparison and current pulse injection under digital control. The 65-nm LP CMOS prototype achieves a FoM of 276 fJ/conv-step with 70.4 dB SNDR over a 2.5-MHz bandwidth while consuming 3.73 mW from a 1.2-V supply.**

I. Introduction

Zero-crossing-based circuits (ZCBCs) [1] and comparator-based switched capacitors (CBSCs) [1] [2] have been proposed as replacements for conventional OTAs in switched-capacitor (SC) based ADCs. They have provided good performance in pipeline ADCs [3], [4], but their performance in delta-sigma modulators [5]–[7] has trailed that of conventional OTAs.

Existing ZCBCs continuously apply current at the output until a zero crossing of the virtual ground voltage (V_g) is detected by the zero-crossing detector (ZCD) to perform charge transfer between capacitors as shown in the SC integrator in Figure 1(a). Due to the delay in the ZCD (T_d), the V_g ramp does not stop at zero but overshoots leaving a residual virtual ground voltage ΔV_g and thus residual charge in C_s [5], [6]. This overshoot deteriorates the accuracy of the SC operation [5] since it has both linear and nonlinear signal-dependent components due to the nonidealities of the current sources in addition to the DC component.

Furthermore, existing ZCBCs continuously monitor V_g using a partially differential high-gain open-loop amplifier as the ZCD. An exception is [4] which uses a single-ended latch in the last stage of the ZCD. In either case, the partially differential amplification introduces a systematic offset, and high-gain open-loop amplification tends to be slow because of the large output impedance for a high enough gain to resolve a small input to the rail-to-rail logic level.

The dynamic comparator-based OTA proposed in this paper performs a similar operation to existing ZCBCs but by iteration of dynamic comparison of V_g and current pulse injection under digital amplitude control as shown in Figure 1(b). This approach provides several advantages over the existing ZCBCs, which rely on continuous monitoring of V_g and continuous current injection, as follows. Because V_g is constant during each comparison, ΔV_g is decoupled from the comparator delay.

[1]In this paper, we consider CBSCs as ZCBCs since a CBSC is essentially same as a ZCBC except that a comparator is used in a CBSC instead of a zero-crossing detector in a ZCBC. A zero-crossing detector is a circuit block tailored for detecting a zero crossing of its input, which a comparator can also do.

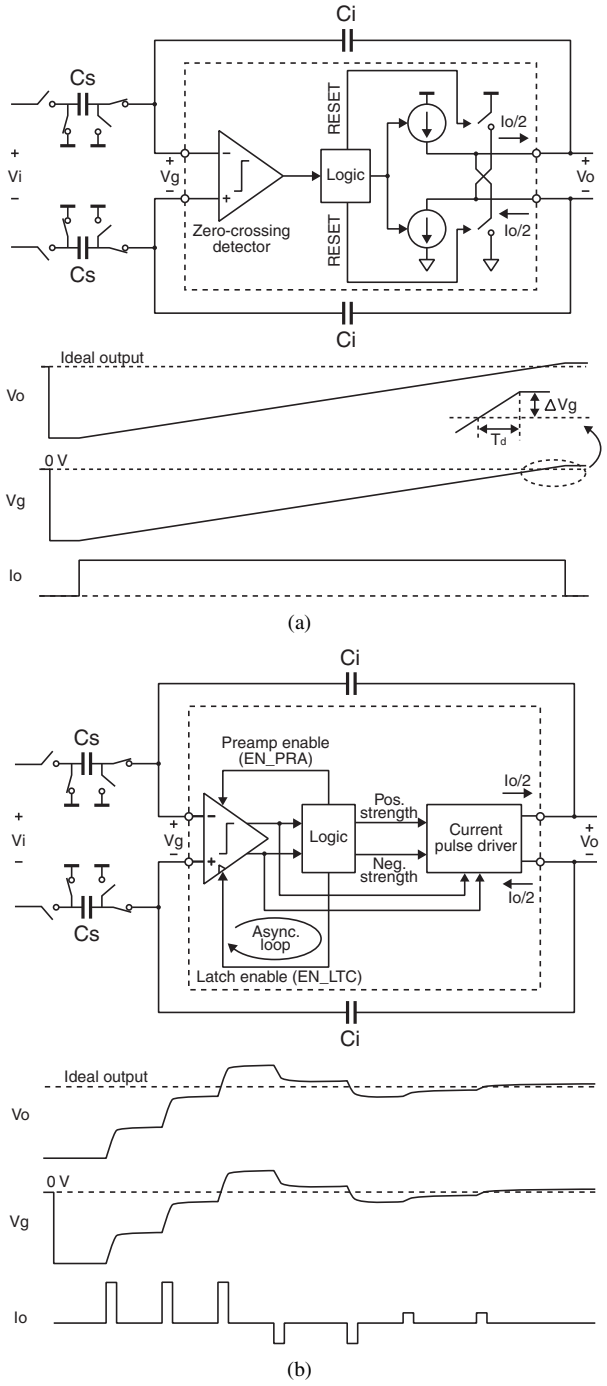


Fig. 1. SC integrators based on ZCBC (a) and proposed OTA (b).

It instead is a uniformly distributed over the final V_g step size. This allows for better control of the integration accuracy. In this work, up to six V_g step sizes are used providing fast integration and a small final V_g step. The constant V_g during comparison also allows it to be monitored using a truly fully-differential regenerative comparator, which has proven its ability to efficiently resolve a small inputs at high speed [8]. It has zero systematic offset, and unlike open-loop amplifiers, it is CMOS scaling friendly since it relies on nonlinear regeneration for resolving its input.

In this paper, we present a 1-1-1-1 MASH delta-sigma modulator implemented with dynamic comparator-based OTAs. The delta-sigma modulator provides a higher SNDR, higher bandwidth, and better figure of merit (FoM) than any previously reported delta-sigma modulators based on ZCBC.

II. Dynamic Comparator-Based OTA

The dynamic comparator-based OTA consists of a fully-differential dynamic comparator, control logic, and current pulse driver as shown in Figure 1(b). The comparator evaluates the sign of V_g. The comparator output triggers the current pulse driver to inject either a positive or negative differential current pulse at the output in order to move V_g toward zero. At the same time, the control logic turns off and resets the comparator to save power and prepare for the next comparison. Shortly after the current pulse injection is complete, the comparator is enabled again, and the operation above repeats.

This iterative process of V_g comparison and current pulse injection is timed asynchronously as shown in Figure 2 so no high-speed clocks need to be explicitly generated or routed over a long distance. This asynchronous operation is similar to that of an asynchronous SAR ADC [9].

The control logic also governs the amplitude of current pulses. At the beginning of an integration phase, the amplitude is set to the maximum, and each time a V_g sign change is detected, the amplitude is reduced so V_g converges to zero by repeating V_g comparison and current pulse injection. The iteration ceases with the DONE signal asserted once a V_g sign change is detected at the minimum current pulse amplitude setting as shown in Figure 2. This current pulse amplitude logic is the timing critical path of the control logic, so it can limit the speed of the OTA. If both positive and negative current pulse amplitudes are updated at the same time at each V_g sign change, the amplitude update would have to complete within a very short time window (T_a in Figure 2) between comparison and the immediately following current pulse injection. However, since a current pulse amplitude update is always accompanied by a change in the polarity of the current pulse, the amplitude of the next opposite polarity can be pre-decremented so the amplitude update time window is significantly extended (T_b).

A schematic of the comparator is shown in Figure 3. The dynamic latch follows the 3-stage fully-differential preamplifier with a 30-dB overall gain and 3-GHz bandwidth. For each comparison, the preamplifier is enabled about 200 ps ahead of the latch so the preamplifier output settles before the latch is enabled. During the reset and power-down phase, the tail

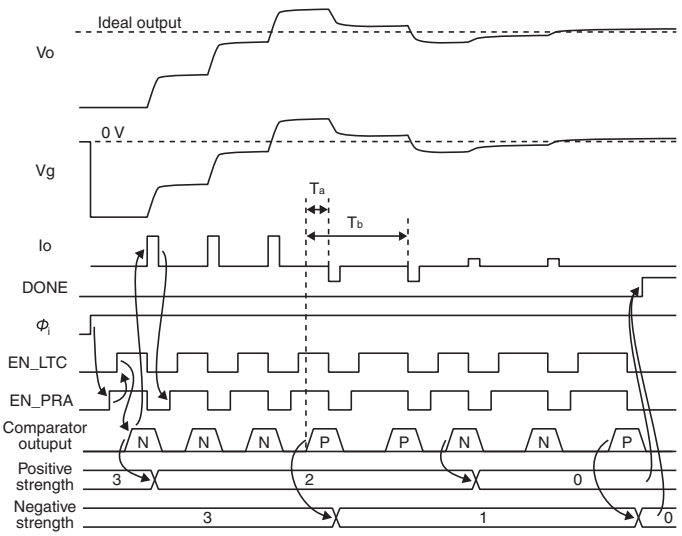


Fig. 2. Timing diagram of the proposed OTA.

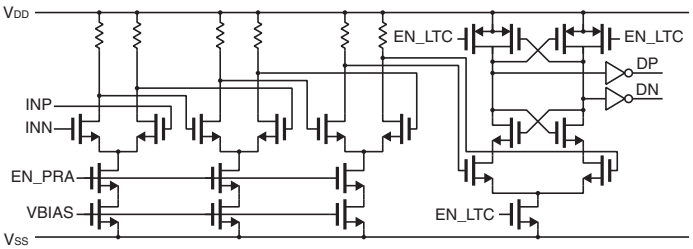


Fig. 3. Comparator schematic.

current sources of the preamplifier are disconnected so the output nodes of the preamplifier are reset to VDD by the load resistors and the latch output nodes are also reset to VDD by reset switches. The comparator was sized to meet the thermal noise requirements found from system-level simulations.

Figure 4 shows a simplified schematic of the current pulse driver. After each comparison of the comparator, either DP or DN goes up triggering a simple combinational circuit that generates a pulse five inverter delays in duration. This pulse is delivered to a current driver that is divided in to six quaternary ratioed slices, which the control logic selectively enables determining the current pulse amplitude. PMOS transistors source a current pulse into one side of the differential output while NMOS transistors sink a current from the other side. The output common-mode voltage of the discrete-time OTA is loosely set to midrail without CMFB by sizing PMOS and NMOS transistors for an equal resistance.

III. 1-1-1-1 MASH Delta-Sigma Modulator

The proposed dynamic comparator-based OTAs with six quaternary scaled current pulse amplitude settings were applied to the 1-1-1-1 MASH delta-sigma modulator shown in Figure 5(a). Interleaved sampling capacitors [10] were used so all of the integrators integrate and sample during the same phase (Φ_2) and the quantizers are the only blocks that operate in the other phase (Φ_1). The integration phase was made twice as long as

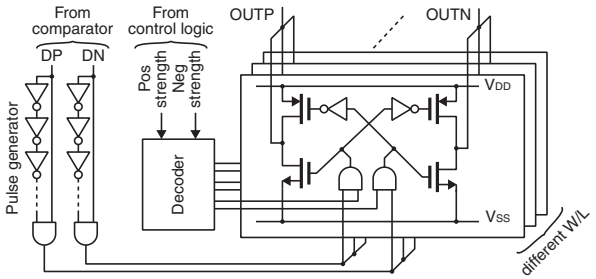


Fig. 4. Current pulse driver schematic

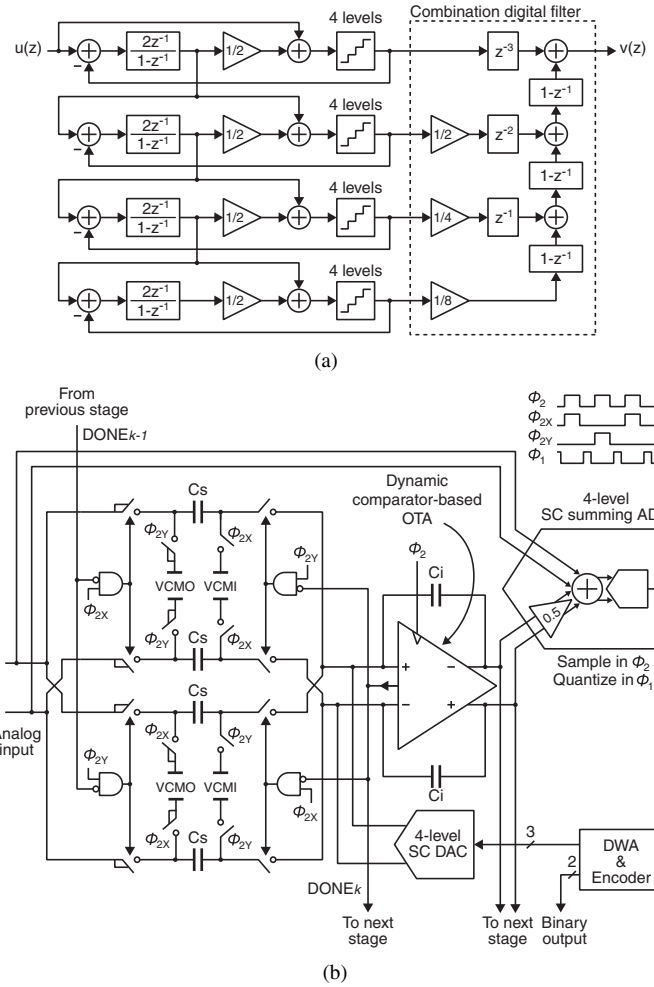
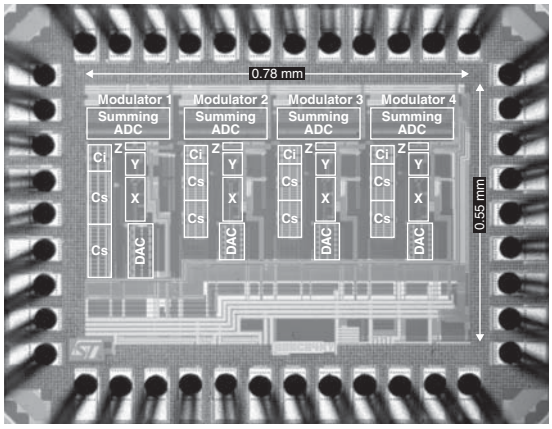


Fig. 5. Modulator block diagram (a) and schematic of one stage (b).

the other phase extending the integration phase by 33%, and thus increasing the maximum sampling frequency by the same factor. Figure 5(b) shows a simplified single-ended schematic of one stage of the modulator. Capacitors Cs and Ci are 1 pF and 0.5 pF, respectively, in the first stage and they are 0.5 pF and 0.25 pF for the rest of the stages. The DONE signal isolates the capacitors after integration to prevent unwanted charge transfer after the integrator output has settled but before the end of clock phase Φ_2. The quantizer passively sums its two inputs with weighted SCs and then quantizes the sum.



X: Comparator, Y:Control logic, Z: Current pulse driver

Fig. 6. Die microphotograph.

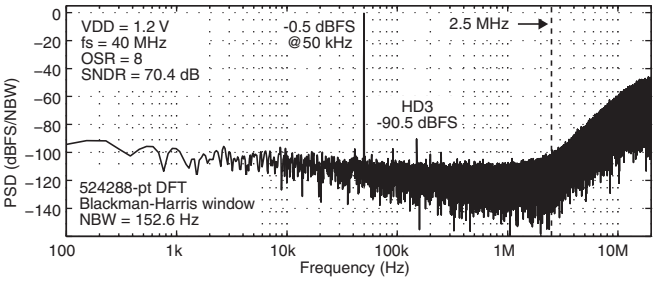
TABLE I
SUMMARY OF THE EXPERIMENTAL RESULTS.

	This work		[5]	[6]	[7]
Conventional OTA	No		No	No	No
CMOS technology	65 nm		45 nm	0.18 μm	3 μm TFT
Supply (V)	1.2	1.0	1.1	1.8	11.2
Sampling rate (MHz)	40	30	50	2.56	0.4
OSR	8		30	64	128
Bandwidth (MHz)	2.5	1.875	0.833	0.02	0.00156
Peak SNDR (dB)	70.4	67.5	47.7	65.3	65.6
Dynamic range (dB)	71.3	67.7	54.3	71	69
Power (mW)	3.73	1.88	0.63	0.42	63.3
FoM (fJ/conv-step)	276	259	1907	6980	13.0×10^6

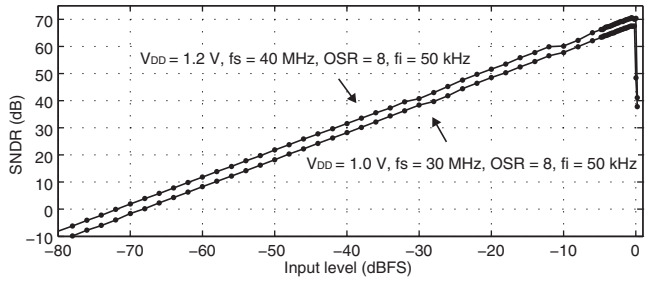
IV. Experimental Results

The prototype delta-sigma modulator was implemented in a silicon area of 0.43 mm^2 in a 65-nm LP CMOS technology with standard-Vt devices only. A die photo of the prototype is shown in Figure 6. The measured peak SNDR is 70.4 dB and power dissipation is 3.73 mW at VDD=1.2 V, f_s=40 MHz, and OSR=8 without any calibration. Figure 7 shows the measured output spectrum at the peak SNDR and SNDR versus the input level. Figure 8 shows the measured output spectrum with a two-tone input near the edge of the signal bandwidth (2.5 MHz). The peak SNDR and IMD in this case are 67.3 dB and -89.5 dBc, respectively. This 3-dB penalty in SNDR compared to the single-tone measurement is inherent to the nature of the two-tone test in which the total power of the input is half (-3 dB) of that of the single tone test for the same input swing. Table I summarizes the experimental results and compares the results with other reported implementations of ZCBC-based delta-sigma modulators.

The FoM of 276 fJ/conv-step is not the best when compared with continuous-time delta-sigma modulators with a similar bandwidth and resolution. However, the modulator in this work provides both f_s (or bandwidth) scalability and power scalability over f_s without requiring any circuit reconfiguration because of the discrete-time delta-sigma modulation and dynamic operation of the OTAs. The f_s scalability requires RC time constant tuning in continuous-time delta-sigma modulators,



(a)



(b)

Fig. 7. Measured modulator output spectrum (a) and SNDR versus input level (b).

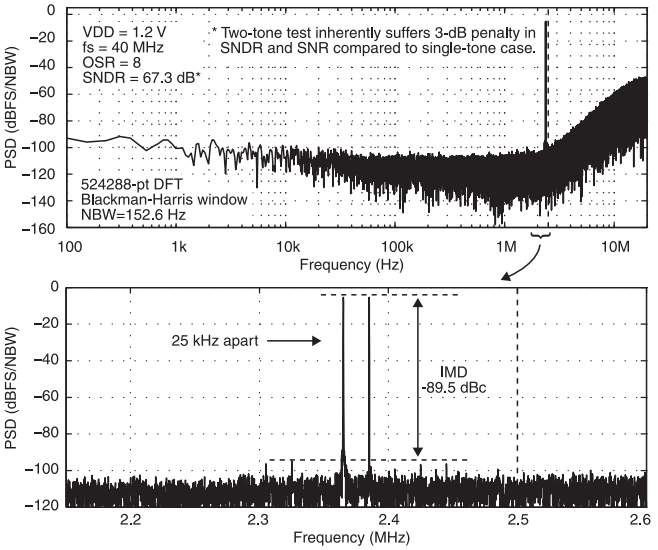
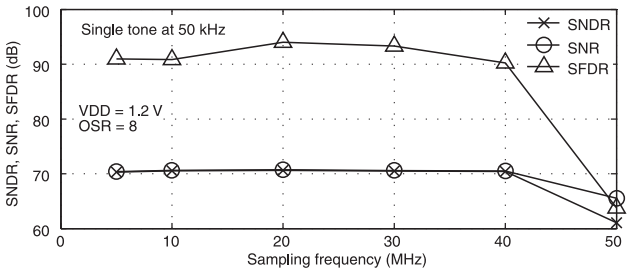


Fig. 8. Measured modulator output spectrum with a two-tone input.

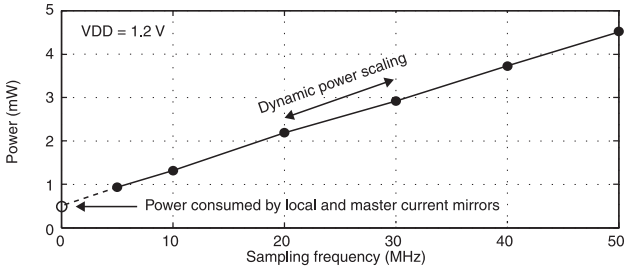
and power scalability over f_s requires bias current adjustment in both conventional discrete-time and continuous-time delta-sigma modulators. Both are difficult to achieve over a decade range of f_s as is shown here. The SNDR, SFDR, SNR, and power consumption measured over f_s are shown in Figure 9. The offset in the power consumption plot is the static power dissipation of the master and local bias generation circuits, which could be reduced with a redesign.

V. Conclusion

A successful implementation of a 1-1-1-1 MASH delta-sigma modulator with dynamic-comparator based OTAs as



(a)



(b)

Fig. 9. Measured SNDR, SNR, and SFDR (a) and power consumption (b) over f_s

replacements for conventional OTAs in a 65-nm LP CMOS technology is presented. It efficiently performs SC integration by iteration of asynchronously timed dynamic regenerative V_g comparison and current pulse injection under digital amplitude control. The prototype achieves a peak SNDR of 70.4 dB over a 2.5-MHz bandwidth dissipating 3.73 mW from a 1.2-V supply.

References

[1] L. Brooks and H.-S. Lee, "A Zero-Crossing-Based 8-bit 200 MS/s Pipelined ADC," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 12, pp. 2677–2687, Dec. 2007.

[2] J. Fiorenza, T. Sepke, P. Holloway, C. Sodini, and H.-S. Lee, "Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2658–2668, Dec. 2006.

[3] L. Brooks and H.-S. Lee, "A 12b, 50 MS/s, Fully Differential Zero-Crossing Based Pipelined ADC," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3329–3343, Dec. 2009.

[4] J. Chu, L. Brooks, and H.-S. Lee, "A zero-crossing based 12b 100MS/s pipelined ADC with decision boundary gap estimation calibration," in *VLSI Circuits, 2010 IEEE Symposium on*, Jun. 2010, pp. 237–238.

[5] T. Musah, S. Kwon, H. Lakdawala, K. Soumyanath, and U.-K. Moon, "A 630 μW zero-crossing-based $\Delta\Sigma$ ADC using switched-resistor current sources in 45nm CMOS," in *IEEE Custom Integrated Circuits Conference*, Sep. 2009, pp. 1–4.

[6] M.-C. Huang and S. luan Liu, "A Fully Differential Comparator-Based Switched-Capacitor $\Delta\Sigma$ Modulator," *IEEE Transactions on Circuits and Systems II*, vol. 56, no. 5, pp. 369–373, May. 2009.

[7] W.-M. Lin, C.-F. Lin, and S.-I. Liu, "A CBSC second-order sigma-delta modulator in 3 μm LTPS-TFT technology," in *Solid-State Circuits Conference, 2009. A-SSCC 2009. IEEE Asian*, Nov. 2009, pp. 133–136.

[8] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas, "Noise Analysis of Regenerative Comparators for Reconfigurable ADC Architectures," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.

[9] S.-W. Chen and R. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-μm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 12, pp. 2669–2680, Dec. 2006.

[10] A. Gharbiya and D. Johns, "On the implementation of input-feedforward delta-sigma modulators," *IEEE Transactions on Circuits and Systems II*, vol. 53, no. 6, pp. 453–457, Jun. 2006.