A Delta-Sigma Modulator With a Widely Programmable Center Frequency and 82-dB Peak SNDR

Kentaro Yamamoto, *Student Member, IEEE*, Anthony Chan Carusone, *Senior Member, IEEE*, and Francis P. Dawson, *Senior Member, IEEE*

***Abstract*—In this paper, analysis and design of a four-bit fourth-order delta-sigma modulator with a widely programmable center frequency are presented. Novel methods for quantizing and implementing the digitally programmable modulator coefficients enable performance comparable to state-of-the-art discrete-time fixed-frequency modulators at any center frequency from DC to $0.31f_s$ in steps of $0.0052f_s$. The 0.18 μm 1.8 V CMOS prototype implemented in a silicon area of 4.5 mm^2 consumes 115 mW at a sampling frequency of 40 MHz. The SNDR and SNR over a 310 kHz bandwidth range from 71 dB to 82 dB and from 76 dB to 86 dB, respectively.**

***Index Terms*—Analog-to-digital converter (ADC), bandpass, delta-sigma, low-pass, multibit, programmable, tunable, sigma-delta.**

I. Introduction

ONGOING CMOS technology scaling has motivated the replacement of analog components in signal-processing systems with their digital counterparts for improved reliability, flexibility, and process portability. In some radio systems, for example, the intermediate frequency (IF) is directly and efficiently digitized by a bandpass analog-to-digital converter (ADC) and digitally downconverted to baseband as shown in Fig. 1(a). This scheme eliminates the final analog downconverter from a receiver, and does not suffer from flicker noise or phase mismatch of the quadrature oscillator. Since the center frequency (f_c) of a bandpass ADC is usually fixed, the signal band of interest is required to be well aligned with f_c. In a radio receiver, this requires an oscillator with a variable frequency to place the band of interest within the passband of the ADC for channel selection.

A delta-sigma modulator with a variable f_c allows the variable oscillator to be replaced with a fixed-frequency one [1] as shown Fig. 1(b), and may allow the same modulator to be used for different IFs or applications. Since the receiver in Fig. 1(b) does not require a variable oscillator, one local oscillator's output may be simply divided to generate the other local frequencies and clocks for the ADC and the digital signal processor (DSP), thus requiring fewer phase-locked loops (PLLs). In exchange for these benefits, the required bandwidth of the blocks before the ADC is increased, and the filter before the ADC may need to be programmable depending on the system's dynamic range requirement. Continuous-time bandpass delta-sigma modulators with analog tuning of the resonators' resonant frequencies have been reported in [2] and [3]. Both are single-bit modulators which, compared to multi-bit modulators, require a high oversampling ratio (OSR) and, hence, high sampling frequency (f_s) for sufficient signal-to-noise ratio (SNR) and bandwidth. To achieve such high sampling frequencies, both were fabricated in fast technologies (BiCMOS for [2] and and HBT for [3]). Also, both have a relatively narrow tuning range $(< 0.15f_s)$.

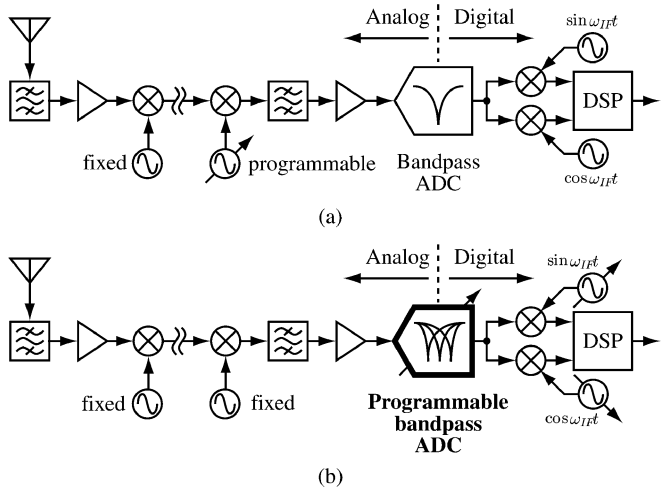

Fig. 1. (a) A typical digital radio receiver with a bandpass ADC. (b) A possible digital radio receiver with a bandpass ADC with a programmable center frequency.

Little work has been done on discrete-time implementations of delta-sigma modulators with programmable f_c. Two implementations of programmable discrete-time modulators were reported in [4] and [5]. Single-bit quantization and limited programmability of just a few coefficients restricted these designs to narrow tuning ranges $(< 0.2f_s)$ and high OSRs (i.e., small bandwidth) for modest SNRs (<60 dB).

In this work, a discrete-time 4-bit fourth-order delta-sigma modulator with f_c programmable from DC to $0.31f_s$ in steps of $0.0052f_s$ is described. Architectural and circuit-level design techniques to minimize the power and the overhead associated with this programmability will be described in Sections II and III, respectively. Experimental results are presented in Section IV. Despite the wide f_c tuning range, the modulator demonstrates performance competitive with that of recently

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The authors are with the Department of Electrical Engineering, University of Toronto, Toronto, ON M5S3G4 Canada (e-mail: kentaro@eecg.toronto.edu).

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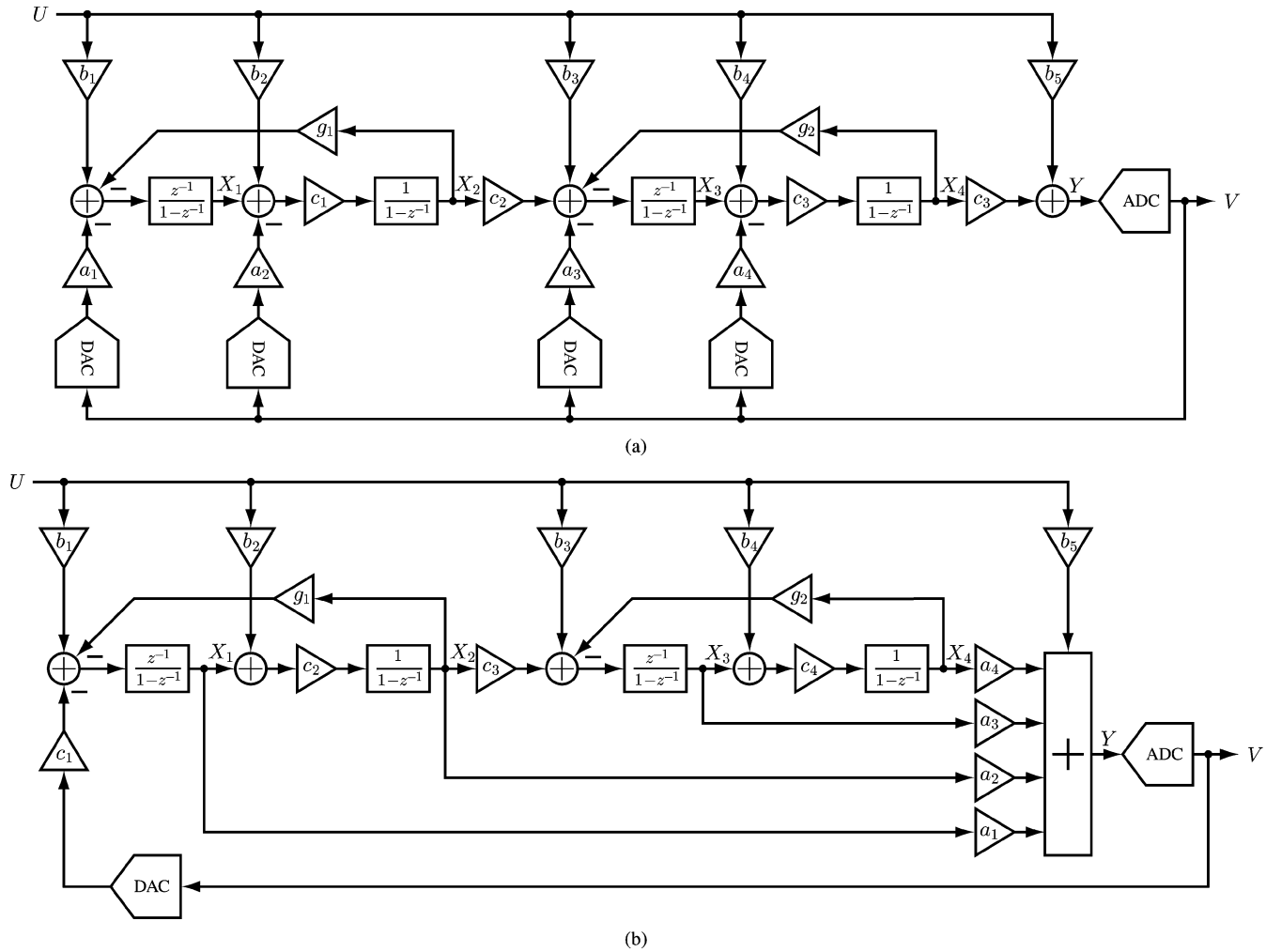

Fig. 2. (a) Fourth-order CRFB topology. (b) Fourth-order CRFF topology.

reported discrete-time bandpass delta-sigma modulators with a fixed f_c and similar bandwidth.

II. Modulator Architecture

In a bandpass delta-sigma modulator, resonators are designed to provide a high loop gain within the band of interest, providing high attenuation of the quantization noise at frequencies around f_c. In other words, the resonant frequencies of the resonators correspond to the zeros of the noise transfer function (NTF). Therefore, f_c-programmability of a bandpass delta-sigma modulator is achieved by changing the resonant frequencies of its resonators. However, this approach is only suitable when adjusting f_c over a narrow range as in [4] and [5]. In order to maintain stability and SNR over a wide range of f_c, it is imperative that other parameters such as the NTF poles, signal transfer function (STF), and signal swings of resonators' outputs be controlled in addition to the resonant frequencies by programming more modulator coefficients.

The modulator coefficients are programmed using banks of digitally switchable unit capacitors. The number of unit capacitors in each bank determines the resolution of the corresponding coefficient. In order to accurately set the NTF, STF, and integrators' output swing for high SNR and stability, high resolution is required in the modulator coefficients. However, increasing the coefficient resolution results in larger capacitor banks and, hence, more silicon area and power dissipation. A delta-sigma modulator with f_c programmability suffers a disadvantage in power consumption since the capacitor sizes and operational transconductance amplifier (OTA) design cannot be simultaneously optimized for power and thermal noise for all possible values of f_c. Therefore, it is important to minimize capacitor sizes by minimizing resolution of the modulator coefficients to limit the power overhead of the OTAs. This was the primary consideration in choosing a modulator topology.

A. Modulator Topology

There are two generic discrete-time topologies of a delta-sigma modulator with resonators. One is Cascade of Resonators with Feedback (CRFB) and the other is Cascade of Resonators with Feed Forward (CRFF) [6]. Block diagrams of fourth-order CRFB and CRFF delta-sigma modulators are shown in Fig. 2. For implementation of a delta-sigma modulator with wide f_c-programmability, the CRFF topology is advantageous for the following reasons.

Both CRFB and CRFF architectures shown in Fig. 2 include input feed-forward which eliminates the input-signal content

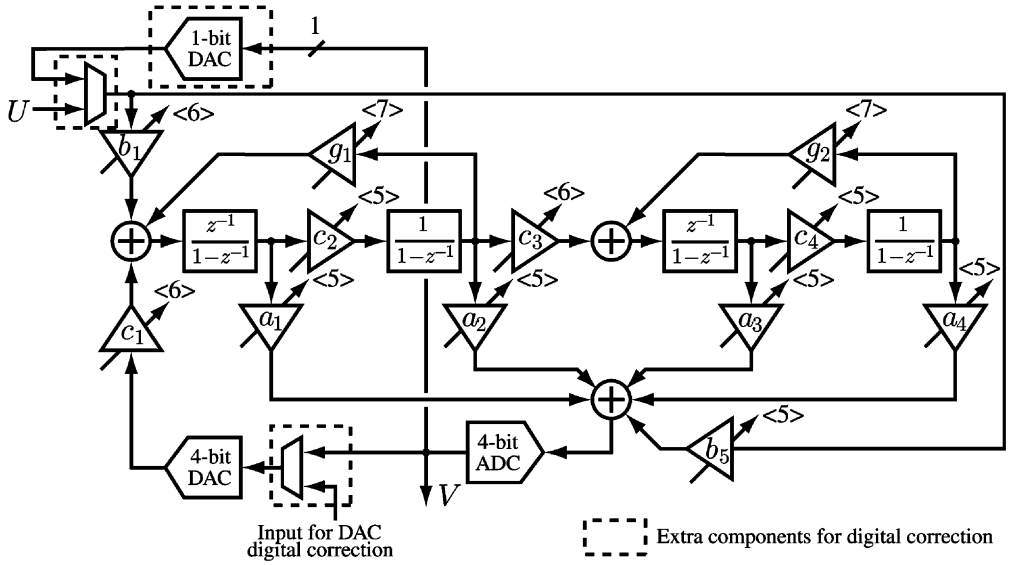

Fig. 3. Block diagram of the implemented modulator.

from the loop filter thus relaxing the performance requirements of the loop filter [7]. Furthermore, to this, if designed properly, input feed-forward flattens the STF to a constant without any peaking [6]. A constant STF without peaking prevents undesirable amplification of out-of-band interferers that may overload the quantizer. Both CRFB and CRFF can provide a flat STF if coefficients are set properly. However, the CRFB architecture requires that the input feed-forward coefficients b_1–b_4 match the feedback coefficients a_1–a_4 for a flat STF. Since coefficients a_1–a_4 are adjusted with f_c, a CRFB modulator with a widely programmable center frequency would therefore also require programmability of all four input feed-forward coefficients, b_1–b_4. The CRFF topology, on the other hand, requires that the feed-forward coefficients b_2–b_4 be zero. Hence, CRFF topology requires fewer programmable coefficients to enable f_c programmability. In addition, since the CRFF only has one feedback digital-to-analog converter (DAC), there is only one DAC whose nonlinearity needs to be compensated for in case of multi-bit delta-sigma modulation. The input feed-forward technique introduces critical timing in the feedback path [8]. However, this is not a big issue for implementation of this work since the sampling frequency is not high ($f_s = 40$ MHz). For these reasons, the CRFF topology shown in Fig. 3 was chosen rather than CRFB for implementation of the modulator in this work.

B. Modulator Coefficients and Quantization

Initial modulator coefficients were obtained with computer programs [6] that synthesize an NTF for each center frequency and order, and calculate the coefficients. With these coefficients, time-domain simulations were run to obtain the output swings of the loop-filter integrators for each f_c, and the modulator coefficients were scaled accordingly to maintain a reasonable swing at the output of the integrators without changing the NTF or STF. Large output swing of the integrators minimizes the input-referred thermal noise of the modulator.

As explained earlier in this section, one of the challenges in the system-level design of a delta-sigma modulator with programmable f_c is quantization of the modulator coefficients. Quantization of the coefficients introduces quantization errors in the coefficients, which slightly change the NTF zeros, NTF poles, the output swing of the integrators, and the STF. Among these parameters, the SNR is particularly sensitive to the NTF zero locations, which are determined by the resonators' resonant frequencies. Therefore, the coefficients that determine the resonators' resonant frequencies must be quantized in a way that minimizes the errors in f_c, but incurs minimal overhead. Fig. 4 shows a block diagram of a discrete-time resonator whose resonant frequency is

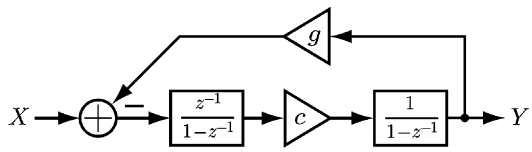

Fig. 4. Discrete-time resonator.

$$f_r = \frac{\tan^{-1}\frac{\sqrt{4cg-c^2g^2}}{2-cg}}{2\pi}. \quad (1)$$

The resonant frequency is a function of cg, which is a product of two variables that have to be quantized. A straightforward approach to quantizing these coefficients is to perform quantization for c and g independently. However, this approach introduces a large error in the product cg and hence, the resonant frequency, so quite high resolutions for both c and g are required, thus imposing a large hardware overhead. A better approach is to quantize one coefficient (c) coarsely and quantize the other coefficient (g) with high resolution while taking into account the quantization error of c in a way that minimizes the error of the product cg. How coarsely c can be quantized depends on the tolerance of the architecture to errors in other parameters such as the NTF pole locations, integrator output swing, and the STF. The resolution of the modulator coefficients was minimized according to this approach with the aid of extensive be-

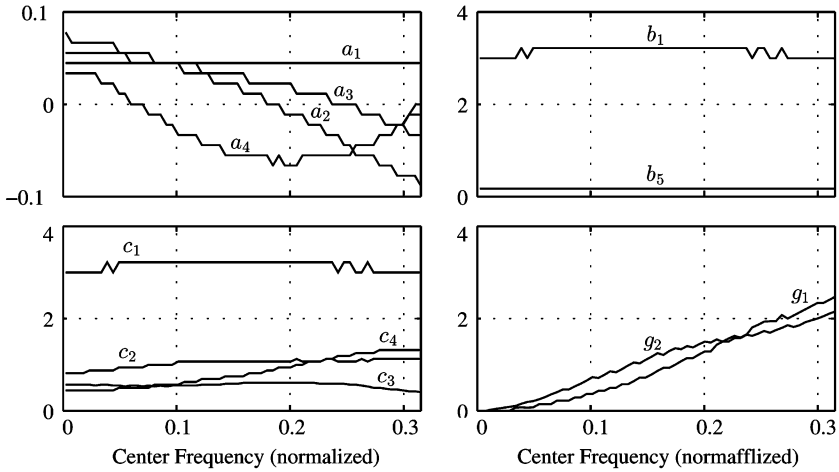

Fig. 5. Modulator coefficients after quantization.

havioral simulations. It is difficult to predict how quantization of the modulator coefficients will affect the statistics of the resonators' output swing. The complicated relationship between f_c and the coefficients shown in (1) makes it even harder to predict the required coefficient resolution. Therefore, simulations were used to determine the minimum required resolution of the coefficients for a given f_c step.

The numbers in angled brackets in Fig. 3 indicates the resolution of each coefficient in bits, and Fig. 5 shows all of the coefficient values after quantization over f_c.

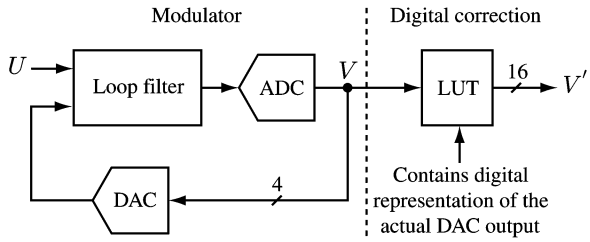

Fig. 6. Feedback DAC digital correction.

C. Feedback DAC Nonlinearity Compensation

Although dynamic element matching (DEM) is a popular technique for feedback DAC nonlinearity compensation in multi-bit delta-sigma modulators, its application to a delta-sigma modulator with f_c programmability would be complicated by the need to tune the DEM transfer function for different values of f_c. Therefore, the digital correction technique described in [6] for correction of a multi-bit feedback DAC outside the modulator loop was employed here instead. A block diagram of the correction scheme is shown in Fig. 6. In this technique, nonlinearity of the feedback DAC is compensated by replacing the digital output of the ADC (V) with a high-precision digital representation of the actual DAC output for the same input code V. This is done outside the modulator loop in the digital domain as shown in Fig. 6. The look-up table in Fig. 6 contains the digitized DAC output values for all possible digital input codes. Therefore, in order to create the look-up table, off-line linear A/D conversion of the feedback DAC output is needed prior to the normal operation of the delta-sigma modulator. We call this a calibration mode. In [9], a delta-sigma modulator is reconfigured such that the output of the feedback DAC is taken as the input of the modulator with a single-bit feedback DAC, which is inherently linear; in this way, linear measurement of the multi-bit DAC output is performed. For this work, the same technique is used to obtain linear digital representation of the multi-bit feedback DAC output by transforming the original modulator to a single-bit second-order delta-sigma modulator with the multi-bit feedback DAC as the input. Since the modulator must be highly reconfigurable to accommodate f_c programmability anyway, this facility is implemented with little hardware overhead as shown in Fig. 3. Circuit-level details are described in Section III. Fig. 7 shows how the original modulator in Fig. 2(b) can be transformed for the calibration mode. High-precision digital representations of the feedback DAC output that are obtained in the calibration mode replace the output of the ADC during normal operation of the modulator as shown in Fig. 6.

III. Modulator Circuit Implementation

The switched-capacitor (SC) representation of the modulator with the extra circuitry for DAC nonlinearity digital correction is shown in Fig. 8. It consists of four SC integrators arranged into two resonators. The last OTA with its SC branches sums the feed-forward signals from the integrators and the modulator input together, and passes the sum to a 4-bit flash ADC. The digital output of the ADC is fed to the 4-bit SC feedback DAC. Table I relates the capacitances in the circuit to the modulator coefficients. The common-mode voltage $\mathrm{V_{CM}}$ is 0.9 V, which is half the supply voltage, everywhere in the circuit.

With the exception of the first integrator, sampling capacitors were made programmable while the integrating capacitors were kept fixed providing linear control of the modulator coefficients. An exception was made at the input because the sampling capacitor size in the first integrator (C_{Sb_1}) directly affects the modulator's SNR since the thermal noise of that stage is not noise shaped at all. In addition, the sampling capacitor has to

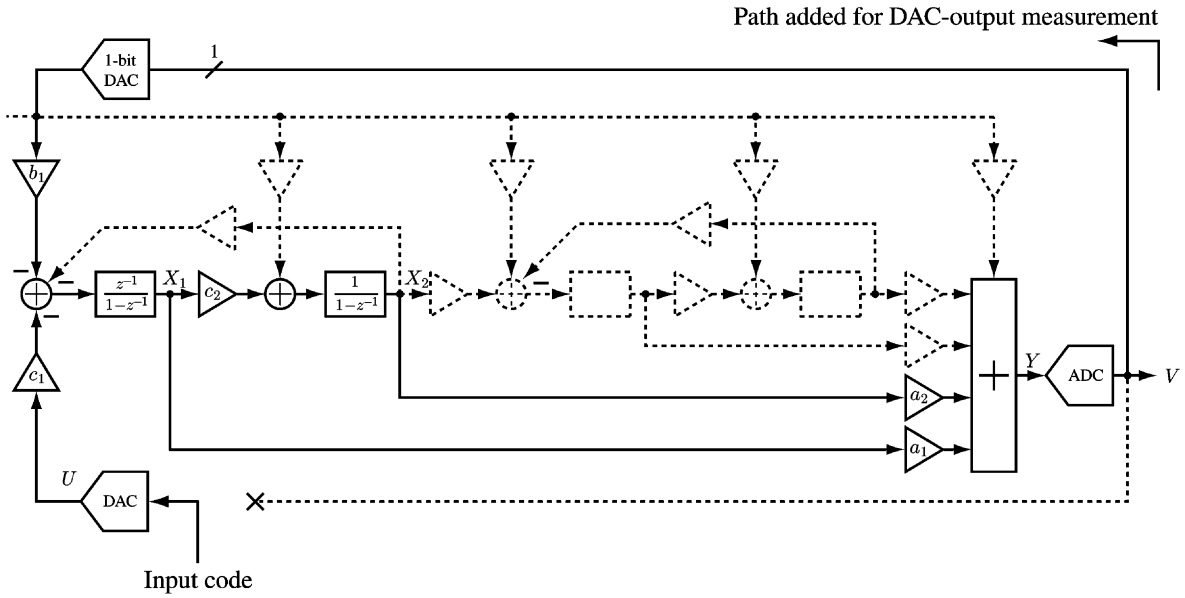

Fig. 7. Modulator block diagram in the calibration mode.

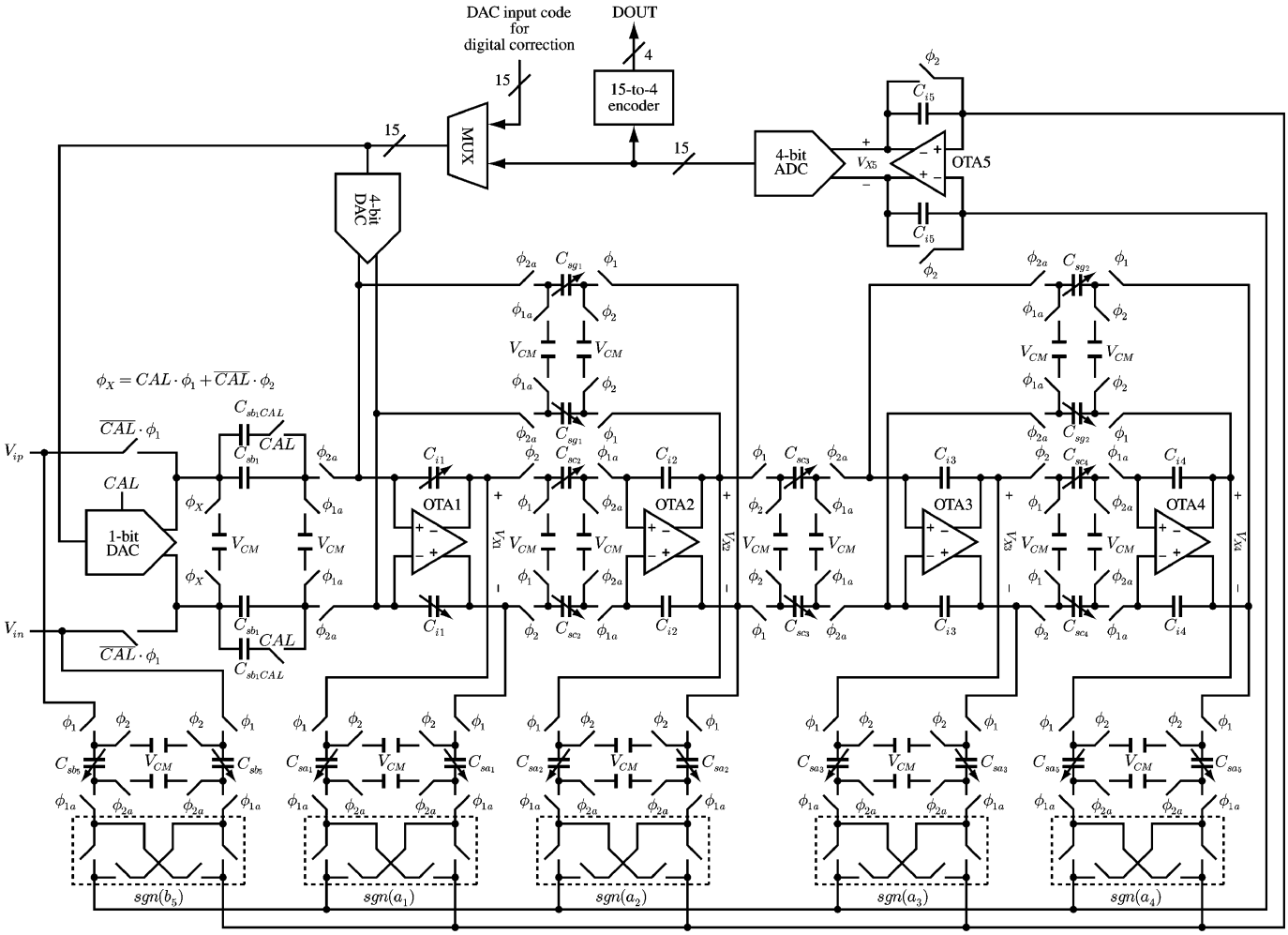

Fig. 8. Circuit implementation of the modulator.

match the capacitance of the feedback DAC to maintain a constant STF. Therefore, the integrating capacitors (C_{i1}), which are shared by the SC feedback DAC and the first integrator, were made programmable rather than the sampling capacitors (C_{sb_1}) for this integrator. In Fig. 8, the variable capacitor symbols are used to represent digital coefficient programmability. The actual SC implementation of the digitally programmable coefficients is described later in this section.

TABLE I
MODULATOR COEFFICIENTS IN TERMS OF CAPACITANCES

a_1	a_2	a_3	a_4	b_1	b_5	c_1	c_2	c_3	c_4	g_1	g_2
$\frac{C_{sa_1}}{C_{i5}}$	$\frac{C_{sa_2}}{C_{i5}}$	$\frac{C_{sa_3}}{C_{i5}}$	$\frac{C_{sa_4}}{C_{i5}}$	$\frac{C_{sb_1}}{C_{i1}}$	$\frac{C_{sb_5}}{C_{i5}}$	$\frac{\sum C_d}{C_{i1}}$	$\frac{C_{sc_2}}{C_{i2}}$	$\frac{C_{sc_3}}{C_{i3}}$	$\frac{C_{sc_4}}{C_{i4}}$	$\frac{C_{sg_1}}{C_{i1}}$	$\frac{C_{sg_2}}{C_{i3}}$

A. Thermal Noise

Programming the modulator coefficients involves changing the sizes of switched capacitors. Changes in capacitance affect the modulator's input-referred thermal noise and the SNR. Therefore, the input referred thermal noise has to be analyzed for all possible f_c values to ensure sufficient SNR.

The dominant contributors to the input-referred thermal noise are the first resonator and the SC feedback DAC. The in-band input-referred thermal noise contributed by the other components is negligible due to the noise shaping provided by the high gain of the first resonator. The input-referred noise contributed by the first resonator and the SC feedback DAC can be approximated as

$$\overline{e_i^2} = \frac{4kT}{\mathrm{OSR}}\left(\frac{1}{C_{sb_1}} + \frac{\sum C_d}{C_{sb_1}^2} + \frac{C_{sg_1}}{C_{sb_1}^2} + \frac{1}{b_1^2 C_{sc_2}}|1 - e^{-j2\pi f_c}|^2\right) \quad (2)$$

where C_{sx_n} are the values of the sampling capacitors corresponding to the modulator coefficients x_n, and C_d is the unit capacitor size of the DAC. The input-referred thermal noise increases with f_c mainly due to the accompanying increase in C_{sg_1}, which is proportional to the coefficient g_1, and $|1 - e^{-j2\pi f_c}|$. The first and the second terms of (2) are fairly constant over f_c since C_{sb_1} and ΣC_d are constant, and C_{sc_2} does not vary much. In order to decrease the input-referred thermal noise, C_{sb_1} and C_{sc_2} should be increased or C_d has to be decreased. Since the ratio of C_{sb_1} and the amount of the charge transfered by the DAC (which is proportional to the product of the DAC reference voltage and C_d) has to be maintained constant to keep the STF unchanged, C_d cannot be simply decreased. The only way to decrease C_d while maintaining the same STF is to increase the reference voltage of the DAC, but it has a limit on it as explained later in this section. Unit capacitor sizes of the binary-weighted capacitors were determined using (2).

B. Programmable Switched Capacitor

A simplified single-ended version of a four-bit programmable integrator is shown in Fig. 9. It utilizes a binary weighted capacitor bank with gated clock signals that select which capacitors to charge and discharge. This structure provides a digitally programmable SC without placing additional MOS switches in series with the capacitors. Therefore, the coefficient programmability does not increase the *RC* time constants of the switched-capacitor circuits.

The clock signal is gated by transmission gates instead of typical CMOS logic gates. The reason that transmission gates are preferred over CMOS logic is that if logic gates are used, they have to be sized carefully for switches of different sizes in order to avoid clock skew between the switches, which would decrease the time available for the switched capacitors to charge and discharge. Furthermore, having strong gate drivers near the sensitive SC circuit may introduce noise coupling and complicate digital power supply routing. On the other hand, if transmission gates are used, as long as they are large enough, the skew is minimized without fine size tuning, and the clock driver can be placed far away from the sensitive locations at the expense of some extra power to drive the large transmission gates.

As mentioned earlier, for the first integrator, the integrating capacitors C_{i1} are made programmable instead of the sampling capacitors C_{sb_1}. The integrating capacitors were made programmable using a binary-ratioed array with series switches, as shown in Fig. 10.

As shown in Fig. 5, $a_1 - a_4$ are the only coefficients whose sign changes. Therefore, switched-capacitor branches for these coefficients have extra switches to flip the signal polarity as shown in Fig. 8.

C. Operational Transconductance Amplifier

The time constant of an OTA with a capacitive feedback and a capacitive load is expressed as

$$\tau = \frac{1}{g_m}\frac{C_L}{\beta} \quad (3)$$

where C_L is the total load capacitance, β is the feedback coefficient, and g_m is the transconductance of the OTA. For all of the OTAs in the modulator, since both β and C_L change with f_c, (C_L/β) changes with f_c as well. In order to ensure sufficient settling accuracy, g_m has to be made large enough for the worst case, when the ratio (C_L/β) is at a maximum. Fig. 11 shows the ratio (C_L/β) of all OTAs for all center frequencies. All of the OTAs suffer the largest ratio at the maximum f_c. Therefore, the g_m of the OTAs are designed for this worst case. This implies some power overhead when configuring the modulator with a low center frequency since the OTA outputs will settle faster than necessary.

The fact that both C_L and β change with f_c makes compensation of the OTAs difficult especially for a two-stage OTA architecture since its second pole location varies a lot depending on C_L; furthermore, large power consumption would be required to place the second pole far enough from the first pole to ensure sufficient phase margin for any f_c. Therefore, for this work, a single-stage architecture is selected since it is stable as long as the second pole, which is at the internal node, is placed far enough from the maximum possible first pole, which is at the output node. In order to achieve large output swing and a large DC gain, the standard pMOS-input folded-cascode architecture was selected for all of the five OTAs. The first four

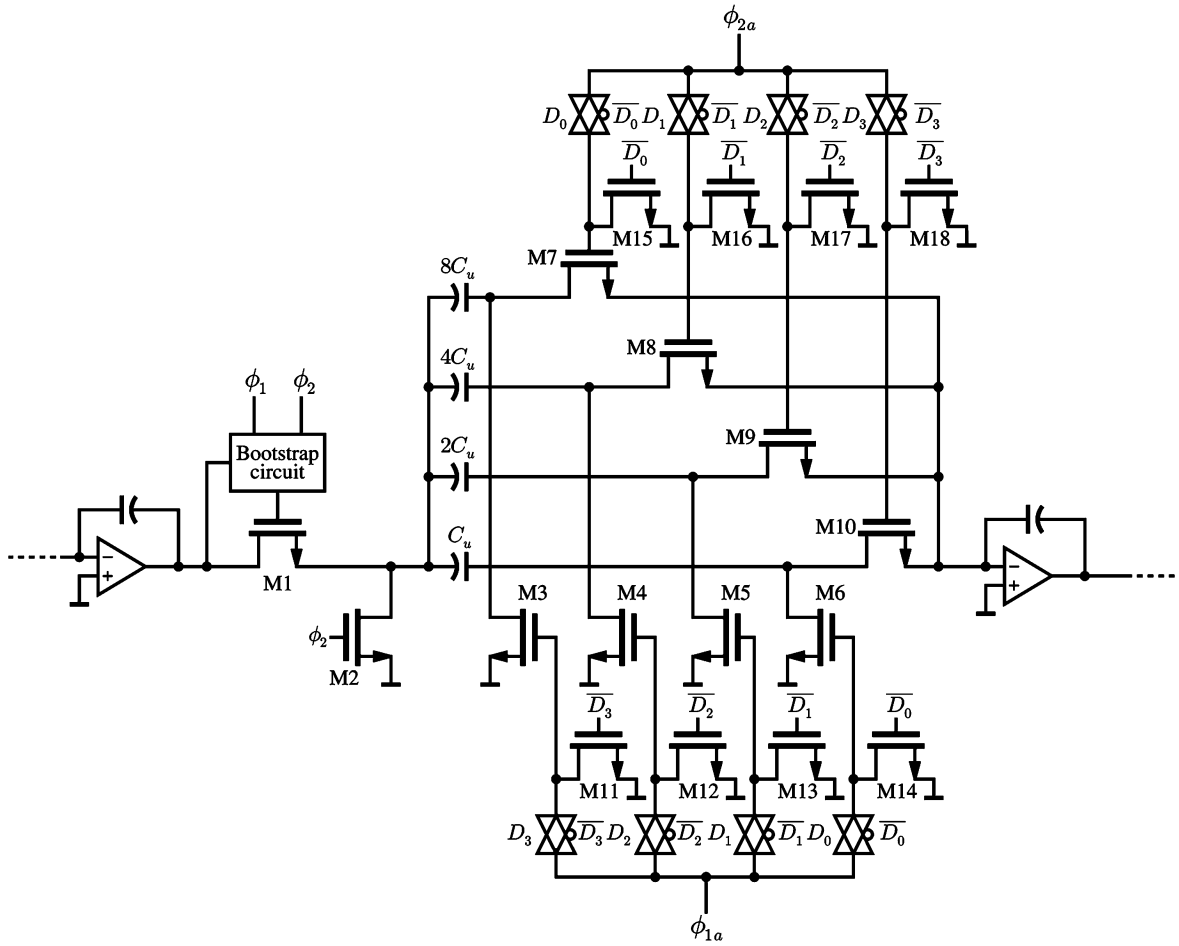

Fig. 9. Simplified schematic of a programmable integrator.

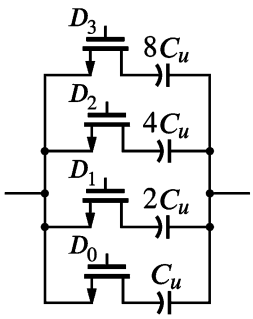

Fig. 10. Implementation of C_{i1}.

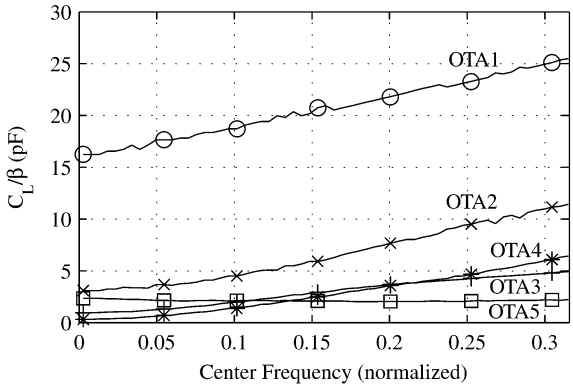

Fig. 11. C_L/β of the OTAs.

OTAs are gain boosted by gain enhancement circuits [10] for accurate coefficient settings and improved linearity since coefficients associated with these OTAs affect the NTF zero locations, which must be very accurately set to achieve high SNR. For the last OTA, however, an OTA without gain enhancement was used; its gain can be much lower without affecting the NTF zero locations.

All switches in the integrators are nMOS switches. The input switches of each integrator are bootstrapped as described in [11] for linearity enhancement.

D. ADC and DAC

The ADC used for the modulator is a simple 4-bit flash ADC with 15 comparators. Each comparator consists of a continuous-time preamplifier followed by a regenerative latch. Due to the limited input range of the preamplifier, the reference voltage of the ADC was set to ± 0.6 V (differential), and its input swing was scaled accordingly in the system-level design.

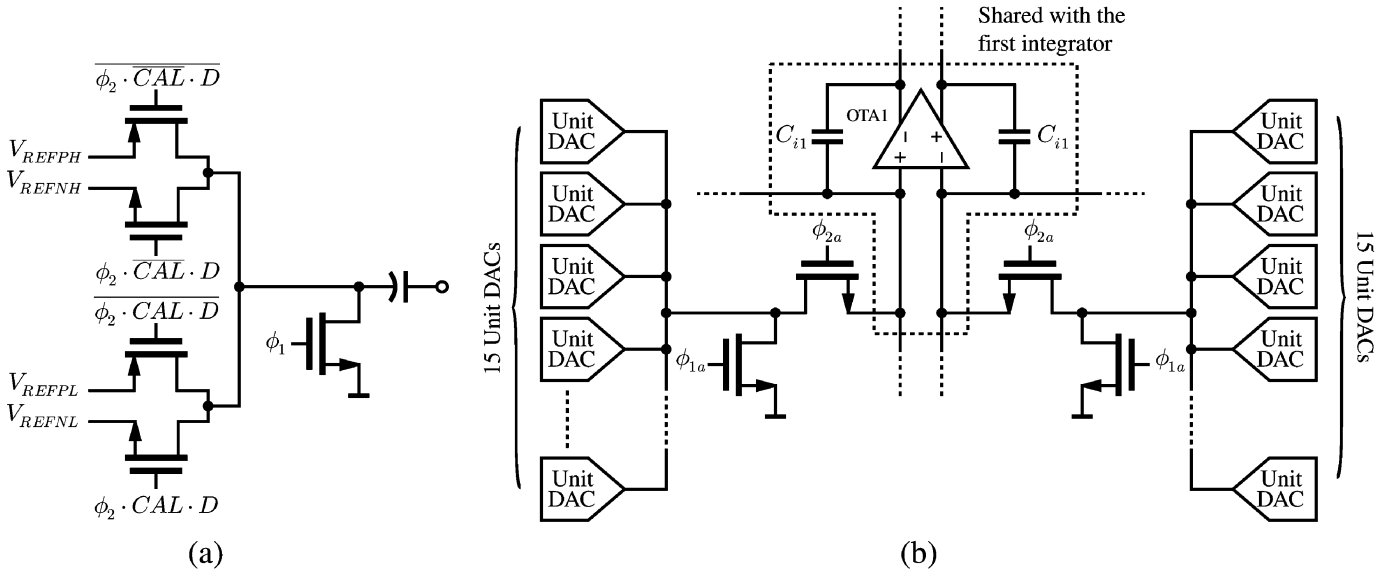

Fig. 12. (a) Unit DAC element. (b) SC 4-bit DAC.

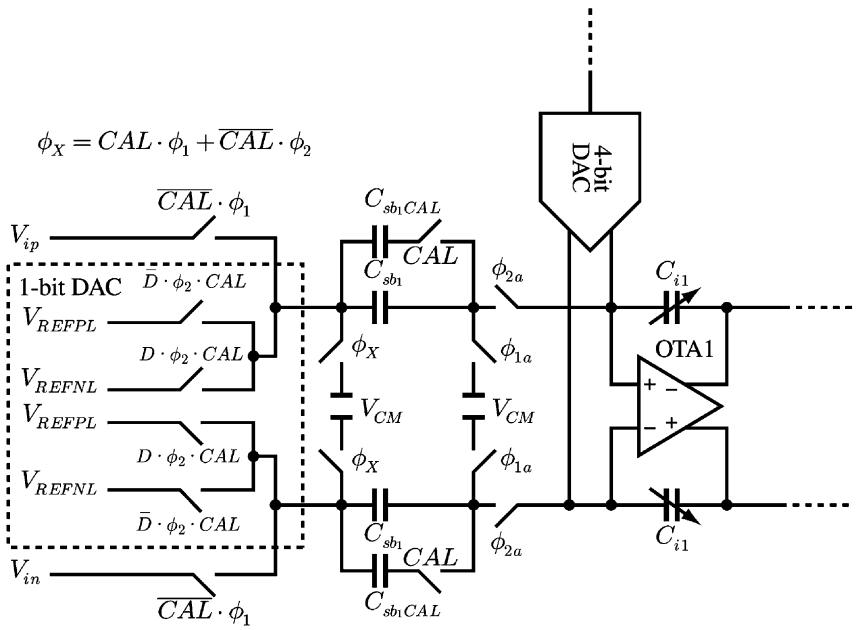

Fig. 13. First integrator with calibration related circuits shown.

The multi-bit DAC used for the modulator is a simple 4-bit switched capacitor DAC shown in Fig. 12. It shares the integrating capacitor C_{i1} with the first integrator. The reference voltage during the normal operation was made $\pm(V_{\mathrm{REFPH}} - V_{\mathrm{REFNH}}) = \pm 1.8$ V (differential), which is the maximum possible value with a 1.8 V supply, in order to minimize the thermal noise contribution by this DAC. Maximizing the reference voltage minimizes C_d, which is the DAC unit capacitor size, in (2). The other pair of reference voltages (V_{REFPL} and V_{REFNL}) are used during the calibration mode as explained later in this section.

E. Circuit Modification for Feedback DAC Digital Correction

As explained in Section II, before normal operation of the modulator, the circuit is configured as a second-order single-bit delta-sigma modulator with the output of the multi-bit feedback DAC taken as the modulator input in order to take linear measurements of the multi-bit feedback DAC output. This configuration requires a few modifications to the switched-capacitor branch of the first integrator and the multi-bit feedback DAC.

Fig. 13 shows the first integrator with the extra circuits for digital correction. When $\mathrm{CAL} = 1$ the modulator is in calibration mode, taking measurements of the multi-bit feedback DAC output, and when $\mathrm{CAL} = 0$ the modulator is in normal operation. By adding extra switches (shown in a dotted box in Fig. 13) to the first switched-capacitor branch, it can be used as a single-bit DAC as required for the calibration mode. With these switches enabled, and the analog-signal input switches disabled, C_{sb_1} is charged to either $V_{\mathrm{REFPL}} = 1.05$ V or $V_{\mathrm{REFNL}} = 0.75$ V depending on the digital input to this single-bit DAC. The capacitors added in parallel with C_{sb_1} are used to change the modulator coefficient during the calibration phase.

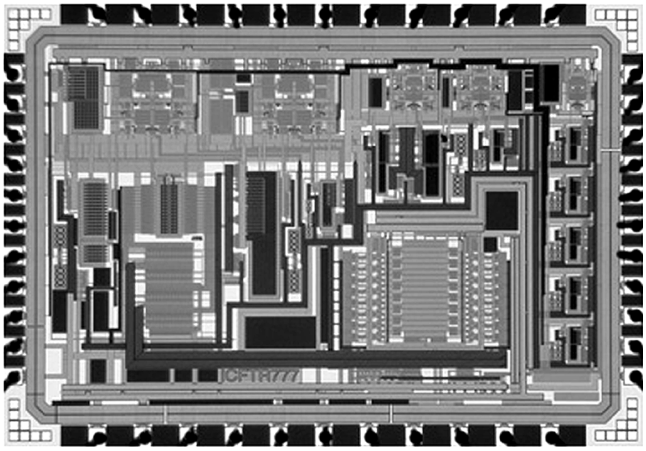

Fig. 14. Die photo of the modulator.

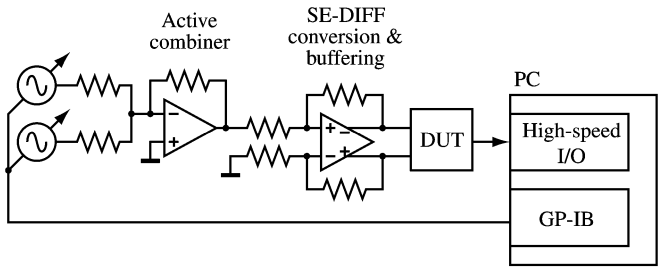

Fig. 15. Block diagram of the test setup.

For the calibration mode, it is necessary to change the reference voltage of the multi-bit DAC from its usual ± 1.8 V (differential) to ± 0.3 V, which is same as the same reference voltage of the single-bit DAC in order to prevent overloading of the integrators. This requires extra switches as shown in Fig. 12.

The multi-bit ADC is simply used as a single-bit ADC by truncating all of the bits other than the MSB, which is the sign bit.

The test input to the multi-bit DAC is externally supplied, and the output is captured off chip for decimation. Decimation is simply averaging a large number of samples since the signal under measurement is a DC quantity. Sixteen possible DAC codes are tested, and the averaged values are stored in the digital-correction look-up table shown in Fig. 7 and used during normal operation of the modulator.

IV. Experimental Results

The modulator implemented in a one-poly six–metal (1P6M) 0.18 μm CMOS technology occupies a core area of 3.2 mm^2 and die area of 4.5 mm^2 including the pad frame. Fig. 14 shows a die photo of the modulator. Testing had to be automated due to a large number (60) of f_c settings. Fig. 15 shows a block diagram of the test setup. A PC sets the amplitude and the frequency of one or two signal generators via a GP–IB interface, and captures the digital output of the modulator for processing and analysis. A single low-noise low-distortion signal generator was used for $f_c = 0$ Hz, but could not be used for other center frequencies due to its low maximum output frequency. Two high-frequency signal generators were used for all other

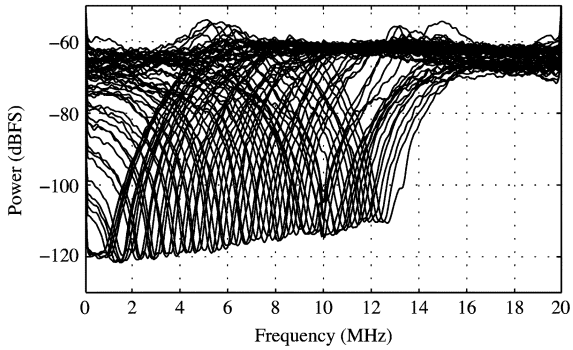

Fig. 16. Smoothed zero-input spectra of the modulator for all possible f_c.

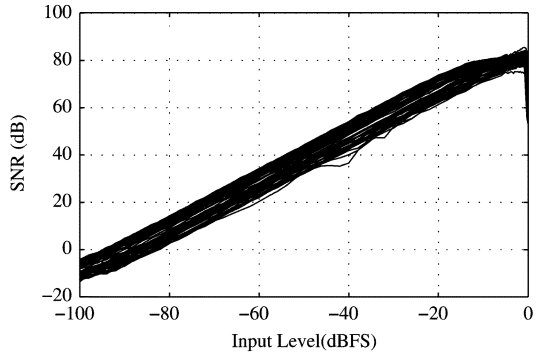

Fig. 17. Measured SNR versus input amplitude for all f_c.

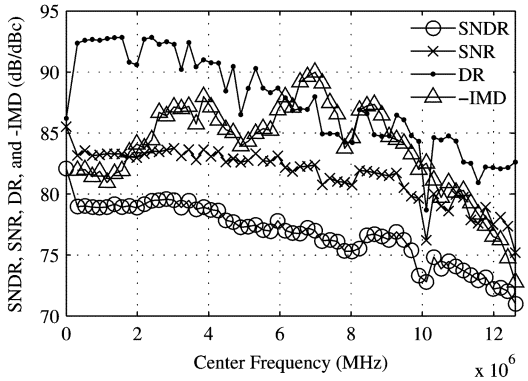

Fig. 18. Measured peak SNDR, SNR, IMD, and DR over f_c.

f_c-settings. Both two-tone and single-tone test signals were converted to differential signals and buffered by a commercially available fully differential operational amplifier. The two-tone test signals were generated by using an active summing amplifier since a passive combiner causes cross-modulation between the two signal generators due to insufficient isolation between the input ports.

Fig. 16 demonstrates the f_c programmability. Fig. 16 was obtained by plotting smoothed zero-input spectra on top of each other for different f_c settings. What is seen are the spectra of the quantization noise only for visual presentation of the f_c programmability. As expected from (2), the noise floor rises as f_c increases.

The SNR and the dynamic range were measured with a single-tone input. SNR versus input amplitude and dynamic range for all possible center frequencies are shown in Figs. 17 and 18, respectively. For $f_c = 0$ Hz, the modulator was

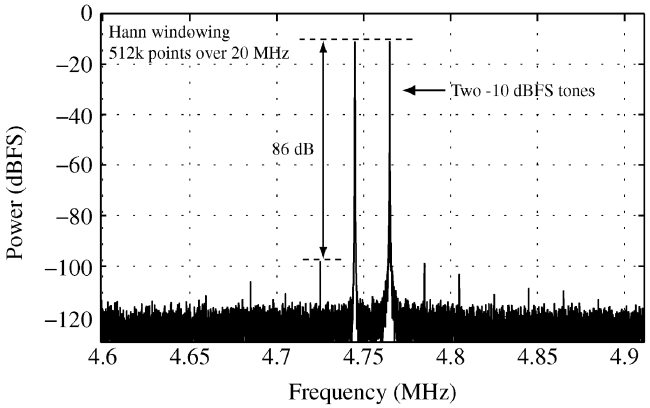

Fig. 19. Zoomed measured spectrum at $f_c = 4.78$ MHz.

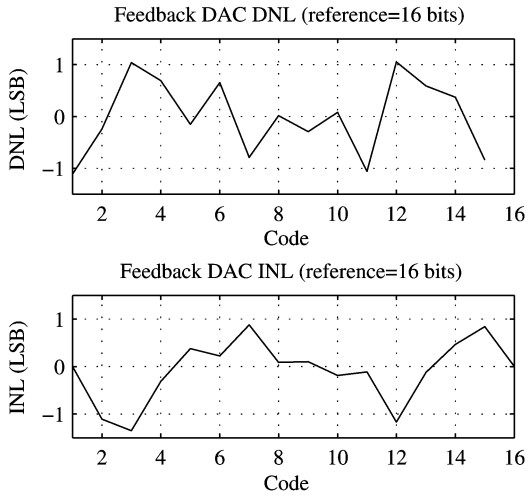

Fig. 20. Measured DNL and INL of the DAC.

treated as a low-pass modulator for calculation of the SNR and dynamic range. The SNR saturates because noise from the signal generator starts limiting the SNR at high amplitude for $f_c \neq 0$ Hz. A synthesized signal generator with single sideband (SSB) phase noise of -131 dBc/Hz at 20 kHz offset for a carrier frequency of 100 kHz was used for $f_c \neq 0$ Hz. This observation is supported by the fact that the dynamic range values shown in Fig. 18 are much higher than the peak SNR values. For $f_c = 0$ Hz, however, the SNR does not saturate since a low-frequency low-noise signal generator for audio testing with higher spectral purity was used, but the peak SNR and dynamic range are instead limited by flicker noise generated inside the modulator. For this case, the SNR and dynamic range are in close agreement as shown in Fig. 18.

Two-tone inputs were conducted for all linearity tests (SNDR and IMD) except for $f_c = 0$ Hz since the low-order harmonics of a single-tone input stay within the band of interest in that case. Fig. 18 shows the peak SNDR and IMD measured with two -10 dBFS tones (-4 dBFS in total) at which the peak SNDR was obtained. Fig. 19 shows the output spectrum of the modulator for one of the two-tone measurements.

Multi-bit DAC calibration data obtained during the calibration phase was processed on a PC to create a look-up table for multi-bit DAC digital correction. During normal operation of the modulator, this look-up table was used in order to replace the output of the 4-bit ADC with high-precision digital representations of the feedback DAC output levels measured in the calibration mode. Digital correction made a negligible difference in performance. In order to investigate this unexpected result, the linearity of the multi-bit DAC was measured using the calibration feature of the modulator. The measured DNL and INL of the DAC are shown in Fig. 20, which indicates static linearity of close to 14 bits. Therefore, it is assumed that the implemented multi-bit DAC is linear enough for the modulator to achieve the linearity shown in Fig. 18. These results were confirmed across three dice.

Table II summarizes the performance of the implemented modulator. Table III compares the performance of this work with published fixed-f_c discrete-time bandpass delta-sigma modulators with similar bandwidth as well as one with programmable f_c. It can be seen that performance of this work is

TABLE II
SUMMARY OF THE EXPERIMENTAL RESULTS

Technology	0.18-μm 1P6M CMOS
Die Size	2.55 mm x 1.77 mm (4.5 mm^2)
Core Area	2.21 mm x 1.43 mm (3.2 mm^2)
Architecture	4-bit 4-th order CRFF
f_s	40 MHz
OSR	64
BW	310 kHz
f_c	0-12.6 MHz ($0.31 f_s$)
f_c step	208 kHz ($0.0052 f_s$)
VDD	1.8 V
Power	115 mW
SNDR	82-71 dB
SNR	86-75 dB
DR	96-76 dB
IMD	-(90-73) dB

TABLE III
COMPARISON WITH RECENT FIXED-f_c DISCRETE-TIME BANDPASS DELTA-SIGMA MODULATORS

	f_s (MHz)	f_c (MHz)	BW (kHz)	SNDR (dB)	SNR (dB)	DR (dB)	IMD (dBc)	P (mW)
This work	40	0-12.6	310	82-71	86-75	93-76	-(90-73)	115
[12]	37.05	10.7	200	-	72	78	-65	88
[13]	42.8	10.7	200	61	-	74	-75	76
[14]	80	20	270	78	80	86	-	24
[4]	2.358	0.47-0.7	12	-	47	-	-	-

comparable with those in Table III despite the wide f_c tuning range. One major drawback is the silicon area.

V. Conclusion

A successful implementation of a delta-sigma modulator with a wide f_c tuning range was presented. Despite the wide f_c programmability, the performance of the modulator is still competitive with other discrete-time bandpass delta-sigma modulators with similar bandwidth.

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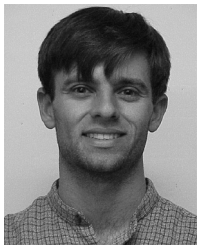
Kentaro Yamamoto (S'05) received the B.S. degree in electrical engineering from the University of Texas at Arlington in 2004, and the M.A.Sc. degree from the University of Toronto, Toronto, ON, Canada, in 2006. He is currently working toward the Ph.D. degree at the University of Toronto.

He was with Qualcomm Inc. as an intern during the summer of 2008.

Mr. Yamamoto received the Analog Devices Outstanding Student Designer Award in 2007. He is the winner of the Best Student Paper Award at the IEEE Custom Integrated Circuits Conference (CICC) in 2007.



Anthony Chan Carusone (S'01–M'07–SM'08) received the B.A.Sc. and Ph.D. degrees from the University of Toronto, Toronto, ON, Canada, in 1997 and 2002, respectively, during which time he received the Governor-General's Silver Medal.

Since 2001, he has been with the Department of Electrical and Computer Engineering at the University of Toronto where he is currently an Associate Professor. From 2002 to 2007, he held the Canada Research Chair in Integrated Systems.

Dr. Carusone was a coauthor of the best paper at the 2005 Compound Semiconductor Integrated Circuits Symposium and best student paper at the 2007 Custom Integrated Circuits Conference. He is a past chair of the Analog Signal Processing Technical Committee for the IEEE Circuits and Systems Society, a member of the technical program committee for the IEEE Custom Integrated Circuits Conference, and is currently the Deputy Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Express Briefs.

Francis Dawson (S'86–M'87) received the B.Sc. degree in physics and the B.ASc., M.A.Sc., and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1978, 1982, 1985, and 1988, respectively.

He worked as a process control engineer in the pulp and paper, rubber and textile industries during 1978–1980. From 1982 to 1984, he acted as a consultant on various projects. Development areas included high-frequency link power supplies, power supplies for specialized applications and high current protection circuits. Since 1988, he has been with the Department of Electrical and Computer Engineering at the University of Toronto where he is engaged in teaching and research. His areas of research interest include static power converters and their applications, signal processing in power engineering applications and device or process modeling. He has also participated as a Consultant or Project Leader in several industrial projects.

Dr. Dawson is a member of the Association of Professional Engineers of Ontario.