A 1-1-1-1 MASH Delta-Sigma Modulator With Dynamic Comparator-Based OTAs

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***Abstract*—A dynamic comparator-based OTA is introduced as a replacement for a conventional OTA. It performs charge transfer in a switched-capacitor circuit by repeatedly evaluating the polarity of the differential input using a dynamic clocked comparator and injecting current pulses at the output to move the input voltage toward zero. The amplitude of the current pulse is reduced each time the input voltage crosses zero to provide fast but accurate settling of the output voltage. Dynamic comparator-based OTAs are applied to the design of a 1-1-1-1 MASH delta-sigma modulator. The 65-nm CMOS prototype achieves a 70.4 dB peak SNDR over a 2.5-MHz bandwidth while consuming 3.73 mW from a 1.2-V supply. The 276-fJ/conv-step FoM represents a four times improvement over previously-reported delta-sigma modulators using zero-crossing-based circuits or comparator-based switched capacitors. Because of the dynamic operation of the OTAs and discrete-time delta-sigma modulator architecture, both bandwidth and power consumption linearly scale with the sampling frequency without any reconfiguration of the modulator.**

***Index Terms*—ADC, CBSC, delta-sigma modulator, DCBOTA, dynamic comparator, switched capacitor, ZCBC.**

I. Introduction

ZERO-CROSSING-BASED CIRCUITs (ZCBCs) [1] and comparator-based switched capacitors[1] (CBSCs) [2] have been proposed as alternatives for conventional OTA-based switched-capacitor (SC) circuits because of the difficulties in implementing high-gain conventional OTAs in nanometer CMOS technologies.

ZCBCs emulate the operation of a conventional OTA in a SC circuit (shown in Fig. 1(a)) by applying a current (I_o) at the output until the input voltage (V_g) crosses zero. For example, a dual-slope ZCBC [2]–[4] shown in the SC integrator example in Fig. 1(b) first applies a large current at the output until an input (V_g) zero crossing is detected by the zero-crossing detector (ZCD) and then applies a smaller current of the opposite sign until another V_g zero crossing is detected for finer settling. It should be noted that the ZCD output is the inverse of the V_g sign because of the reversed connection at the ZCD input. This is what provides the negative feedback to zero V_g.

As shown in Fig. 1(b), V_g overshoots zero leaving residual charge in C_s and thus non-zero V_g because of the time delay (t_d) between a V_g zero crossing and output current cutoff. This residual V_g can be directly referred to the input as the input-referred settling error, and is expressed as

$$V_{gn}(V_o) = m_n(V_o)t_d \tag{1}$$

where m_n is the final (nth) V_g slope of an n-slope ZCBC ($n = 2$ for Fig. 1(b)). Because of the nonidealities of the output current sources such as the finite output impedance and nonlinearity, m_n is not a constant but a nonlinear function of the output voltage (V_o) [5]. Therefore, V_{gn} and thus the input-referred settling error are also nonlinear functions of V_o. This nonlinearity limits the settling accuracy of a ZCBC.

Smaller m_n and t_d can improve the settling accuracy of a ZCBC, but neither is trivial. A small m_n may result in an excessively long settling time, and a small t_d is difficult to achieve due to the open-loop (as opposed to regenerative) nature of the ZCD needed to continuously monitor V_g during settling. All of the ZCBCs reported so far in the literature use an open-loop partially- or pseudo-differential amplifier or an open-loop single-ended dynamic amplifier [1] as the ZCD with the exception of [6], which uses a single-ended latch as the last stage. A ZCD based on an open-loop amplifier tends to be slow because amplifier stages with large output impedance are required to provide enough gain to generate a rail-to-rail logic output from a very small input signal. Furthermore, a partially-differential ZCD introduces additional DC offset, which needs to be corrected in some cases [6], [7].

The dynamic comparator-based OTA [8] presented in this paper addresses these issues by eliminating the need for a high-gain circuit continuously monitoring V_g and by using brief current pulses at the output. As shown in Fig. 1(c), V_g comparison is performed repeatedly followed by injection of a current pulse that moves V_g toward zero. Because V_g is constant during comparison, it does not need to be continuously monitored. This scheme allows use of a fully-differential regenerative dynamic comparator, which has shown its ability to efficiently resolve a small input with a small latency [9]. In addition, the dynamic latch in such a comparator resembles the sense amplifier in a memory readout circuit. Therefore, this scheme copes better with CMOS technology scaling driven by memory and digital circuits than the existing open-loop amplification approach.

Furthermore, the proposed OTA uses up to six different current pulse amplitudes during each settling operation. This is equivalent to using six different output slopes in conventional ZCBCs.

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[1]In this paper, CBSCs are generalized as ZCBCs since a CBSC is essentially a ZCBC except that a CBSC uses a comparator to detect zero crossings of its input while a ZCBC uses a zero-crossing detector which is a circuit block especially tailored for detecting zero crossings.

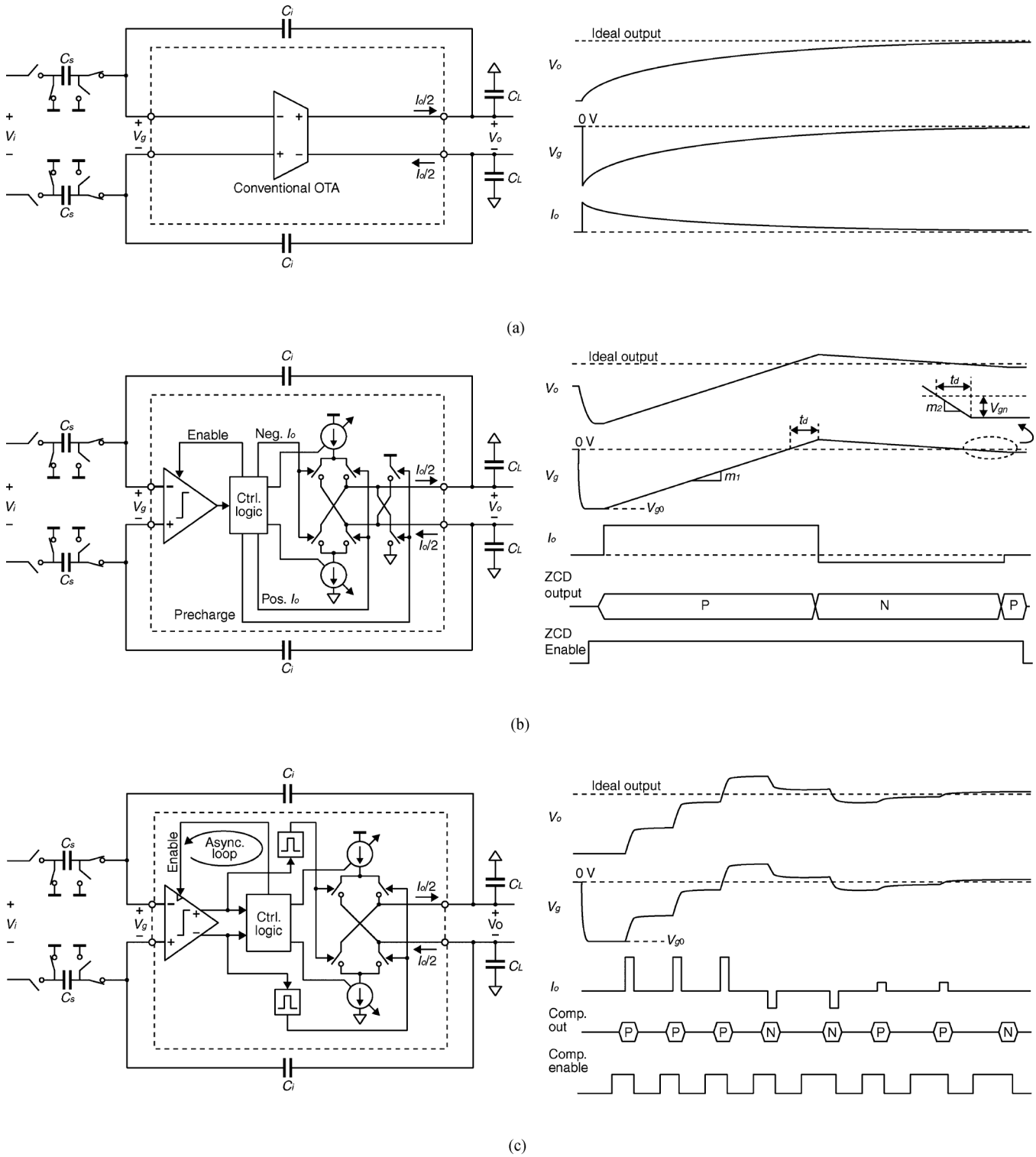


Fig. 1. SC integrators based on a conventional OTA (a), existing ZCBC (b), and the proposed dynamic comparator-based OTA (c).

This paper explores the system- and circuit-level details of the dynamic comparator-based OTA and its application in the 1-1-1-1 MASH delta-sigma modulator presented in [8]. In Section II, the settling behavior of the dynamic comparator-based OTA is described. Circuit design of the proposed OTA follows in Section III. Section IV covers the application of the proposed OTA in a 1-1-1-1 MASH delta-sigma modulator. Section V presents the experimental results of the prototype delta-sigma modulator.

Though this paper focuses on application of the proposed OTA to SC integrators for delta-sigma modulators, the OTA can also be applied to other types of SC circuits such as the MDACs in pipeline ADCs.

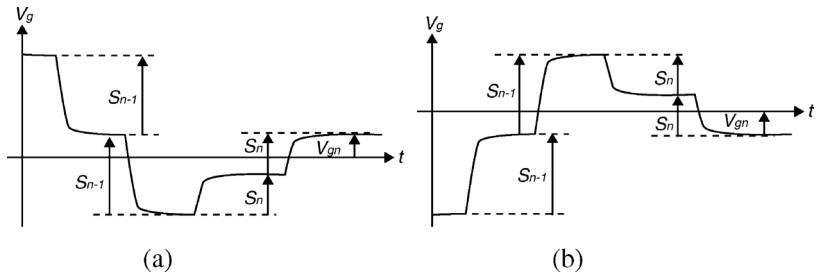


Fig. 2. V_g around the end of integration. (a) $S_n > 0$, (b) $S_n < 0$.

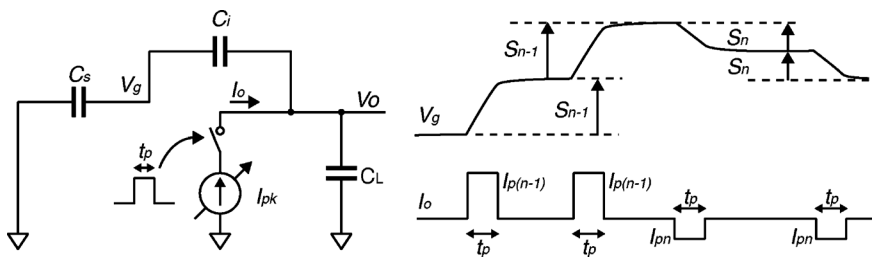


Fig. 3. V_g step sizes.

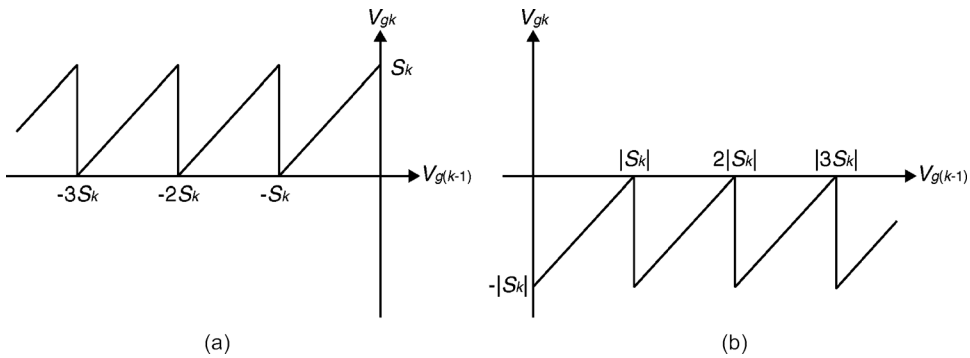


Fig. 4. Relationship between V_g values before and after kth V_g staircase. (a) $S_k > 0$, (b) $S_k < 0$.

II. Settling Behavior of the Dynamic Comparator-Based OTA

The proposed dynamic comparator-based OTA illustrated in Fig. 1(c) transfers charge between the sampling capacitor (C_s) and integrating capacitor (C_i) while driving the output load (C_L). The polarity of V_g determines the polarity of the current pulse injected to the output so that V_g moves toward zero. The initial current pulse amplitude of each integration is large in order to quickly move V_g toward zero. However, the resulting overshoot is also large, so the pulse amplitude is decremented each time the polarity of V_g changes (i.e., after each zero crossing). Accurate final settling is guaranteed by using very small final current pulse amplitude. Once a V_g sign change at the final current amplitude setting is detected, the integration is complete and the iterations above cease.

The residual value of V_g at the end of an integration phase (V_{gn} for an n-staircase dynamic comparator-based OTA) corresponds to the input-referred error for a single-input integrator like the one in Fig. 1. This can be seen recognizing that in each phase, $(C_s/C_i)(V_i + V_{gn})$ is integrated onto the output. Hence, the output is the same as would be obtained from an ideal integrator with input[2] $V_i + V_{gn}$. Therefore, in order to evaluate the impact of the settling error, we study the statistics of V_{gn}. As shown in Fig. 2, the value of V_{gn} falls within two possible ranges depending on the sign of the final V_g staircase,

$$\begin{aligned} 0 < V_{gn} < S_n \quad & (S_n > 0) \\ S_n < V_{gn} < 0 \quad & (S_n < 0) \end{aligned} \tag{2}$$

where S_n is the step size of the final (nth) V_g staircase. Current pulses applied at the output create steps in V_g as shown in Fig. 3, and the step size of the kth staircase can be expressed as

$$S_k = \frac{I_{pk} t_p}{C_{\text{eff}}}, \tag{3}$$

where I_{pk} is the current pulse amplitude of the kth staircase, t_p is the pulse width, and $C_{\text{eff}} \equiv C_s(1 + C_L/C_i) + C_L$. The initial value of k at the beginning of an integration phase is 1, and it ends with n for an n-staircase dynamic comparator-based OTA.

[2]For an integrator with multiple input branches, V_{gn} is referred to any input by scaling it by a factor of larger than one depending on the capacitor ratio of the sampling capacitors.

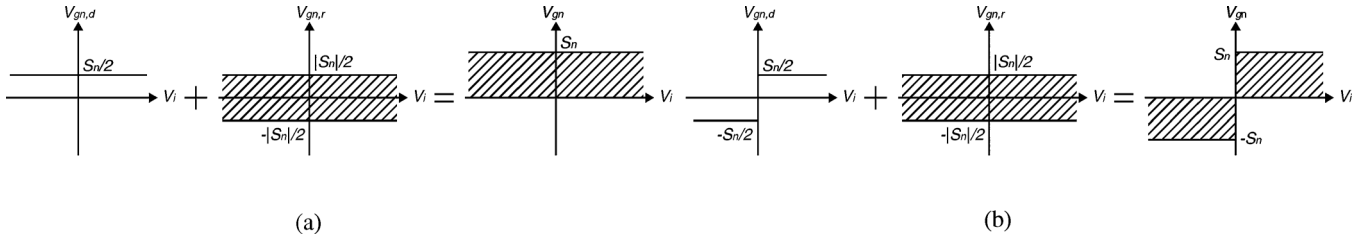


Fig. 5. Statistics of V_{gn}. (a) With output precharge. (b) Without output precharge.

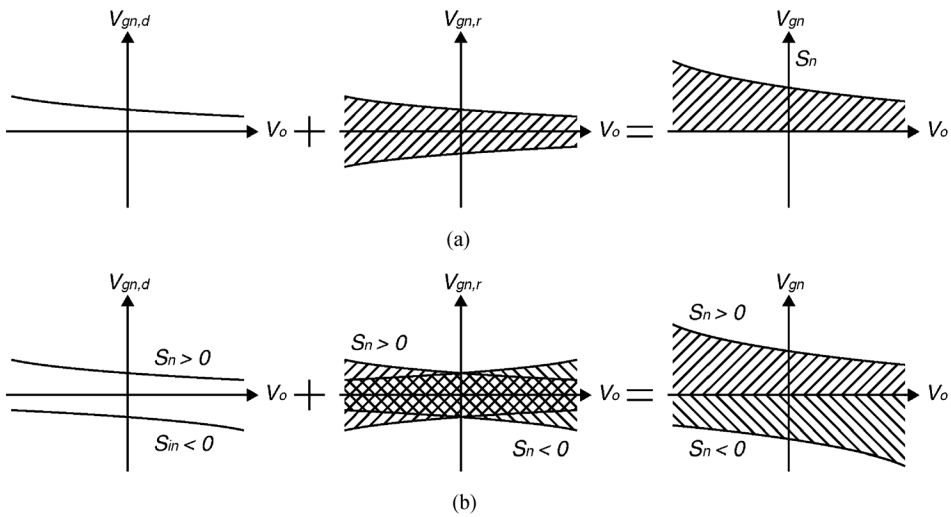


Fig. 6. Statistics of V_{gn} with a nonlinear current pulse driver. (a) With output precharge. (b) Without output precharge.

It can be assumed that V_{gn} is uniformly and pseudo-randomly distributed over each range in (2) because of the quantized V_g step. Fig. 4 shows the relationship between V_g values before $(V_{g(k-1)})$ and after (V_{gk}) a kth stair case. It resembles the relationship between the quantization error and input of an ADC. The quantization error of an ADC is often assumed a pseudo random process uniformly distributed over 1 LSB range for a busy enough input [10]. It should be noted that the relationship shown in Fig. 4 is nested n times for an n-staircase dynamic comparator-based OTA. This makes the statistics of V_{gn} further scrambled.

In this section, the statistics of V_{gn} is first discussed assuming ideal current sources with infinite output resistance for the current pulse driver, so I_{pk} and thus S_n are independent of V_o, and then the nonlinear signal dependence of S_n is taken into account.

A. Settling Behavior With Signal Independent Current Pulses

In order to analyze the statistics of V_{gn} quantitatively, we consider integrators with and without output precharge separately as they exhibit different V_{gn} statistics. Output precharging, which is used by all ZCBC implementations reported in the literature, forces the polarity of V_g to be the same at the start of every integration phase (V_{g0} in Fig. 1) by precharging the output to either a very high or low voltage so the ZCD always sees V_g ramping in the same direction. This is particularly important for unidirectional ZCDs [1], [6] which only work for one ramp polarity and asymmetrical ZCDs [5] which have unequal delays for positive and negative ramps. Even for symmetrical ZCDs, device and layout mismatch can introduce some asymmetry causing a small signal-dependent error.

The proposed OTA, however, does not use output precharging because it uses a symmetrical comparator, and the comparator delay does not affect the amount of overshoot on V_g. There is still a signal-dependent component in the settling error due to the absence of output precharge as explained later in this section, but it can be made less than the thermal noise level of the comparator without incurring a significant power penalty. Nevertheless, the settling behavior of both cases (with and without output precharge) are studied in this section for completeness and future reference.

1) With Output Precharge: If the integrator output is precharged at the beginning of each integration phase such that the initial V_g sign is constant, then the sign of S_n is also constant because

$$\mathrm{sgn}(S_n) = (-1)^n \cdot \mathrm{sgn}(V_{g0}) \tag{4}$$

Therefore, V_{gn} in this case is uniformly distributed within $\pm S_n/2$ around $S_n/2$ as shown in Fig. 5(a). By decomposing V_{gn} into the deterministic $(V_{gn,d})$ and random components $(V_{gn,r})$, this can be expressed as

$$V_{gn} = V_{gn,d} + V_{gn,r}, \tag{5}$$

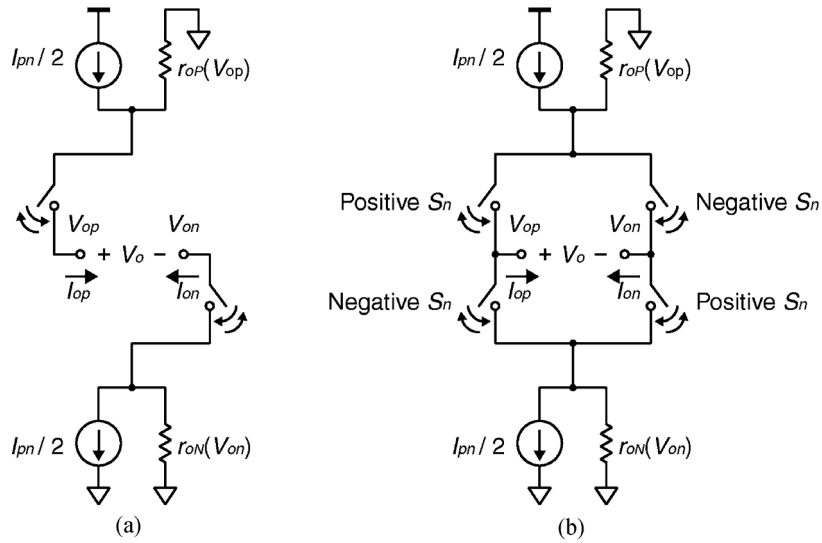


Fig. 7. Current pulse driver with finite nonlinear output resistance. (a) With output precharge, (b) Without output precharge.

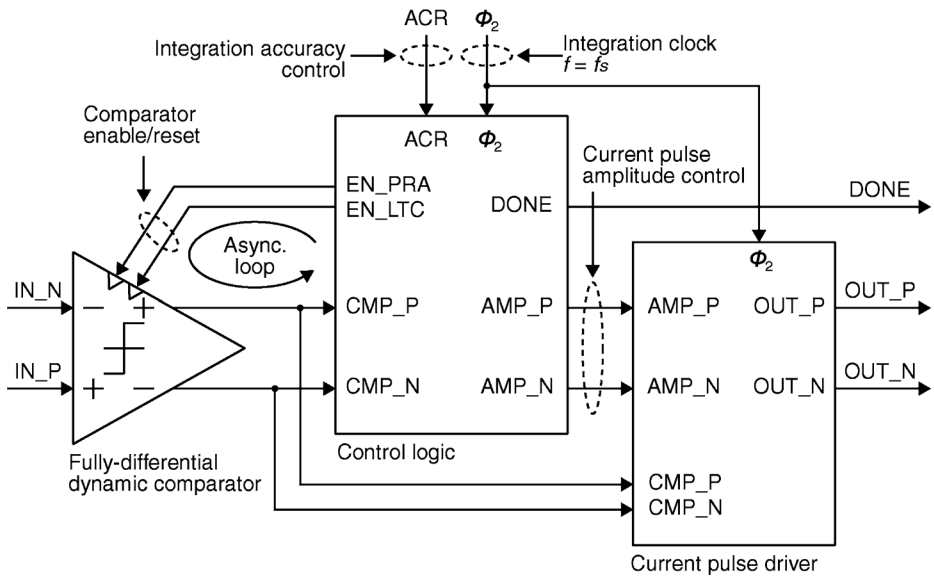


Fig. 8. A block diagram of the proposed dynamic comparator-based OTA.

where

$$V_{gn,d} = \frac{S_n}{2} = (-1)^n \cdot \mathrm{sgn}(V_{g0}) \cdot \frac{|S_n|}{2} \tag{6}$$

and

$$\overline{V_{gn,r}^2} = \frac{S_n^2}{12 \cdot \mathrm{OSR}}, \tag{7}$$

where OSR is the oversampling ratio. Since $\mathrm{sgn}(V_{g0})$ is constant with output precharge, $V_{gn,d}$ only has a DC component.

2) Without Output Precharge: The initial value of V_g depends on the sign of the input (V_i) without output precharge because

$$V_{g0} = -\frac{C_s}{C_s + C_i C_L/(C_i + C_L)} V_i. \tag{8}$$

It should be noted that (8) is independent of V_o. Expressions (6) and (7) still apply, but the sign of S_n is not constant but depends on V_i in this case as

$$\mathrm{sgn}(S_n) = (-1)^n \cdot \mathrm{sgn}(-V_i) \tag{9}$$

Therefore,

$$V_{gn,d} = (-1)^n \cdot \mathrm{sgn}(-V_i) \cdot \frac{|S_n|}{2} \tag{10}$$

and

$$\overline{V_{gn,r}^2} = \frac{S_n^2}{12 \cdot \mathrm{OSR}} \tag{11}$$

as illustrated in Fig. 5(b). Since $\mathrm{sgn}(\,)$ is an odd symmetric nonlinear function, $V_{gn,d}$ contains odd-order harmonics of V_i. The random component remains the same as (7) since its variance is independent of the sign of S_n.

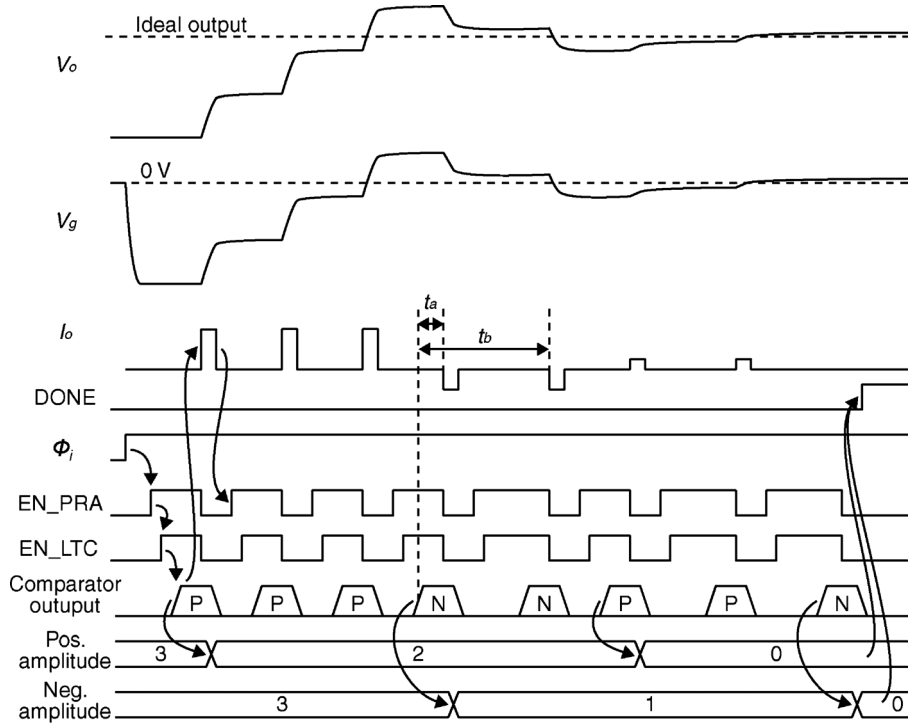


Fig. 9. A timing diagram of the proposed dynamic comparator-based OTA.

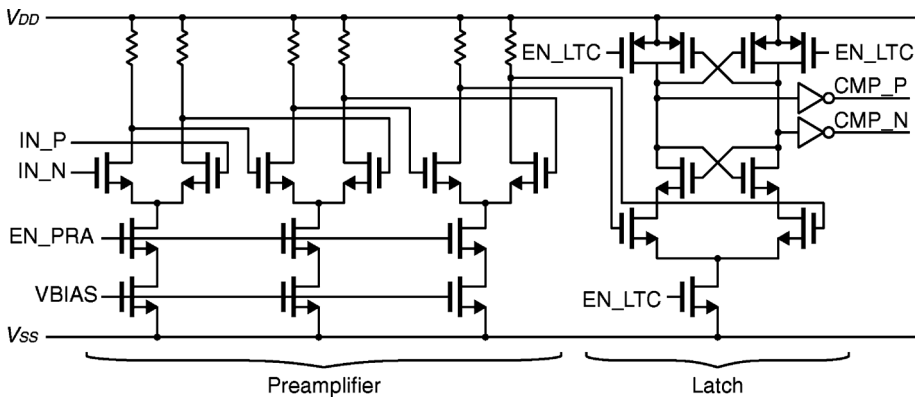


Fig. 10. Dynamic comparator schematic.

The difference in V_{gn} statistics with and without output precharge is in its deterministic component, $V_{gn,d}$. With output precharge, $V_{gn,d}$ only has a DC component whereas it has nonlinear components of V_i without output precharge. The former is obviously a more desirable settling behavior. Though the settling error without output precharge has nonlinear signal dependent components, it is still bounded within $\pm S_n$ as shown in Fig. 5. In addition, The value of S_n can be reduced using many different current pulse amplitudes and a small final step size S_n. Doing so does not require any significant increase in power, whereas decreasing the thermal noise of the comparator does increase power consumption. Hence, the settling error of an efficiently-designed stage will be dominated by the comparator's thermal noise, in which case the distortion caused by the nonlinearity will be well below the noise level. For these reasons, output precharging is not used in the proposed OTA.

B. Settling Behavior With Signal Dependent Current Pulses

The nonlinear output resistance of the current sources in the current pulse driver makes S_n a function of the output voltage (V_o). This causes the V_g distribution to be modulated by V_o as shown in Fig. 6. The variance of the $V_{gn,r}$ is now a function of V_o, but it still remains white. The deterministic component $V_{gn,d}$ with and without output precharge is described below.

1) With Output Precharge: With output precharge, the deterministic component of V_{gn} can be expressed by

$$V_{gn,d}(V_o) = \frac{I_{pn}(V_o)t_p}{2C_{\text{eff}}} \tag{12}$$

$$= \frac{t_p}{C_{\text{eff}}} \sum_{k=0}^{\infty} a_k V_o^k. \tag{13}$$

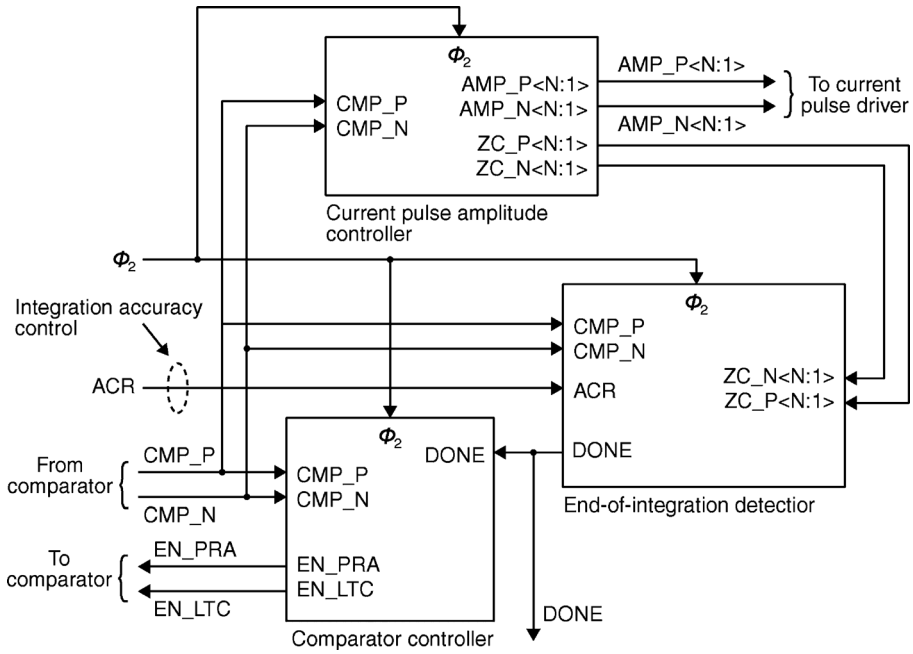


Fig. 11. Control logic of the OTA.

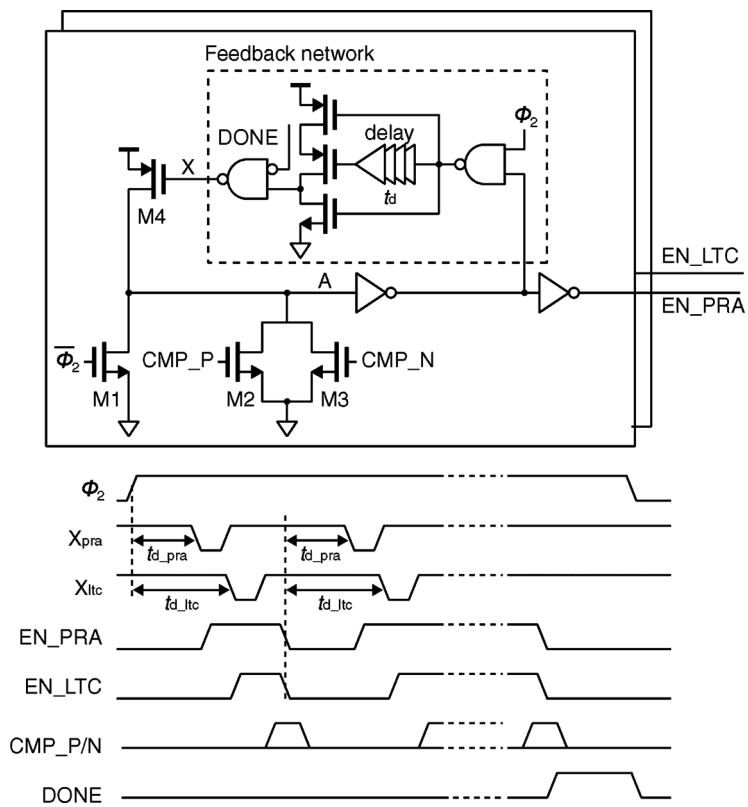


Fig. 12. Comparator control logic.

If we consider the current pulse driver shown in Fig. 7(a),

$$a_0 = \frac{I_{pn}(0)}{2} \tag{14}$$

$$a_1 = \frac{V_o}{r_o(0)} \tag{15}$$

TABLE I
A STATE DIAGRAM OF THE kTH ZERO-CROSSING DETECTION CELL

ZC_P<k>	ZC_N<k>	k-th staircase state	Action at state transition
0	0	Not started	-
0	1	Active ($V_g > 0$)	Decrement AMP_P
1	0	Active ($V_g < 0$)	Decrement AMP_N
1	1	Done	-

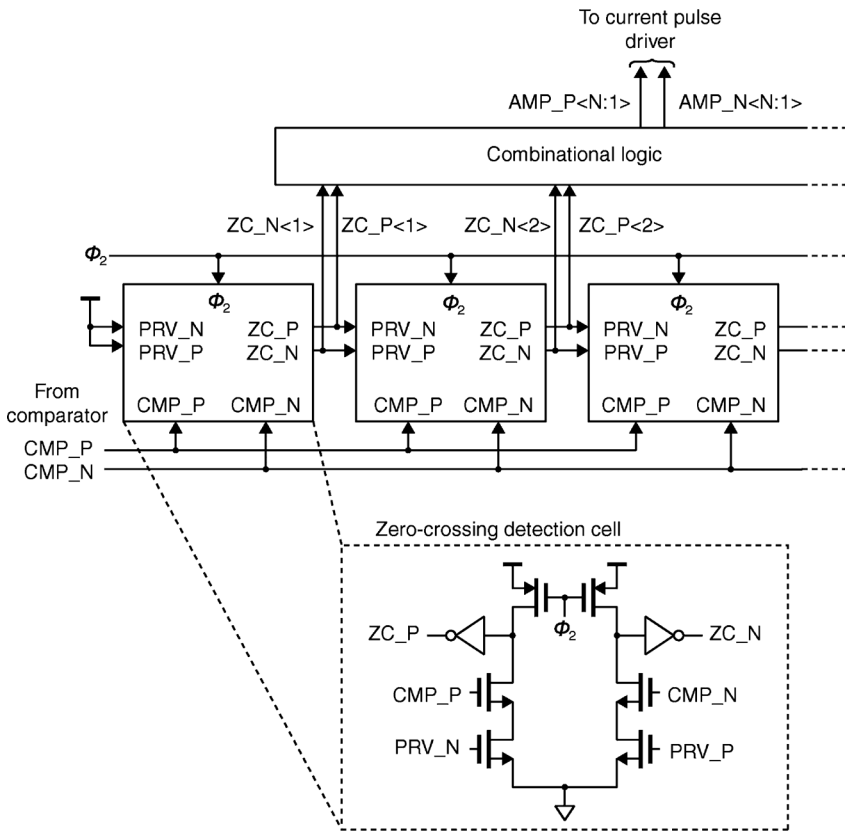


Fig. 13. Current pulse amplitude controller.

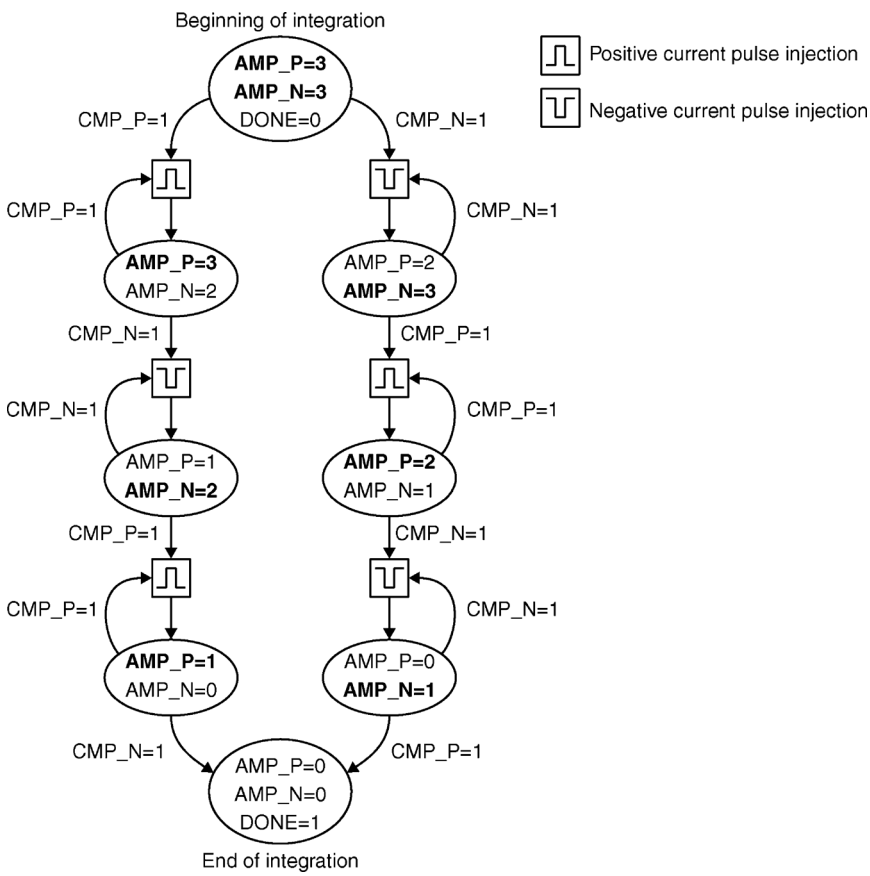


Fig. 14. State diagram of the current pulse amplitude controller.

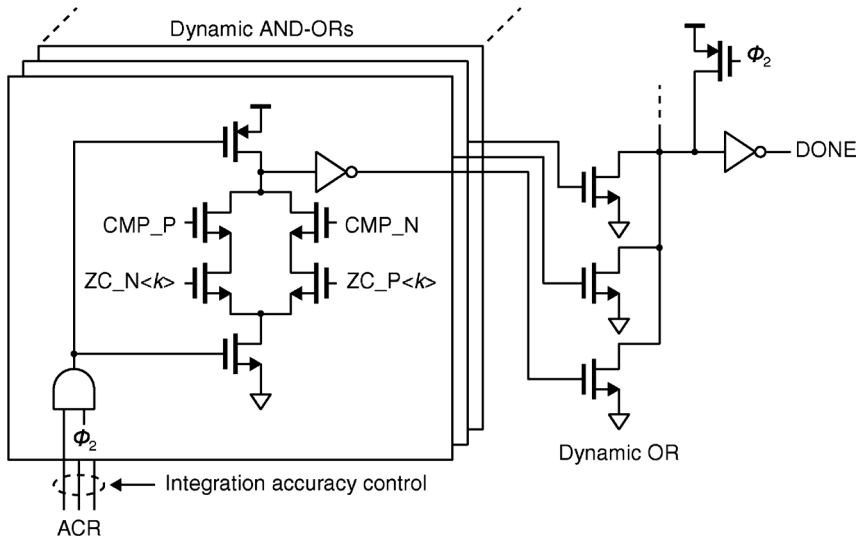


Fig. 15. End-of-integration detector.

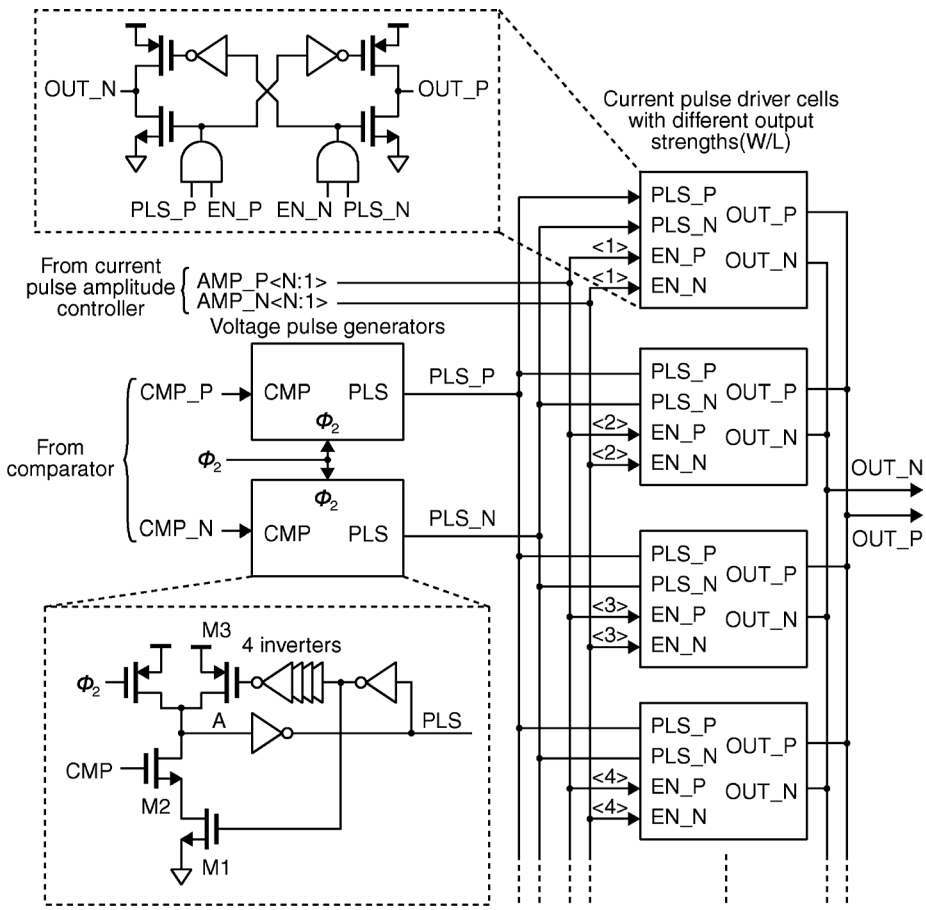


Fig. 16. Current pulse driver with amplitude control.

where $r_o(V_o) \equiv r_{oP}(V_o)+r_{oN}(V_o)$ is the nonlinear differential output resistance. The rest of the components $(a_2, a_3, \ldots)$ are due to the signal dependent components of the current source output resistance. Ignoring the signal dependent resistance results in a first-order approximation (so $a_2, a_3, \ldots = 0$),

$$V_{gn,d}(V_o) = \frac{t_p I_{pn}(0)}{2C_{\text{eff}}} - \frac{t_p}{r_o(0)C_{\text{eff}}}V_o \tag{16}$$

which is analogous to a conventional OTA having a DC offset of $t_p I_{pn}(0)/2C_{\text{eff}}$ and a DC gain of $t_p/r_o(0)C_{\text{eff}}$ because $V_{gn,d}(V_o) = V_{os} - V_o/A_0$ for a conventional OTA with an offset of V_{os} and a gain of A_0.

2) Without Output Precharge: Without output precharge V_{gn} can step up or down depending on the sign of V_i. Therefore, the current pulse driver is capable of sinking and sourcing

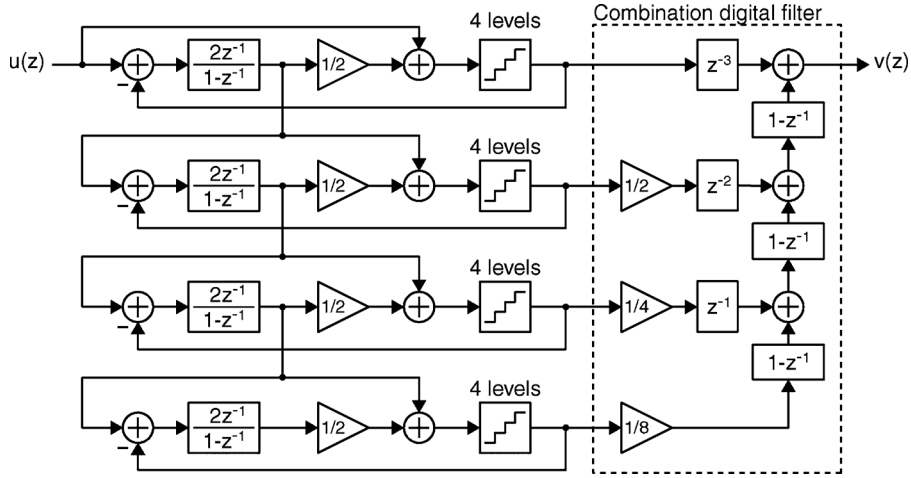


Fig. 17. A 1-1-1-1 MASH delta-sigma modulator block diagram.

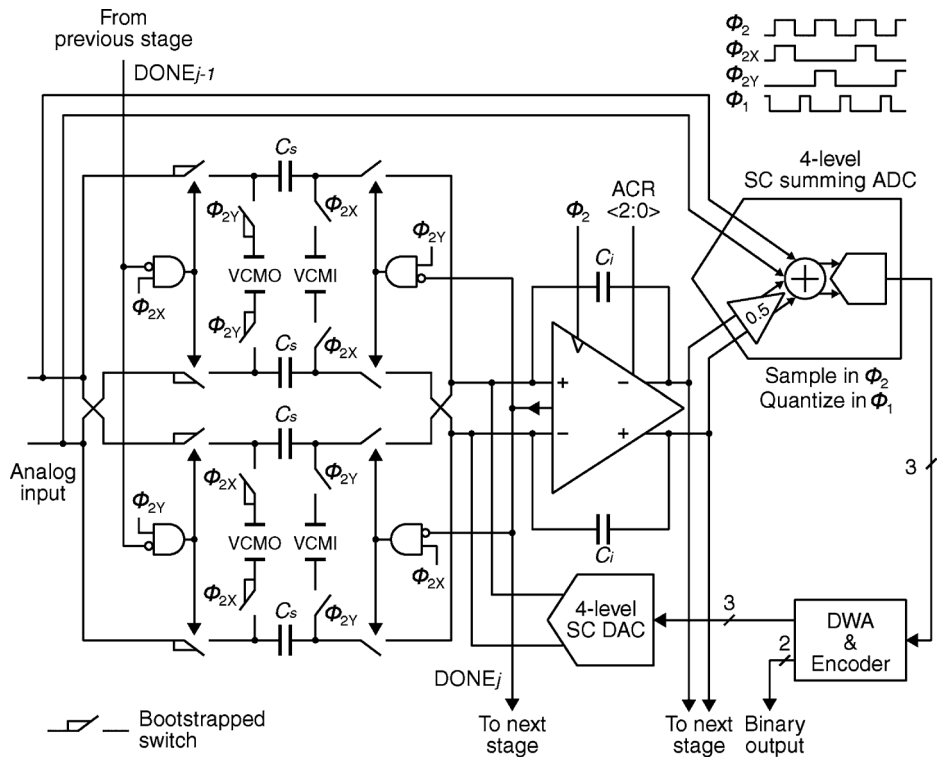


Fig. 18. SC implementation of one first-order modulator stage.

differential currents as shown in Fig. 7(b). In this case, the deterministic component of V_{gn} can be expressed as

$$V_{gn,d}(V_o) = \begin{cases} \dfrac{t_p}{C_{\text{eff}}} \displaystyle\sum_{k=0}^{\infty} a_k V_o^k & (S_n > 0) \\ -\dfrac{t_p}{C_{\text{eff}}} \displaystyle\sum_{k=0}^{\infty} a_k (-V_o)^k & (S_n < 0) \end{cases} \tag{17}$$

$$= \frac{t_p}{C_{\text{eff}}} \sum_{k=0}^{\infty} a_{2k+1} V_o^{2k+1} + (-1)^n \cdot \text{sgn}(-V_i) \sum_{k=0}^{\infty} a_{2k} V_o^{2k}. \tag{18}$$

which shows the same odd-order signal dependence as the case with output precharge but the even-order distortion and DC offset are modulated by the sign of V_i.

Again, if the stage is designed efficiently, the thermal noise of the comparator will dominate the settling error and S_n is made small, so the signal dependence of S_n is not a major concern. The same argument applies any modulation of t_p caused, for example by poor supply rejection of the digital circuits. Modulation of t_p causes a time-varying envelope of the V_{gn} statistics shown in Fig. 6, but in a properly designed circuit, the effect is masked by comparator noise.

C. Thermal Noise

The thermal noise contribution of the switches during a sampling phase is same as that of conventional switched-capacitor

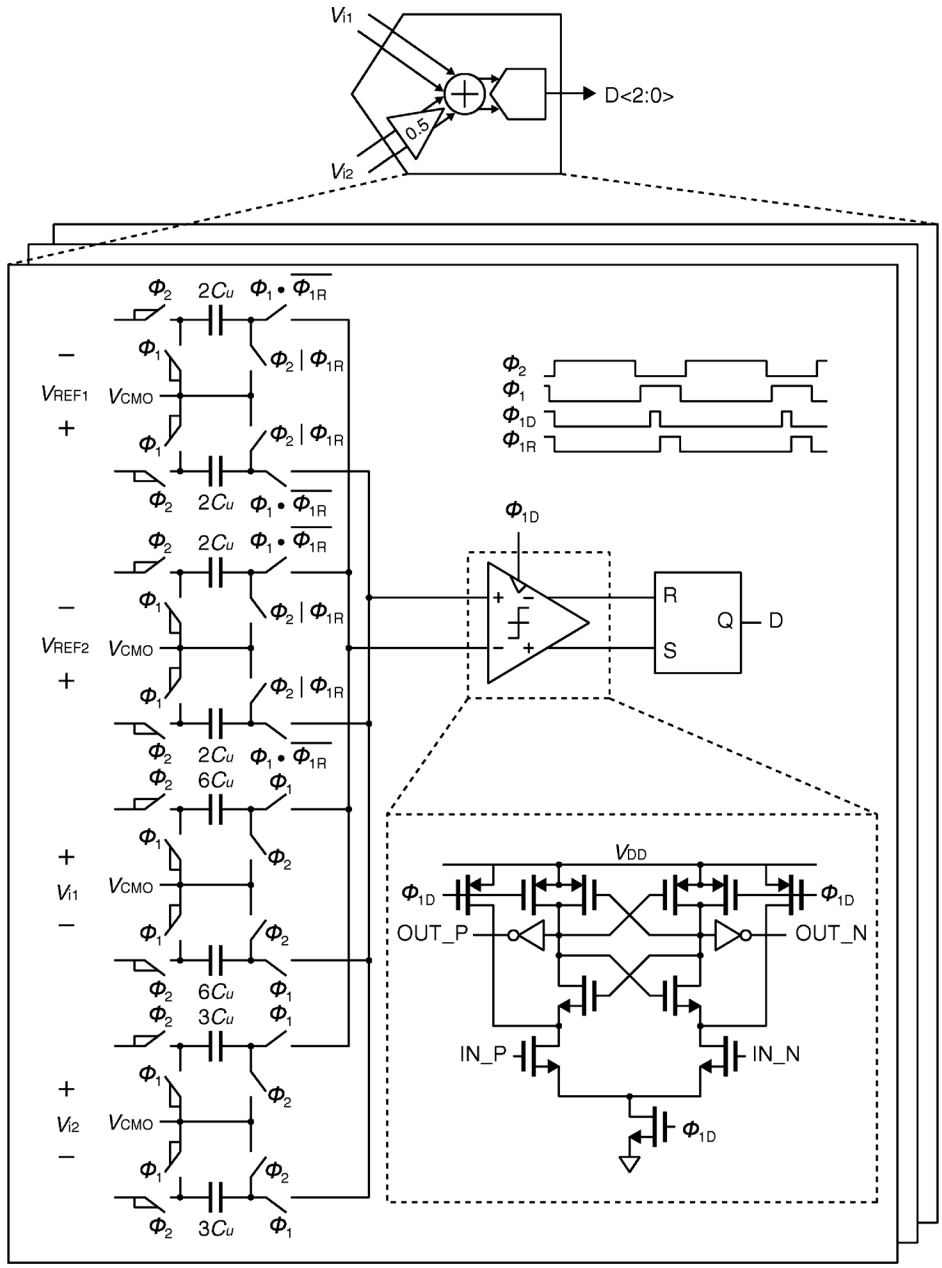


Fig. 19. A block diagram of the summing ADC.

integrator [11]. In an integration phase, the thermal noise of the comparator as well as that of the switches causes the comparator to make a wrong decision with respect to the voltage across C_s contributing additional settling error to that described above. Analysis of the thermal noise in an integration phase is very cumbersome because it involves nested stochastic analysis due to many zero crossings of V_g. System-level simulations with all thermal noise referred to the input of the comparator can be easily done to determine the acceptable input-referred noise of the comparator.

III. Circuit Design of the Dynamic Comparator-Based OTA

The proposed dynamic comparator-based OTA consists of three major components as shown in the block diagram in Fig. 8. The fully-differential dynamic comparator evaluates the sign of its input (V_g) when enabled by the control logic. The current pulse driver injects either a positive or negative pulse to the OTA output when triggered by one of the complementary comparator outputs. The control logic enables and resets comparator, and also controls the current pulse amplitude of the current pulse driver. A timing diagram of the proposed OTA with only three V_g staircases for simplicity is shown in Fig. 9.

In this section, circuit design of each block is described in detail.

A. Dynamic Comparator

The dynamic comparator used in this work consists of a three-stage preamplifier followed by a dynamic latch as shown in Fig. 10. The preamp has roughly 30 dB of DC gain with

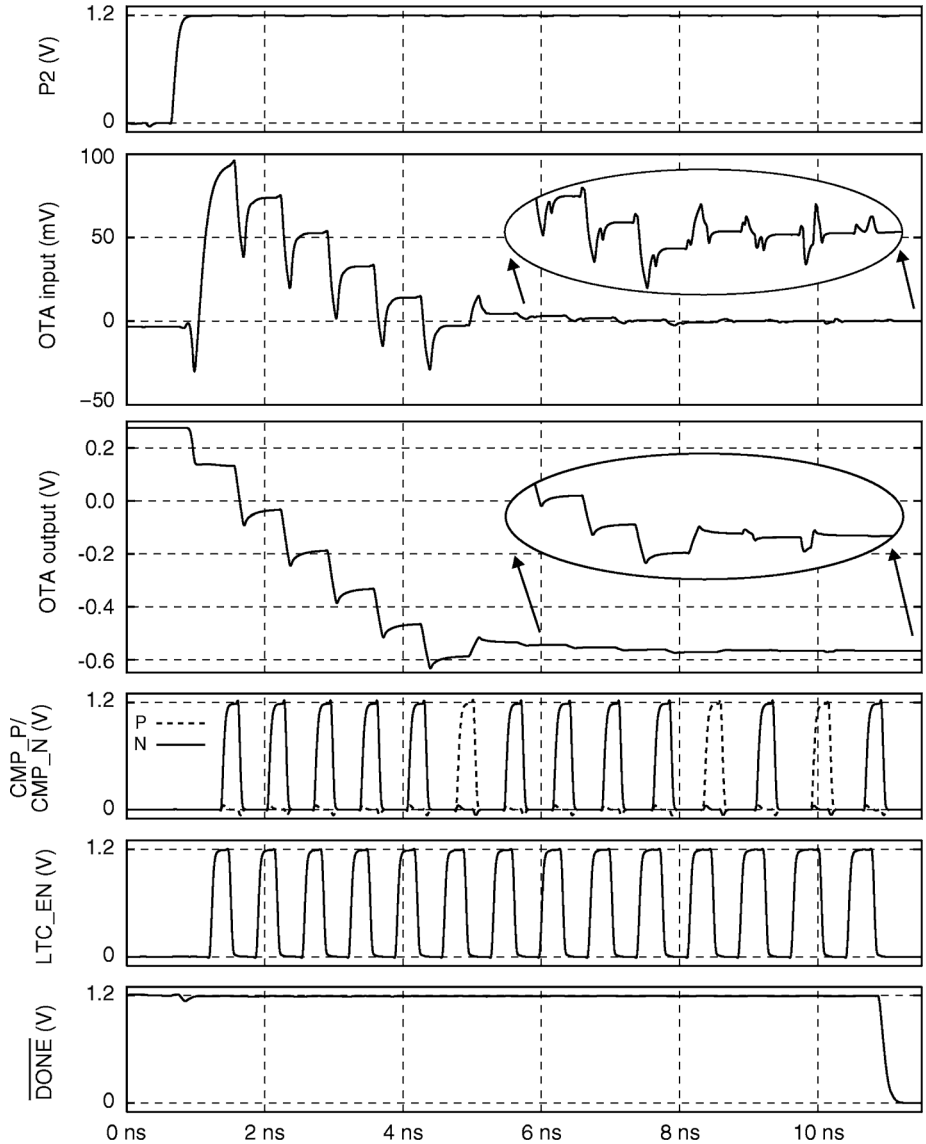


Fig. 20. OTA settling behavior from a post-layout simulation.

1.3-GHz bandwidth. Though the preamp has a large gain with three stages in this implementation, a low-gain single-stage preamp followed by a larger (lower-noise) latch could be used instead. The preamplifier is enabled and disabled by the EN_PRA signal. When EN_PRA is low, the NMOS transistors above the tail current sources cut off the bias currents and the output nodes of the preamplifier stages are reset to VDD by the load resistors. The latch is enabled when the signal EN_LTC is high and is reset during the other phase.

Each comparison starts with enabling the preamp followed by latch enable with a delay of about 120 ps to allow the preamp to wake up and settle before the latch is enabled.

Each time EN_PRA toggles, some charge is injected to the drain and source terminals of the tail-current switch. Part of the charge injected to the drain side splits unequally to the gates of the input differential pair via its gate capacitors because of the imbalance in the differential pair caused by its differential input, V_g. However, the net charge injected to the differential pair input converges to zero with settling because V_g is very close to zero before and after integration due to the settling of V_g to zero in the previous and current integration phases, respectively. Therefore, despite some charge transfer via the gates of the input differential pair during settling, the charge injection via the tail-current switch does not affect the settling accuracy of the integrator.

B. Control Logic

The control logic of Fig. 11 controls the comparator and the current pulse amplitude. It consists of an asynchronous comparator controller, current pulse amplitude controller, and end-of-integration detector as shown in Fig. 11. At the beginning of an integration phase, the comparator controller enables the comparator. Once one of the complementary comparator outputs goes high, the controller disables the comparator immediately by lowering both EN_PRA and EN_LTC for power saving and resetting. The current pulse driver, also triggered by the comparator output, injects a current pulse in the meantime. After the current pulse injection is complete, the comparator is

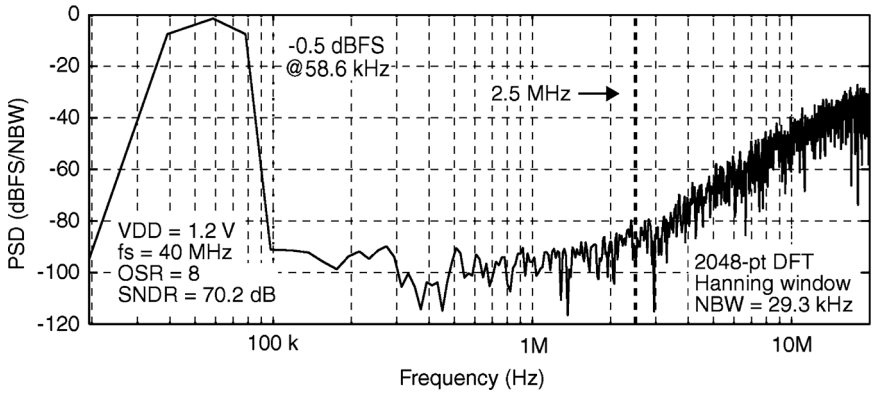


Fig. 21. Modulator output spectrum from a post-layout transient-noise simulation.

enabled again and the operation above repeats unless the DONE signal is high. The current pulse amplitude controller decreases the pulse amplitude each time the sign of the comparator output changes. Finally, the end-of-integration detector asserts the DONE signal once a sign change of the comparator output is detected and the current pulse amplitude is at its minimum as specified by the accuracy control signal (ACR).

The asynchronous control described above allocates just enough time for the comparator to make a decision so the integration time is fully utilized for accurate settling. In addition, it avoids explicit high-speed clock generation and routing over long distance which would result in a large power consumption penalty. This asynchronous operation is similar to that of a SAR ADC with asynchronous control [12]. Details of each block are described below.

1) Asynchronous Comparator Controller: The asynchronous comparator controller, once triggered by the integration clock (Φ_2), keeps enabling and disabling the comparator by asynchronously toggling EN_PRA and EN_LTC signals until a DONE signal is asserted by the end-of-integration detector. A simplified schematic of the asynchronous comparator controller and its timing diagram are shown in Fig. 12. The controller consists of two identical circuits with different delay in the feedback network as shown in Fig. 12. The delay difference corresponds to the time window between the rising edges of EN_PRA and EN_LTC.

While Φ_2 is low, node A of the comparator controller is pulled down by M1 so the comparator remains disabled ($\mathrm{EN\_PRA} = \mathrm{EN\_LTC} = 0$). Once Φ_2 goes high, after the delay ($t_{d\_\mathrm{pra}} \approx 300$ ps and $t_{d\_\mathrm{ltc}} \approx 420$ ps) in the feedback, M4 pulls node A high enabling the comparator. The comparator remains enabled until it makes a decision when either CMP_P or CMP_N goes high. Then either M2 or M3 pulls node A so the comparator is disabled immediately and they are enabled again after the delay through the feedback network unless the DONE signal is asserted. Once the DONE signal is asserted, node X is held high so node A can no longer be pulled high and the comparator is not enabled again until the next integration phase.

2) Current Pulse Amplitude Controller: The current pulse amplitude controller sets the current pulse amplitude to its maximum before the beginning of an integration phase, and updates the amplitude setting each time a zero crossing of V_g is detected in Φ_2.

A straightforward approach to controlling the current pulse amplitudes would be to simply decrement both the positive and negative current pulse amplitudes each time a V_g zero crossing is detected. However, with this approach, the amplitudes would have to be updated within a very short time window (t_a in Fig. 9) after V_g comparison but before the immediately following current pulse injection. This would impose a very challenging timing requirement on the amplitude controller, which is the most complicated component of the control logic.

However, since a V_g polarity change is always accompanied by a change in the polarity of the injected current pulse, the current pulse amplitude of the opposite sign is pre-decremented as shown in Fig. 9. This significantly extends the time window for amplitude update to t_b as shown in Fig. 9.

A block diagram of the current pulse amplitude controller is shown in Fig. 13. It consists of cascaded zero-crossing detection cells and combinational logic. Each zero-crossing detection cell is responsible for keeping track of the state of the corresponding V_g staircase. Before the beginning of the kth staircase, the outputs (ZC_P and ZC_N) of the kth zero-crossing detection cell are both low. Once the kth staircase starts, one of the outputs goes high depending on the sign of V_g, and when V_g crosses zero, the other output goes high. This is summarized in Table I. The output of the zero-crossing detection cells are fed to a combinational logic to generate positive and negative current pulse amplitude control signals (AMP_P and AMP_N). State transitions of the current pulse amplitude controller for the example in Fig. 9 is shown in Table II. The bold numbers in Table II are the amplitude settings used for current pulse injection. It should be noted that each time the comparator output changes, the outputs of the zero-crossing detection cells change, so the current pulse amplitude settings are updated via the combinational logic shown in Fig. 13. The updated current pulse amplitude is not immediately used for current pulse injection as shown in Table II. This is why the timing requirement of the current pulse amplitude control logic is relaxed in this scheme. The state transitions example in Table II walks through the left-side path of the state diagram shown in Fig. 14 because the first comparator output is positive. The bold current pulse amplitude settings in Fig. 14 correspond to the bold numbers in Table II.

3) End-of-Integration Detector: The end-of-integration detector asserts a DONE signal once a sign change of V_g is de-

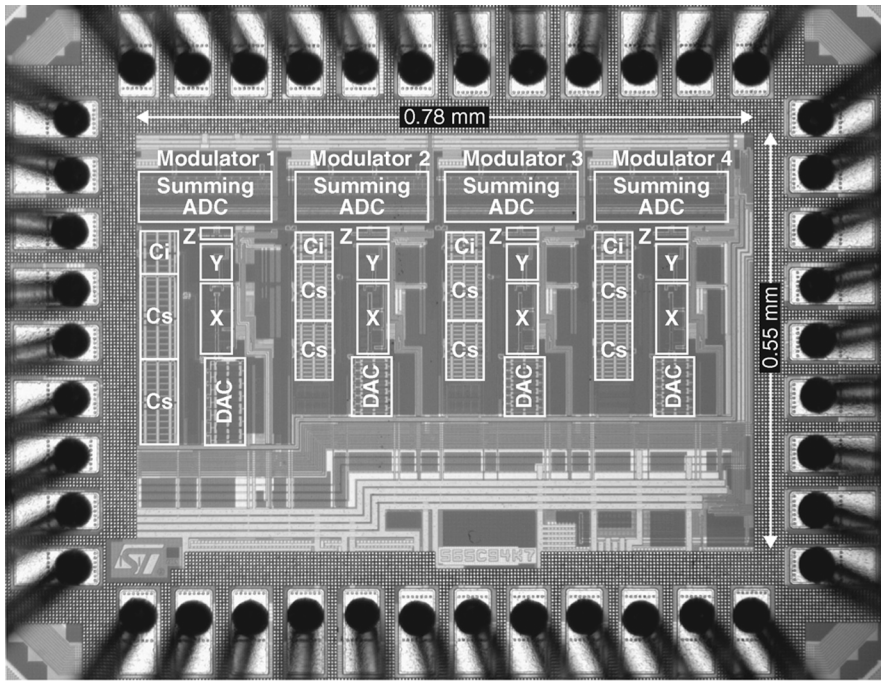


Fig. 22. A die photo of the implemented delta-sigma modulator.

TABLE II
STATE TRANSITIONS OF THE CURRENT PULSE AMPLITUDE CONTROLLER

Comparator out.	Initial	P	P	P	N	N	P	P	N
AMP_P	**3**	**3**	**3**	**3**	1	1	**1**	**1**	0
AMP_N	**3**	2	2	2	**2**	**2**	0	0	0
DONE	0	0	0	0	0	0	0	0	1
ZC_P<1>	0	1	1	1	1	1	1	1	1
ZC_N<1>	0	0	0	0	1	1	1	1	1
ZC_P<2>	0	0	0	0	0	0	1	1	1
ZC_N<2>	0	0	0	0	1	1	1	1	1
ZC_P<3>	0	0	0	0	0	0	1	1	1
ZC_N<3>	0	0	0	0	0	0	0	0	1

tected by the comparator at the current pulse amplitude setting specified by the integration accuracy control input (ACR). For example, if it is set to 2, an integration ceases after the second time V_g reverses its polarity. ACR is set to to the minimum current pulse amplitude when the maximum integration accuracy is desired. This accuracy control allows lower-power operation when lower accuracy is sufficient, for example in the second and later stages of a delta-sigma modulator. As shown in the schematic of the detector in Fig. 15, the ACR input enables one of the AND-OR cells. The selected cell detects a V_g zero crossing of the corresponding V_g staircase, and asserts a DONE signal through the dynamic OR gate.

C. Current Pulse Driver

The current pulse driver provides positive and negative differential current pulses of amplitudes specified by the control logic. A block diagram of the current pulse driver is shown in Fig. 16. One of the two voltage pulse generators triggered by the comparator output turns on one of the current driver cells, selected by the control logic for amplitude control, for a short period (about 100 ps).

When the comparator makes a decision, one of the complementary outputs (CMP_P or CMP_N) turns on transistor M2 of the corresponding voltage pulse generator. Node A, which is precharged to VDD, is discharged by M2 and M1 to the ground so the output goes high. After a delay through the feedback path realized by a chain of inverters, M3 is turned on so node A is precharged to VDD so the output goes down. The comparator is supposed to enter the reset phase where $\mathrm{CMP\_P} = \mathrm{CMP\_N} = 0$ before the node A pull up via M3 so the pull down by M2 and pull up by M3 should not fight. Even if the comparator reset is delayed, the transistor M1 disables the pull down network until some time after node A is pulled up by M3 so the pull-up and down contention will not occur.

Each current pulse driver cell has two pairs of NMOS and PMOS transistors. A voltage pulse at one of the inputs (PLS_P or PLS_N) turns on one of the pairs to provide either a positive or negative current pulse at the output. Different current amplitude settings are realized with different W/L ratios of the transistors in current pulse driver cells. The device sizes W/L of adjacent current driver cells are scaled by a factor of four.

Since the transistors in the current driver cells act as switches instead of constant current sources, the actual current pulse is actually signal-dependent. However, as explained in the previous section, the final V_g step size is made so small that the thermal noise of the comparator dominates the settling error. Therefore, this signal dependence is not of a concern. Because the output transistors operate in triode, the output common-mode is loosely set by the relative sizing of the PMOS and NMOS output transistors. In this work, they were sized to provide a mid-rail common mode, maximizing the available output swing.

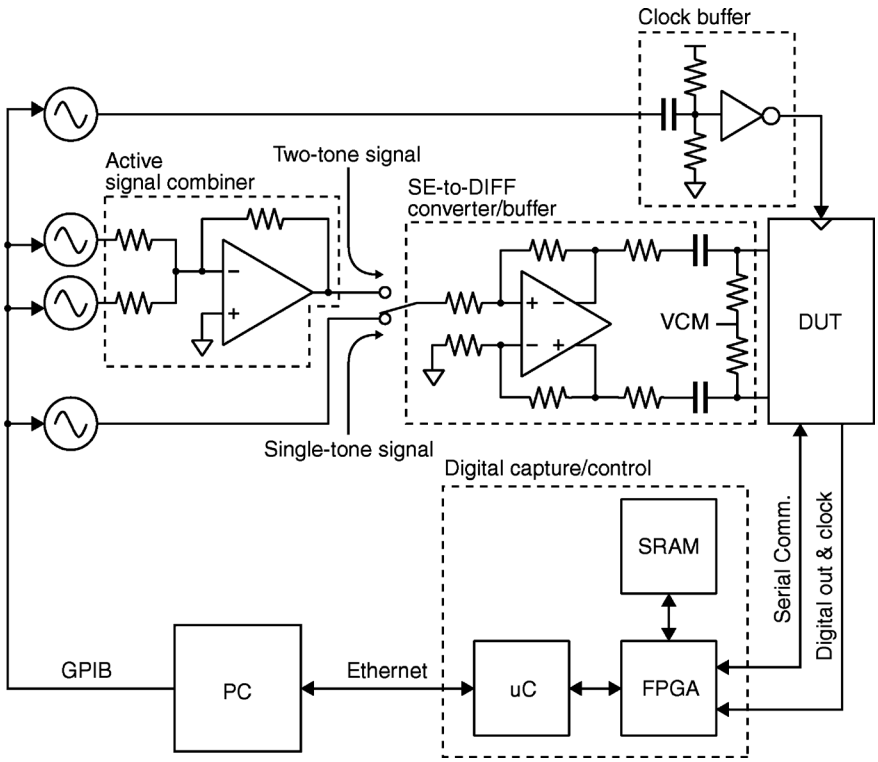


Fig. 23. Experiment setup.

IV. 1-1-1-1 Mash Delta-Sigma Modulator

SC integrators based on dynamic comparator-based OTAs were used in the 1-1-1-1 MASH delta-sigma modulator shown in Fig. 17. The modulator provides fourth-order noise shaping,

$$V(z) = U(z)z^{-3} + \frac{e_4(z)}{8}(1 - z^{-1})^4 \tag{19}$$

where e_4 is the quantization error of the quantizer in the last stage.

Fig. 18 shows a simplified schematic of one stage of the MASH modulator. The interleaved sampling technique proposed in [13] is used for all of the stages since it allows all of the integrators to sample and integrate in the same phase (Φ_2) in a 1-1-... MASH architecture. Therefore, the integrators can completely sleep in Φ_1, and thus the quantizers are the only components that operate in Φ_1.

This scheme allows clock phase Φ_2 (the integration and sampling phase) to be extended and the duration of Φ_1 reduced. For this work, the ratio of Φ_1 and Φ_2 was made 1:3 so Φ_2 is extended by 25%, thereby increasing the maximum sampling frequency by the same factor.

The values of C_s and C_i in the first stage are 1 pF and 0.5 pF, respectively, and they are halved for the rest of the stages. The second, third, and the last stage are identical.

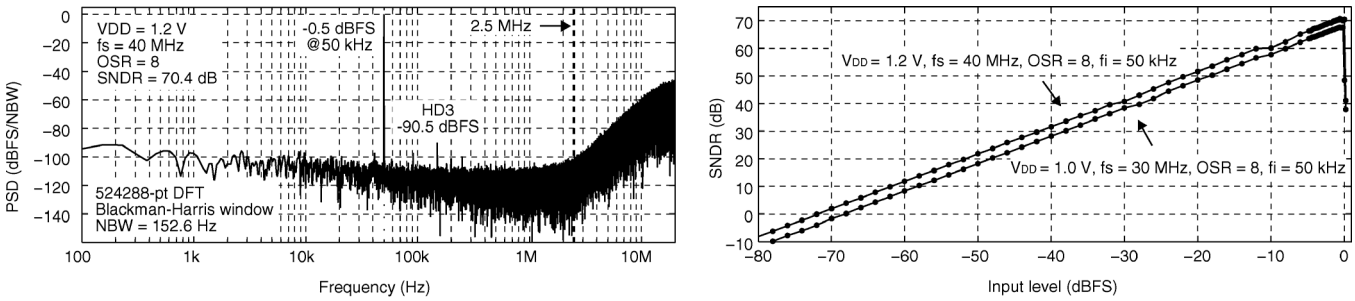
During Φ_2 but after the integration has settled, the integrating capacitor C_i is isolated from other capacitors to prevent unwanted charge transfer. The DONE signal generated by the control logic in each stage does this by opening all switches connected to C_i after integration is complete as shown in Fig. 18.

A. OTA

The dynamic comparator-based OTA described in the previous section is used for all of the stages. The OTAs perform integration during Φ_2 and sleep in Φ_1. The comparator of the OTA in the first modulator stage was designed for about 105-$\mu\mathrm{V}_{rms}$ input-referred noise, and the rest were the scaled by one-quarter to reduce their power consumption. They could have been scaled more aggressively further power saving but were kept the same to save the design time. Identical control logic is used for all of the OTAs. The OTAs' current pulse drivers are scaled by one-half for the last three stages compared with the first stage since C_s and C_i are also scaled by one-half. The number of V_g staircases was set 6, 3, 2, and 2 via the integration accuracy control (ACR) for the first to the last integrators, respectively as the first integrator needs the full accuracy while the later stages need less due to the interstage gain of two per modulator stage as well as the noise shaping.

B. Summing ADC

The summing ADC performs 4-level A-to-D conversions on the weighted sum of its two inputs, V_{i1} and V_{i2}. A block diagram of the ADC is shown in Fig. 19. It consists of sub blocks with weighted charge distributing switched capacitors followed by a comparator. The sub blocks realize comparison of the weighted sum of the inputs with different thresholds realized by different connections to the reference voltages. A schematic of the ADC sub block is shown in Fig. 19. In Φ_2, V_{i1}, V_{i2}, and the reference voltages are sampled onto the sampling capacitors. In Φ_1, all of the sampling capacitors are connected in parallel for charge



(a) (b)

Fig. 24. Measured output spectrum with a 50-kHz single-tone input (a) and SNDR versus the input level (b).

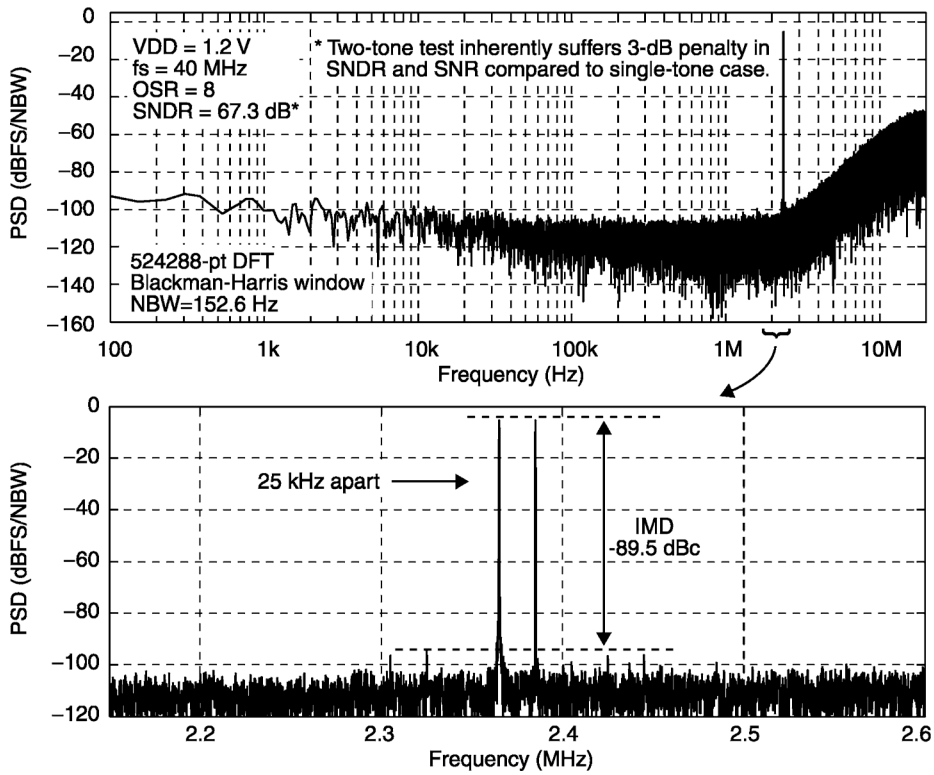


Fig. 25. Measured output spectrum with a 25-kHz apart two-tone input near the band edge.

redistribution so the input to the comparator is

$$V_c = \frac{6C_u}{13C_u + C_p}\left(V_{i1} + \frac{V_{i2}}{2} - \frac{V_{\mathrm{REF1}}}{3} - \frac{V_{\mathrm{REF2}}}{3}\right) \quad (20)$$

where V_{REF1} and V_{REF2} are either $+V_{\mathrm{REF}}$ or $-V_{\mathrm{REF}}$, C_u is 25 fF and C_p is the parasitic capacitance at the input of the comparator. The ADC has thresholds of $(2/3)V_{\mathrm{REF}}, 0$, and $-(2/3)V_{\mathrm{REF}}$ with respect to $V_{i1} + 0.5V_{i2}$.

The comparators are enabled by Φ_{1D} after the charge distribution. Following the comparator decisions, but before the end of Φ_1, all of the capacitors including the input parasitic capacitor of the comparator are reset so the input currents from the reference voltage sources for charging the sampling capacitors in Φ_2 are signal independent.

C. Simulation

Magnified plots showing the settling behavior of the OTA for a single integration cycle are in Fig. 20. Fig. 21 shows the output spectrum of the modulator. An SNDR of 70.2 dB was observed at $f_s = 40$ MHz, OSR $= 8$, and VDD $= 1.2$ V.

All the simulation results above were obtained from post-layout simulations with RC extraction, and Fig. 21 also includes thermal noise.

V. Experimental Results

The prototype delta-sigma modulator was implemented in a 65-nm 1P7M LP CMOS technology with standard-V_T devices only. A die photo of the fabricated prototype is shown in Fig. 22. The modulator core occupies 0.43 mm^2 of the silicon area. The measured peak SNDR is 70.4 dB and the power dissipation is

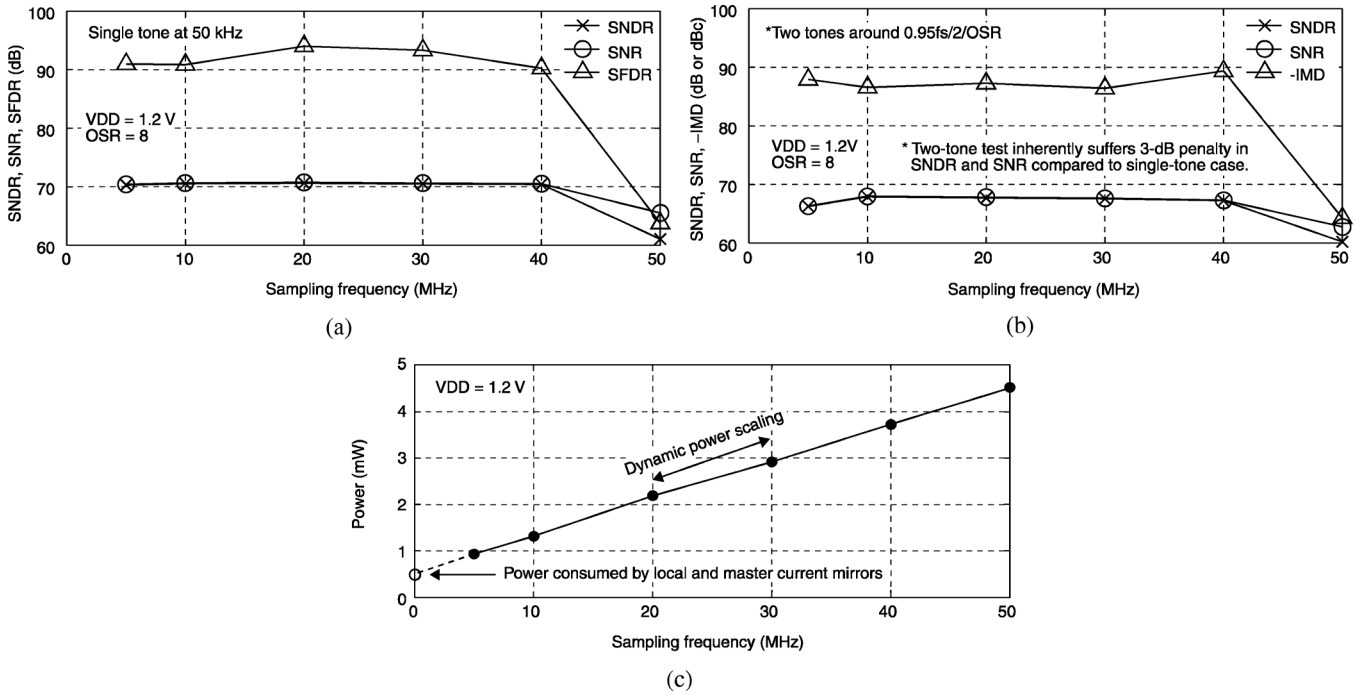


Fig. 26. Measured SNDR, SNR, SFDR for single-tone input (a), SNDR, SNR, and IMD for two-tone input (b), and power dissipation (c) versus the sampling frequency.

3.73 mW at VDD $=$ 1.2 V, $f_s = 40$ MHz, and OSR $= 8$ without any calibration.

Fig. 23 shows the test setup of the modulator. The input signal is either a single-tone signal or two-tone signal generated by active combination of two single tones. They are converted to a fully-differential signal by an off-chip fully differential amplifier. The modulator digital output is captured by an FPGA and stored in an SRAM. The stored data is slowly retrieved by a PC for spectral analysis.

Fig. 24(a) shows a measured spectrum with a 50-kHz single-tone input at -0.5 dBFS achieving the peak SNDR of 70.4 dB. The third order harmonic is the largest harmonic 90 dB below the input tone. Therefore, the SNDR is limited by the thermal noise. SNDR versus the input measured at VDD $=$ 1.2 and 1.0 V is plotted in Fig. 24(b). Since the OSR is relatively low, measurements were also performed with a two-tone input signal close to the edge of the bandwidth to demonstrate the performance of the modulator at high input frequencies. The output spectrum for one such measurement is shown in Fig. 25. An SNDR of 67.3 dB was observed with two -6.5 dBFS tones spaced 25 kHz apart just below $f_s/(2 \cdot \mathrm{OSR})$. The 3-dB degradation of the SNDR compared with the single-tone testing is inherent to the two-tone input. Therefore, no degradation of the performance was observed near the edge of the bandwidth. SNDR, SNR, and SFDR or IMD measured over f_s for low-frequency single-tone inputs and high-frequency two-tone inputs are shown in Fig. 26(a) and (b), respectively. The SNDR is almost constant as f_s is varied from 5 MHz to 40 MHz. Fig. 26(c) shows the power dissipation of the modulator versus f_s. As expected from the design, since most of the power consumption is dynamic, the power consumption scales linearly with f_s. The offset in the plot corresponds to the circuit's static bias current. A breakdown of the power dissipation at $f_s = 40$ MHz is shown in Table III.

TABLE III
BREAKDOWN OF THE POWER DISSIPATION

Supply	1.2 V	1.0 V
Sampling frequency	40 MHz	30 MHz
Comparators	1.42 mA	800 μA
Logic and current pulse drivers	960 μA	582 μA
Clock generator and buffer	444 μA	300 μA
Bootstrap switches	246 μA	150 μA
ADCs	46 μA	44 μA
Total	3.73 mW	1.88 mW

The measured results at both 1.2- and 1.0-V supply are summarized and compared with other work in Table IV. The modulator of this work outperforms all of the existing ZCBC-based delta-sigma modulators in SNDR, bandwidth, and FoM (both in J/conv-step and dB).

The FoM of 276 fJ/conv-step is worse than some continuous-time delta-sigma modulators with a similar bandwidth and resolution. However, unlike those works, the modulator in this work provides both f_s (or bandwidth) scalability and power scaling over f_s without requiring any circuit reconfiguration because of the discrete-time delta-sigma modulation and dynamic operation of the OTAs. In continuous-time delta-sigma modulators, f_s scalability requires RC time constant tuning. Power scalability over f_s requires bias current adjustment in both conventional discrete-time and continuous-time delta-sigma modulators. Both are difficult to achieve over a decade range of f_s as is shown here.

VI. CONCLUSION

System-level analysis and circuit design of the dynamic comparator-based OTA are shown. The 1-1-1-1 MASH delta-sigma modulator with dynamic comparator-based OTAs presented in this paper is faster (2.5-MHz bandwidth), more accurate

TABLE IV
COMPARISON OF THE EXPERIMENTAL RESULTS WITH OTHER WORK

	This work		[14]	[5]	[4]	[15]
Architecture	1-1-1-1 MASH		Multirate 2-1 MASH	Second order	Second order	Second order
Conventional OTA	No		Yes	No	No	No
CMOS technology	1P7M LP 65 nm		90 nm	LP 45 nm	0.18 μm	TFT 3 μm
Supply (V)	1.2	1.0	1.2	1.1	1.8	11.2
Sampling rate (MHz)	40	30	80/320	50	2.56	0.4
OSR	8		20/80	30	64	128
Bandwidth (MHz)	2.5	1.875	2.0	0.833	0.02	0.00156
Peak SNDR (dB)	70.4	67.5	65	47.7	65.3	65.6
Dynamic range (dB)	71.3	67.7	66	54.3	71	69
SFDR (dB)	90.0	91.3	79	-	-	-
Full-scale input (Vpp-diff)	2.0	1.6	1.6	1.2	-	-
Power (mW)	3.73	1.88	6.83	0.63	0.42	63.3
Area mm^2	0.43		0.076	0.0448	0.21	26
FoM (fJ/conv-step)[a]	276	259	1200	1907	6980	13030
FoM (dB)[b]	159	157	149	139	142	110

[a] FoM (fJ/conv-step)=Power / (2·Bandwidth·2^{ENOB})
[b] FoM (dB)= SNDR(dB) + 10·log10(Bandwidth / Power)

(SNDR = 70.4 dB), and more power efficient (FoM = 276 fJ/conv-step) than any other reported delta-sigma modulators based on ZCBC and CBSC.

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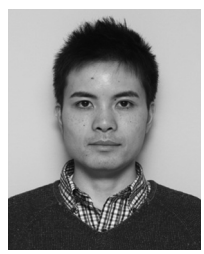

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