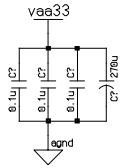
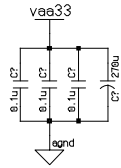


NTSC Video In/RGB Video Out

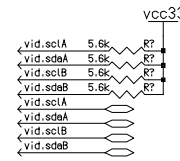
Video In A vcc bypass caps
One per vcc pin



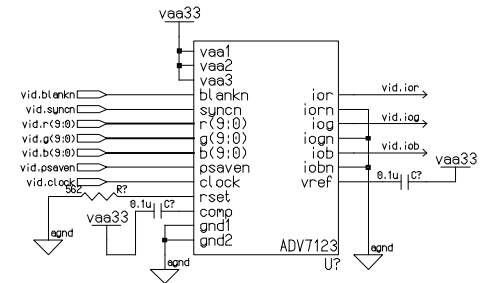
Video In B vcc bypass caps
One per vcc pin



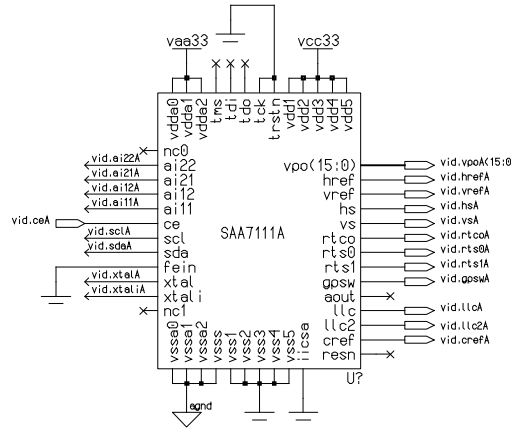
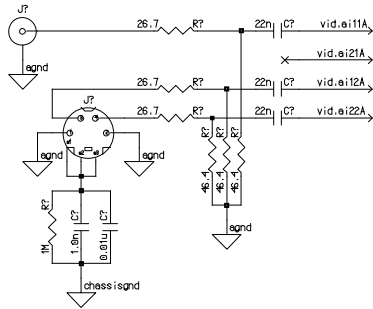
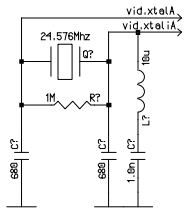
I2C Bus Pullups



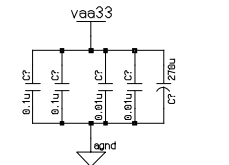
RGB Video Out
Inputs Require 3.3v TTL Signals



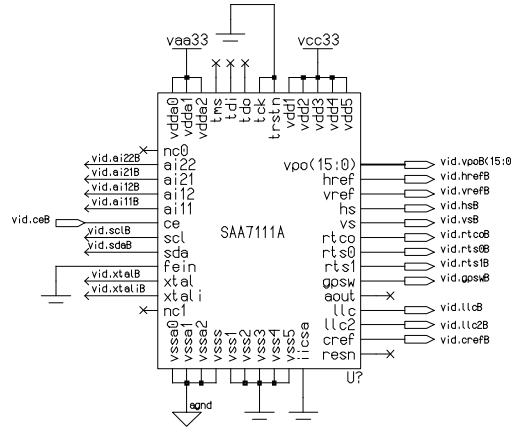
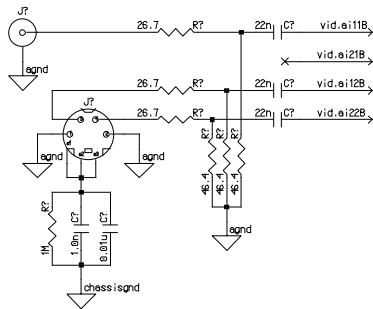
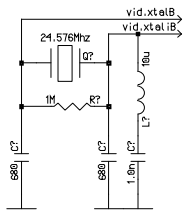
NTSC video decoder channel A



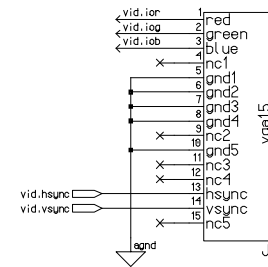
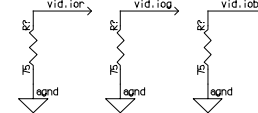
Place Bypass Cap At Each Vaa



NTSC video decoder channel B



Source Cable Termination

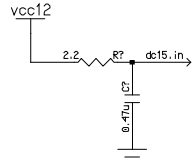


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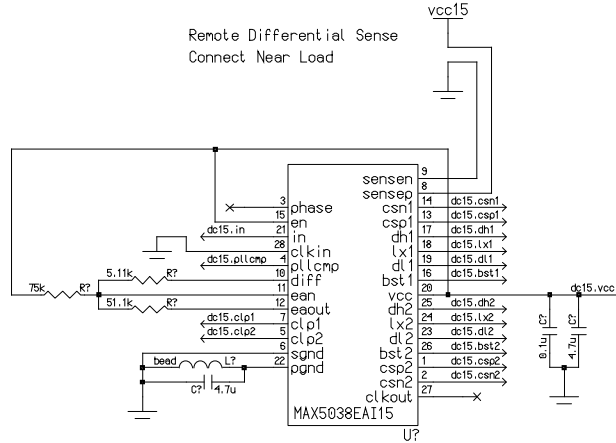
Star
University of Toronto

DC-DC Converter (1.5v 50A)

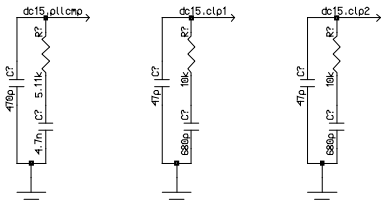
MAX5038 Power Supply Filter



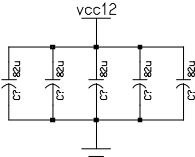
Remote Differential Sense
Connect Near Load



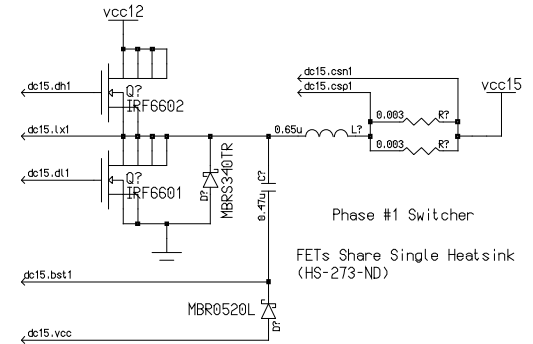
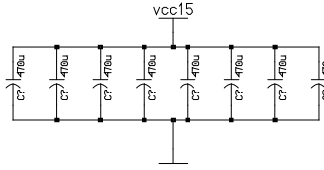
Compensation Networks



Decoupling Capacitors
Distribute Around Highside FETs

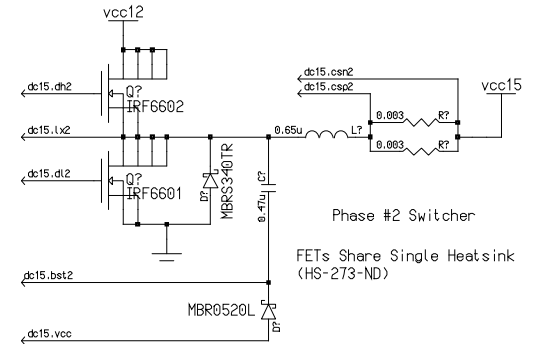


Bulk Holdup Capacitors
Distribute Around 1.5v Loads



Phase #1 Switch

FETs Share Single Heatsink
(HS-273-ND)

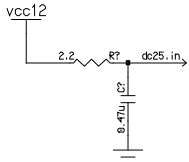


Phase #2 Switch

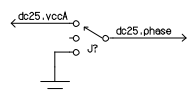
FETs Share Single Heatsink
(HS-273-ND)

DC-DC Converter (2.5v 100A Peak)

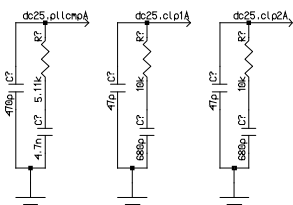
MAX5038 Power Supply Filter



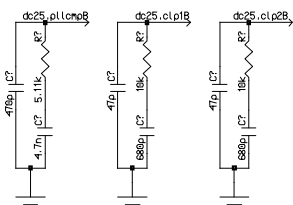
Phase Selection Jumper (vcc=120deg, NC=90deg, gnd=60deg)



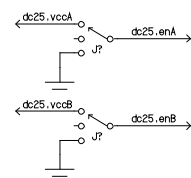
Compensation Networks



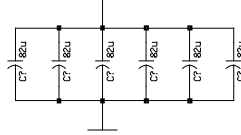
Compensation Networks



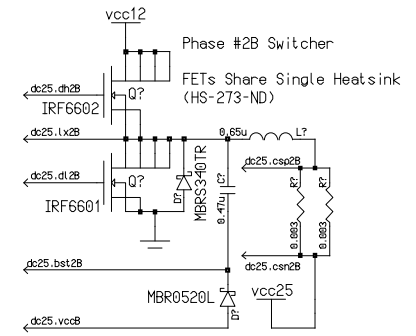
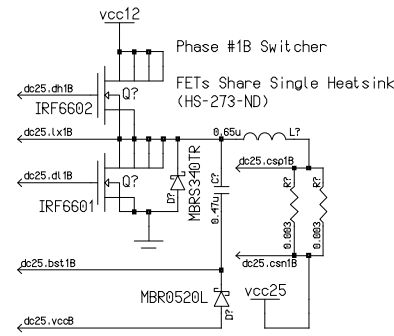
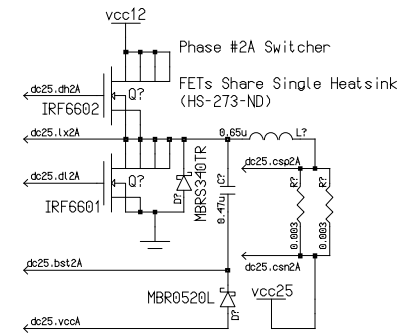
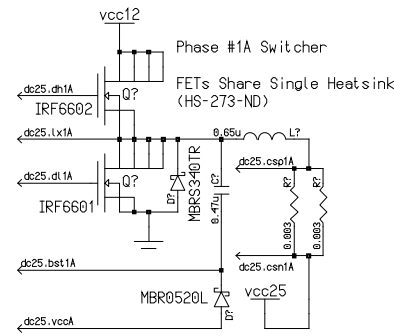
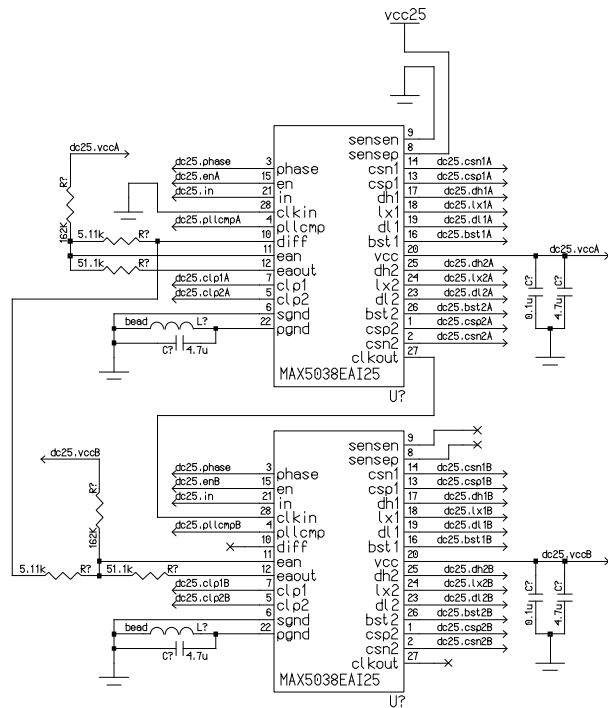
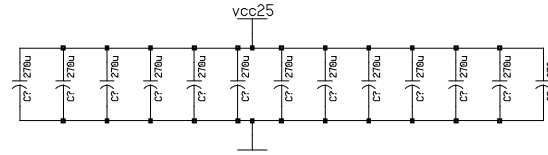
Controller Enable Jumpers



Decoupling Capacitors
Distribute Around Highside FETs
vcc12



Bulk Holdup Capacitors
(1 Per DDR Ground, 2 Per Dev. FPGA, 1 Int FPGA)



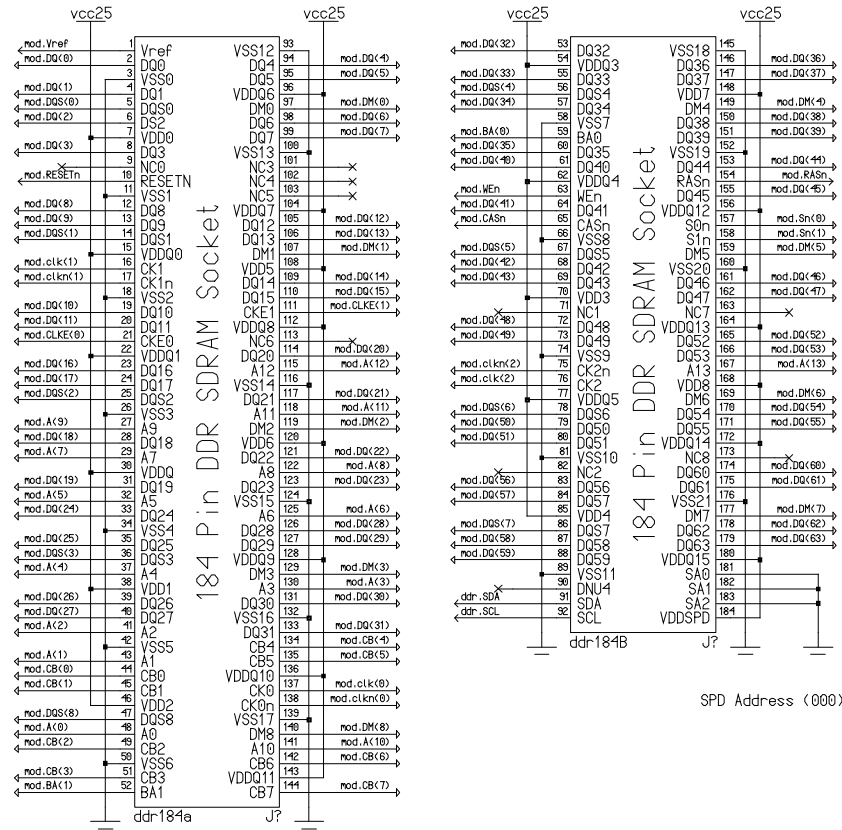
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Texas Instruments

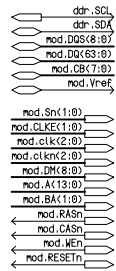
DDR Module Sockets

- mod.DQS(8:0)
- mod.DM(8:0)
- mod.DQ(63:0)
- mod.CB(7:0)
- mod.A(13:0)
- mod.BA(1:0)
- mod.RASn
- mod.CASn
- mod.WEn
- mod.RESETr
- ddr.SCl
- ddr.SDA
- mod.Vref
- mod.Sn(1:0)
- mod.CLKE(1:0)
- mod.clkn(2:0)
- mod.clkn(2:0)

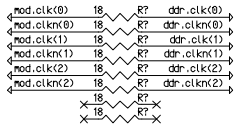
DDR SDRAM 184 Pin Socket A



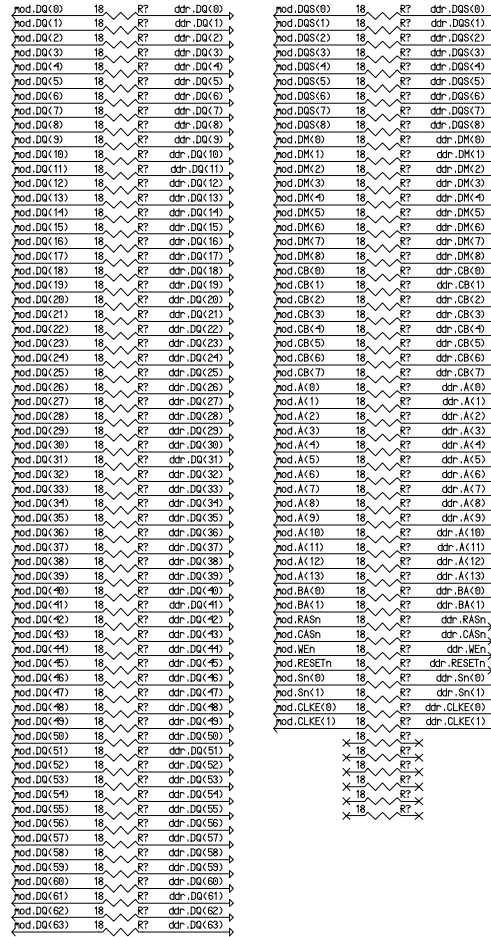
DDR Termination Regulator / Clock Buffer / Termination



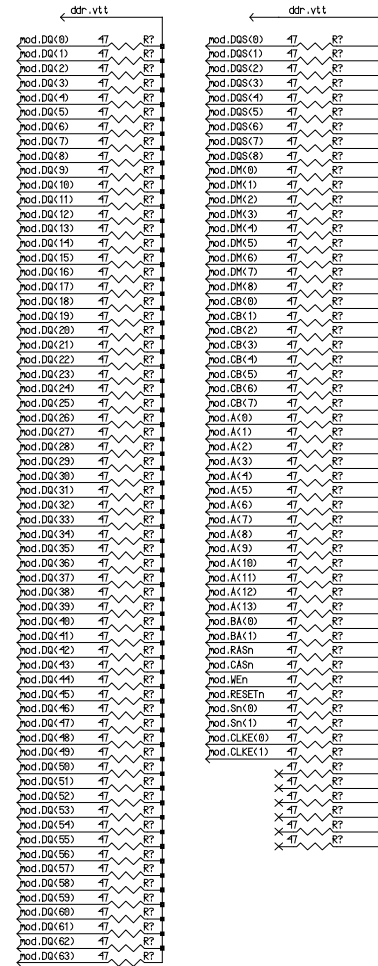
Differential Clock Series Termination



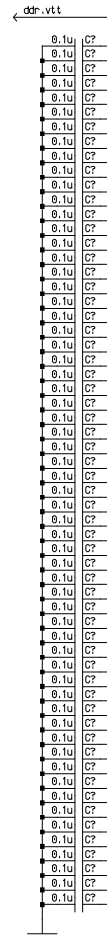
SSTL-2 Series Termination



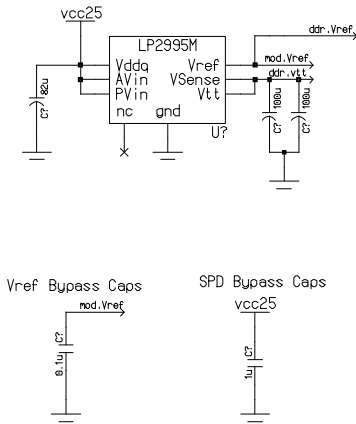
SSTL-2 Parallel Termination Place After Last Socket



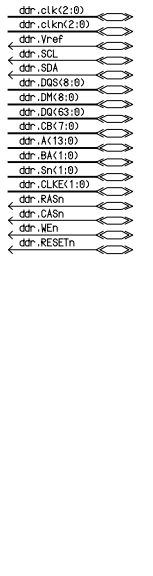
SSTL-2 Termination Bypass 1 Per 2 Termination Res



Termination Regulator



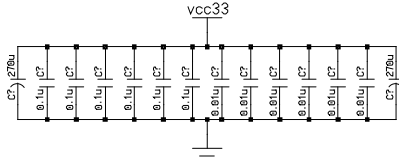
Top Level Ports



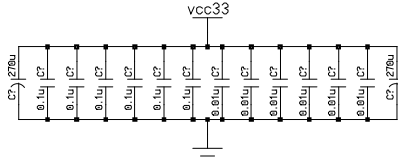
Termination Resistor's Values Are Placeholders
Pending Board Level Simulation

Development FPGA Bypass Capacitors

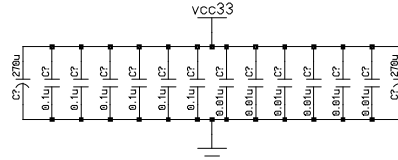
FPGA0 Banks 1,2,5,6 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



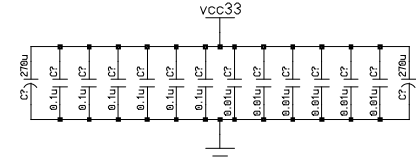
FPGA1 Banks 1,2,5,6 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



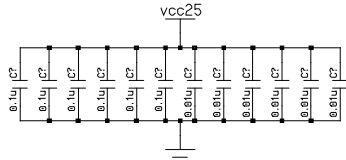
FPGA2 Banks 1,2,5,6 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



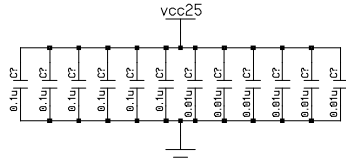
FPGA3 Banks 1,2,5,6 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



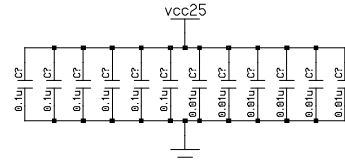
FPGA0 Banks 3,4,7,8 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



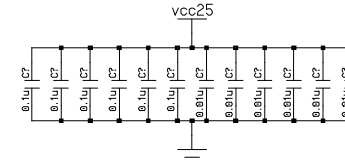
FPGA1 Banks 3,4,7,8 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



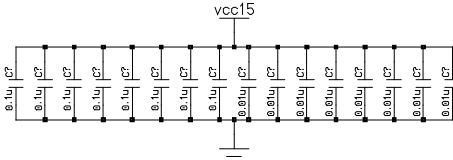
FPGA2 Banks 3,4,7,8 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



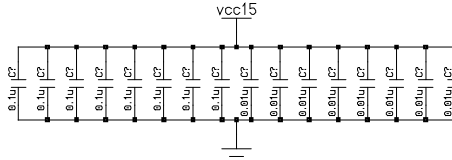
FPGA3 Banks 3,4,7,8 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



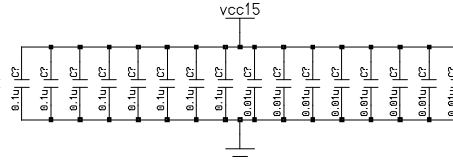
FPGA0 Vccint Bypass Caps 0603
Place near center of FPGA bottom side



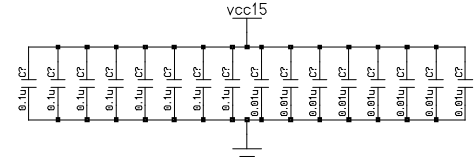
FPGA1 Vccint Bypass Caps 0603
Place near center of FPGA bottom side



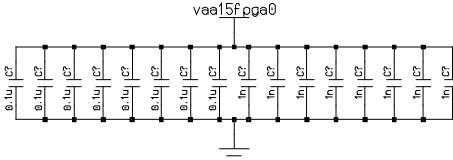
FPGA2 Vccint Bypass Caps 0603
Place near center of FPGA bottom side



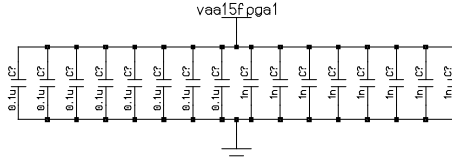
FPGA3 Vccint Bypass Caps 0603
Place near center of FPGA bottom side



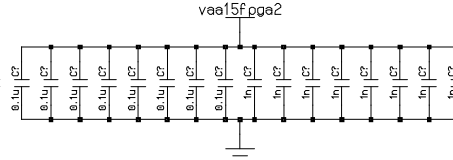
FPGA0 Vcca_pll Bypass Caps 0603
Place pair by each of 8 power pin groups



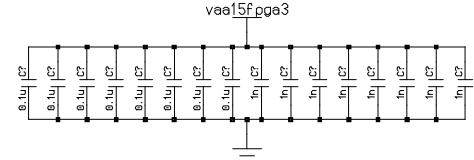
FPGA1 Vcca_pll Bypass Caps 0603
Place pair by each of 8 power pin groups



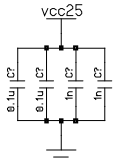
FPGA2 Vcca_pll Bypass Caps 0603
Place pair by each of 8 power pin groups



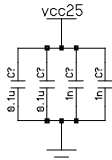
FPGA3 Vcca_pll Bypass Caps 0603
Place pair by each of 8 power pin groups



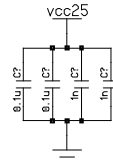
FPGA0 vcc_pll_out Bypass Caps 0603
Place pair by each of 2 power pin groups



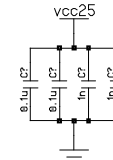
FPGA1 vcc_pll_out Bypass Caps 0603
Place pair by each of 2 power pin groups



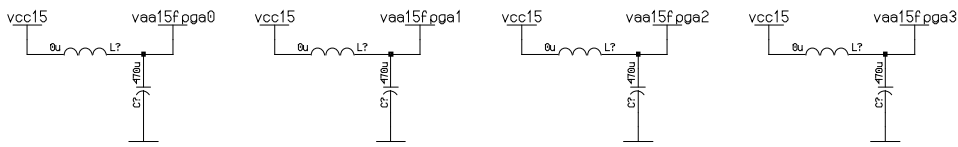
FPGA2 vcc_pll_out Bypass Caps 0805
Place pair by each of 2 power pin groups



FPGA3 vcc_pll_out Bypass Caps 0603
Place pair by each of 2 power pin groups



PLL Analog Supply Ferrite Beads and Bulk Caps

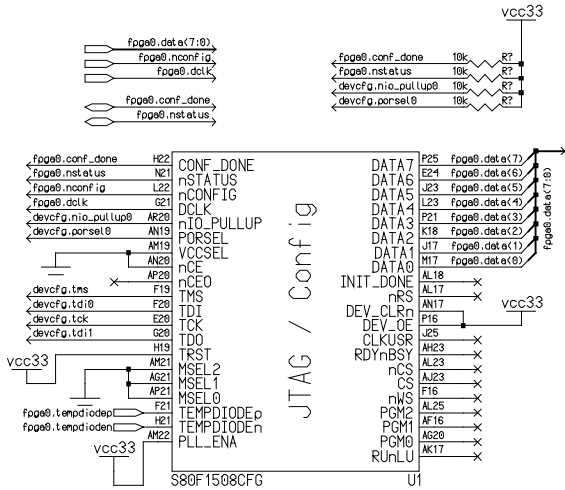


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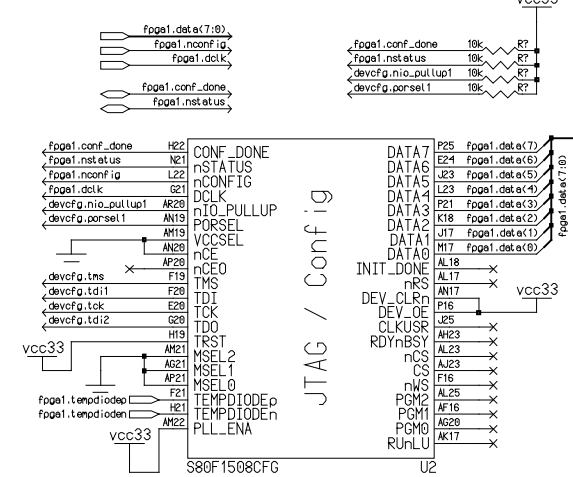
Star
University of Toronto

Development FPGA Configuration

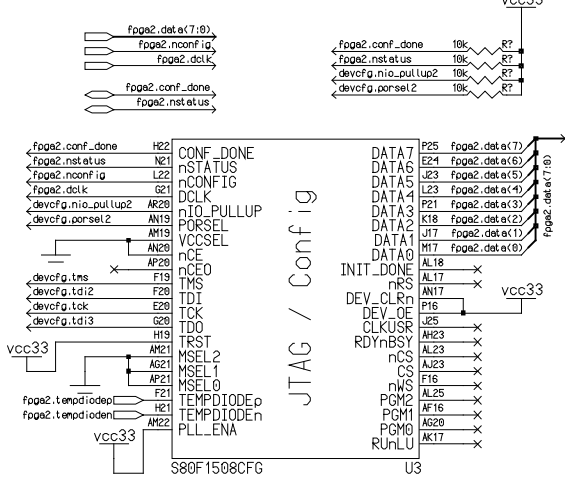
FPGA 0 Configuration Section



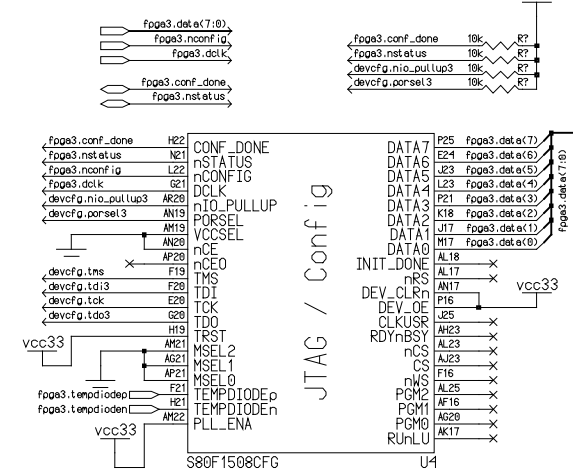
FPGA 1 Configuration Section



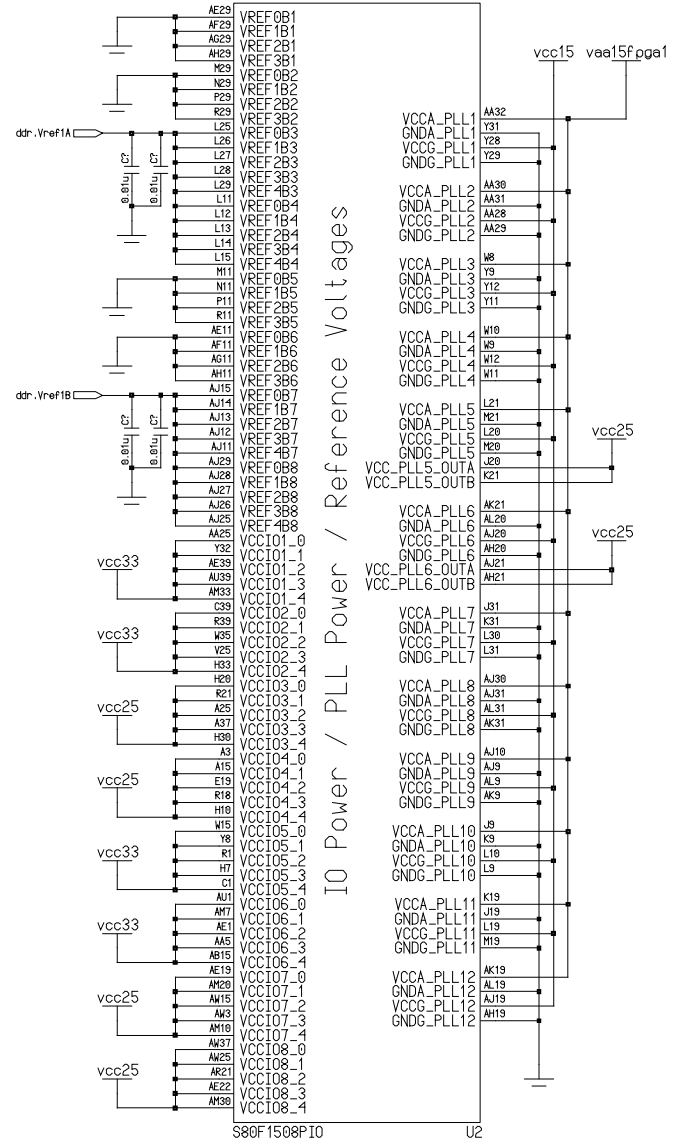
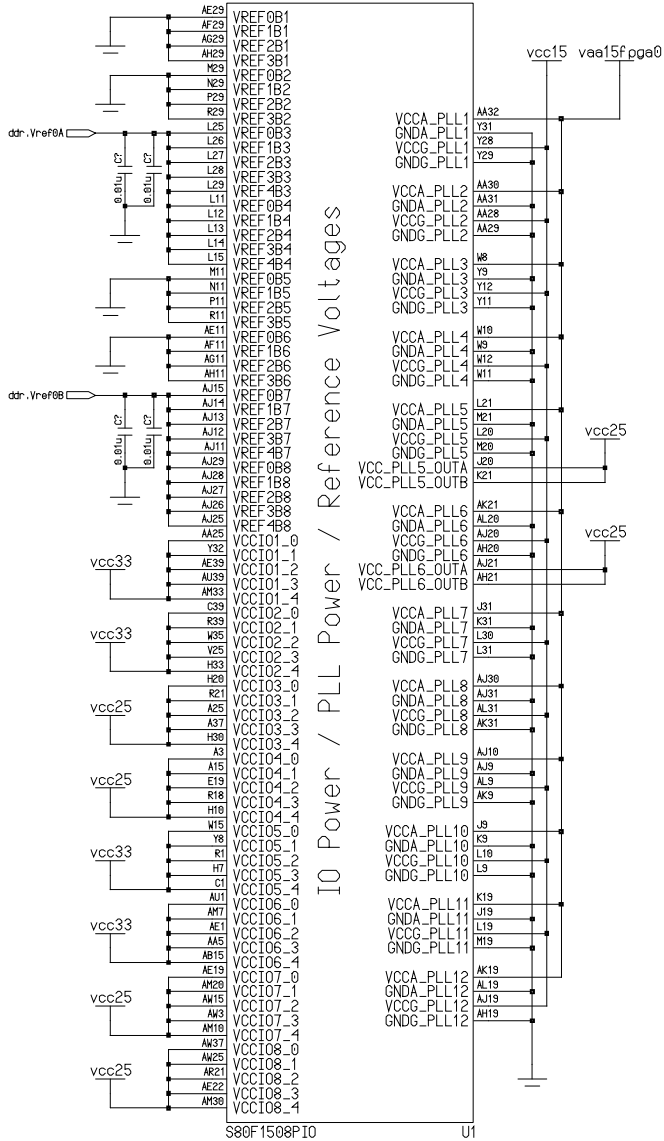
FPGA 2 Configuration Section



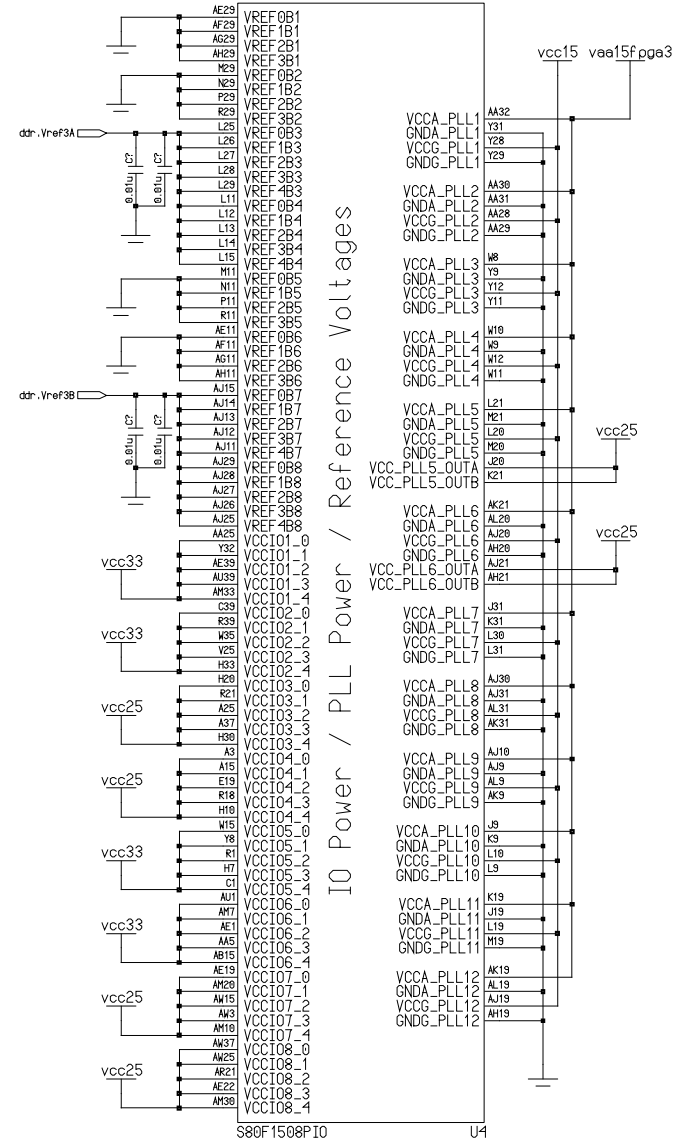
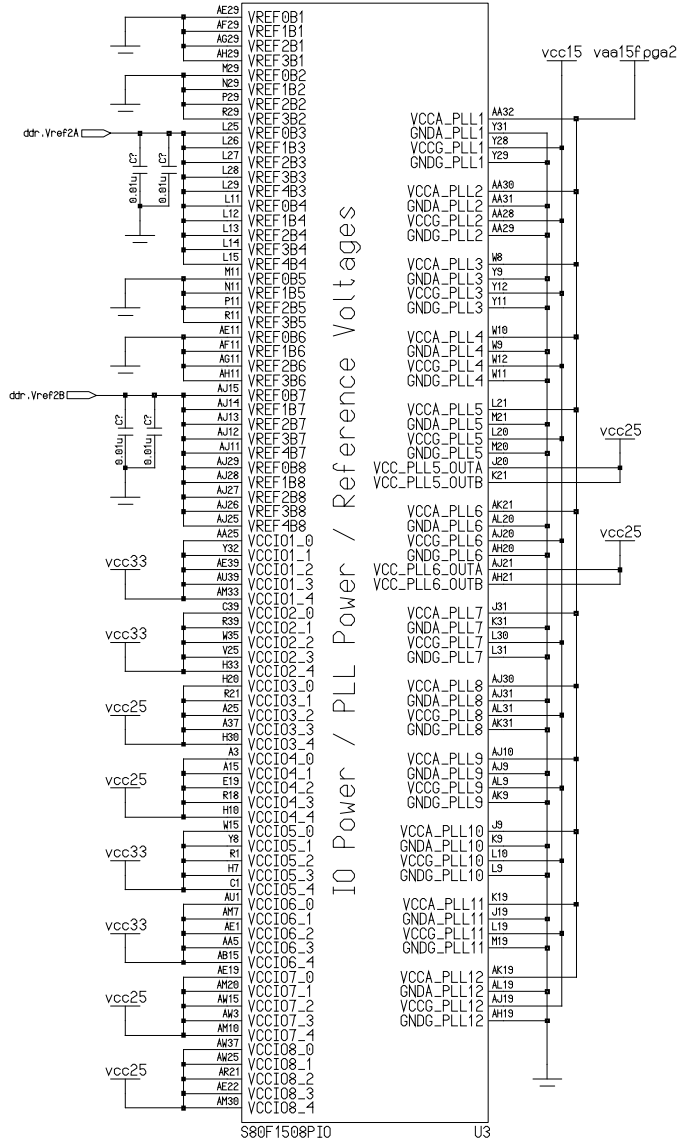
FPGA 3 Configuration Section



Development FPGAs 0, 1 IO/PLL Power & References



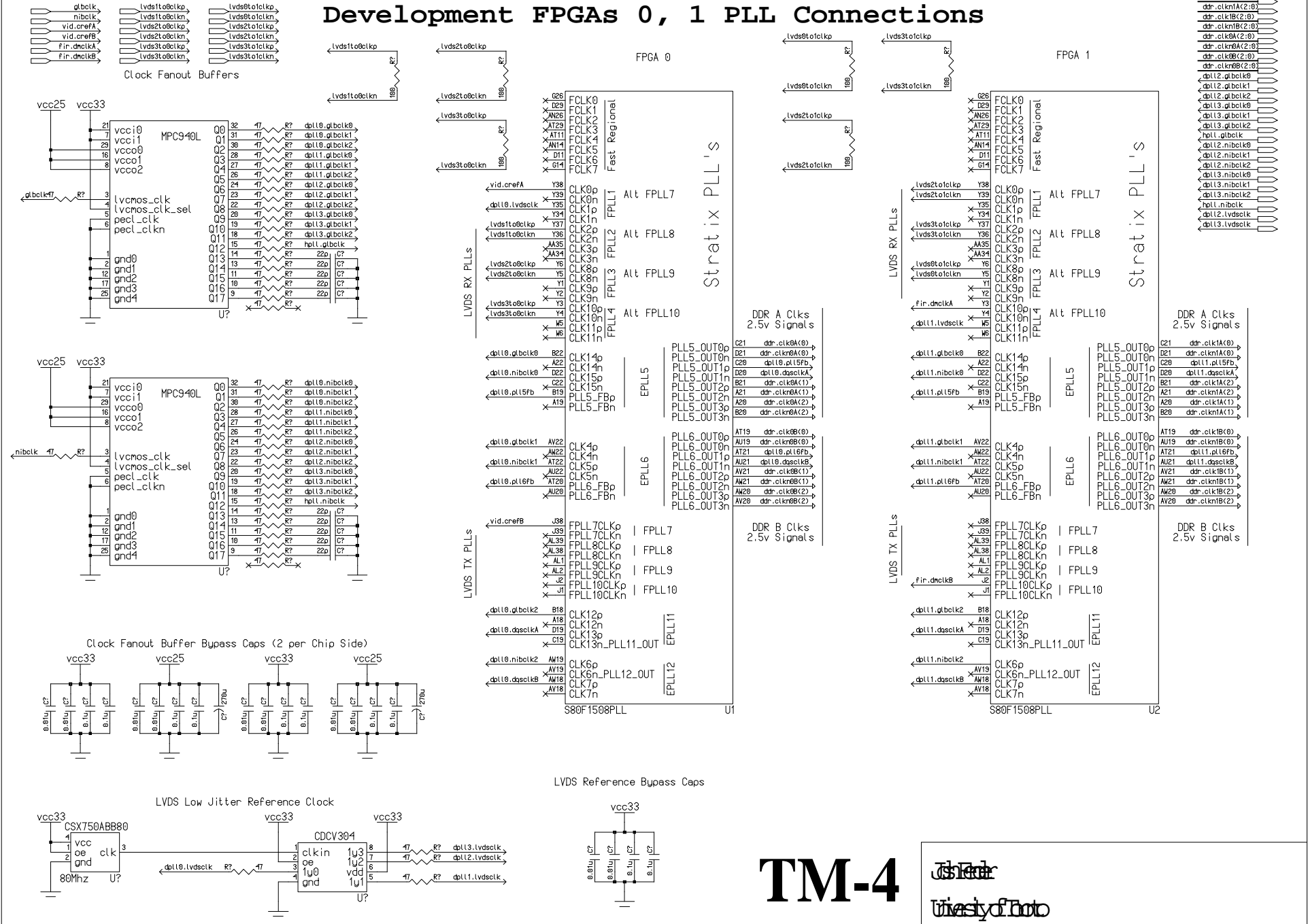
Development FPGAs 2, 3 IO/PLL Power & References



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Texas
University of
Houston

Development FPGAs 0, 1 PLL Connections



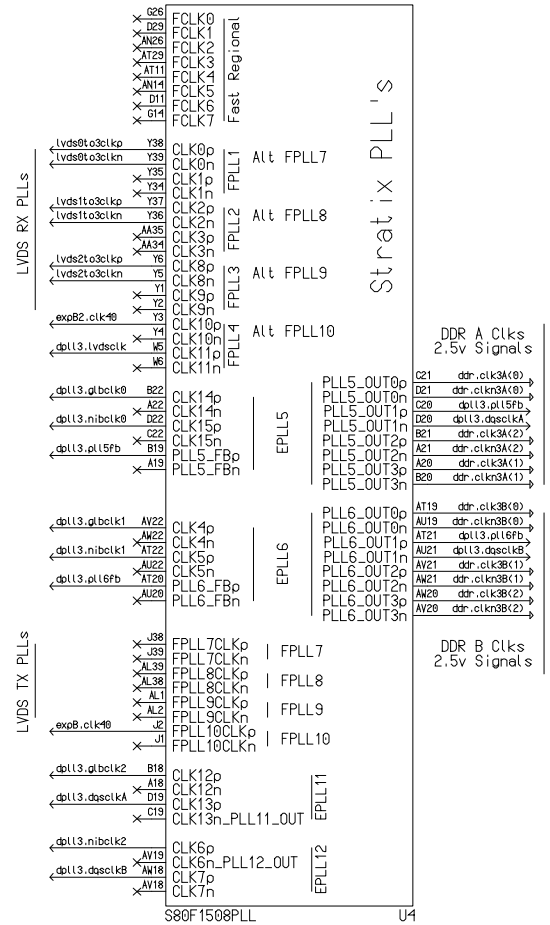
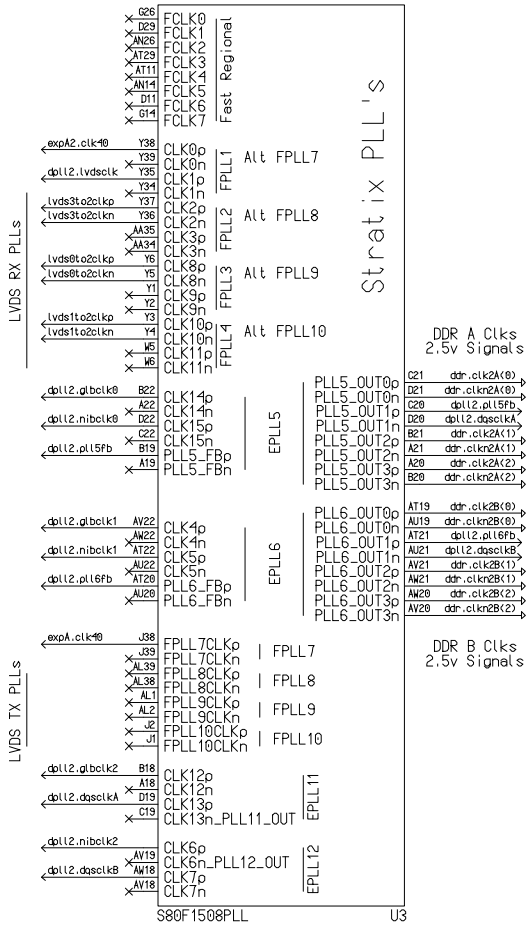
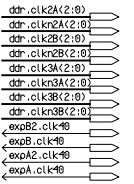
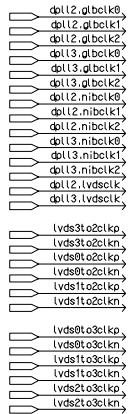
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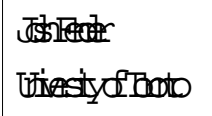
Development FPGAs 2, 3 PLL Connections

FPGA 2

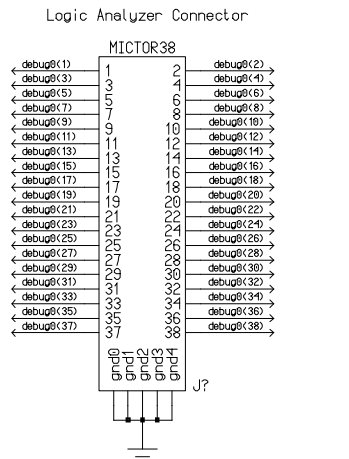
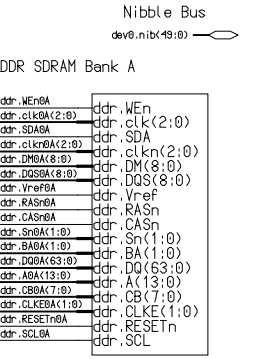
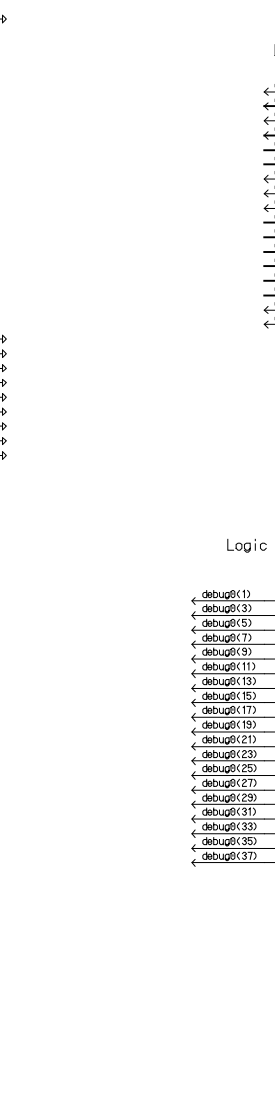
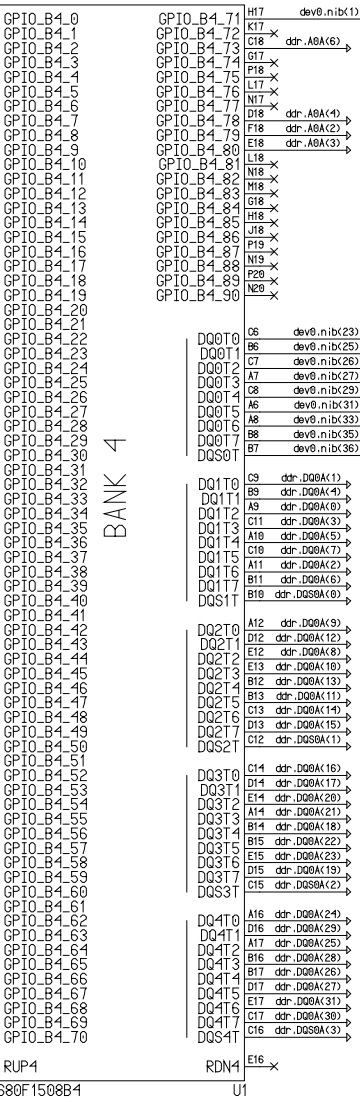
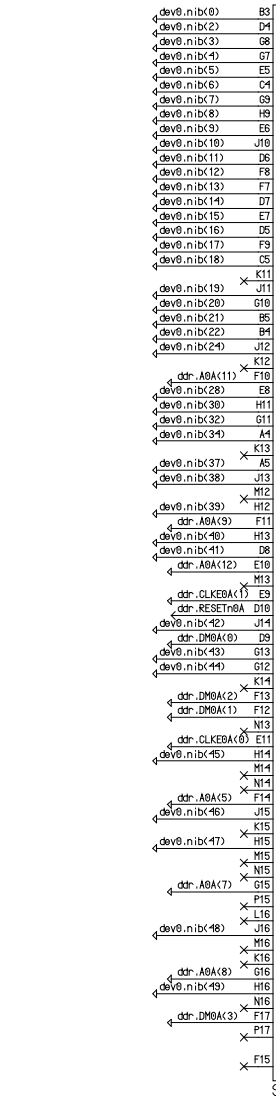
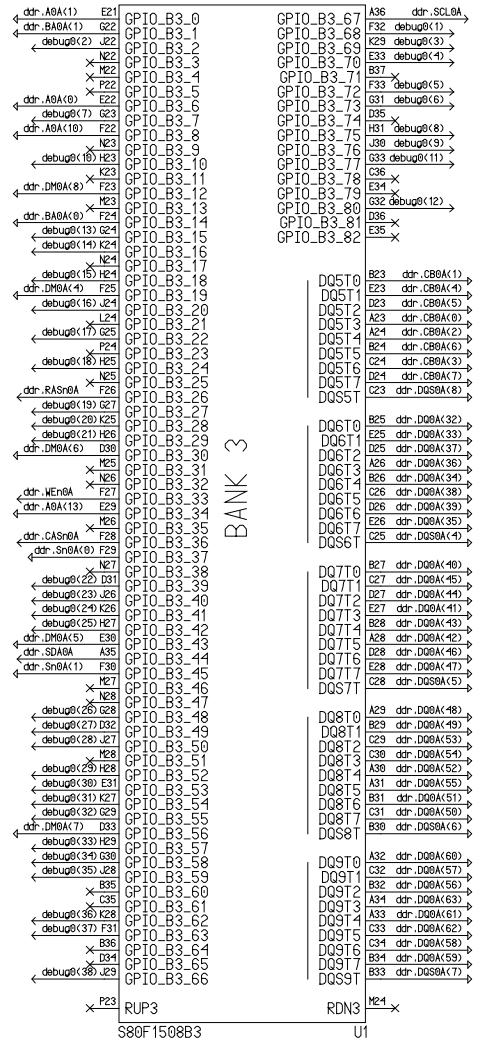
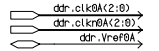
FPGA 3



TM-4

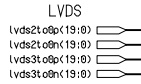


Development FPGA 0 Banks 3 and 4

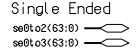
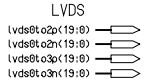


TM-4

Intel
University of Toronto



Development FPGA 0 Banks 5 and 6



```

se0t_03(0) F6 DIFFIO_RX76p
se0t_03(1) F5 DIFFIO_RX76n
se0t_03(2) G5 DIFFIO_RX77p
se0t_03(3) G6 DIFFIO_RX77n
se0t_03(4) H5 DIFFIO_RX78p
se0t_03(5) H6 DIFFIO_RX78n
se0t_03(6) J5 DIFFIO_RX79p
se0t_03(7) J6 DIFFIO_RX79n
se0t_03(8) K5 DIFFIO_RX80p
se0t_03(9) K6 DIFFIO_RX80n
se0t_03(10) E4 DIFFIO_RX81p
se0t_03(11) E3 DIFFIO_RX81n
se0t_03(12) F4 DIFFIO_RX82p
se0t_03(13) F3 DIFFIO_RX82n
se0t_03(14) G3 DIFFIO_RX83p
se0t_03(15) G4 DIFFIO_RX83n
se0t_03(16) H4 DIFFIO_RX84p
se0t_03(17) H3 DIFFIO_RX84n
se0t_03(18) J4 DIFFIO_RX85p
se0t_03(19) J3 DIFFIO_RX85n
se0t_03(20) E1 DIFFIO_RX86p
se0t_03(21) E2 DIFFIO_RX86n
se0t_03(22) F1 DIFFIO_RX87p
se0t_03(23) F2 DIFFIO_RX87n
se0t_03(24) G1 DIFFIO_RX88p
se0t_03(25) G2 DIFFIO_RX88n
se0t_03(26) H1 DIFFIO_RX89p
se0t_03(27) H2 DIFFIO_RX89n
  
```

PLL0 Low Speed RX (14)

```

DIFFIO_TX76p P12 se0t_03(28)
DIFFIO_TX76n N12 se0t_03(29)
DIFFIO_TX77p J14 se0t_03(30)
DIFFIO_TX77n K14 se0t_03(31)
DIFFIO_TX78p K12 se0t_03(32)
DIFFIO_TX78n K13 se0t_03(33)
DIFFIO_TX79p T12 se0t_03(34)
DIFFIO_TX79n T11 se0t_03(35)
DIFFIO_TX80p Q14 se0t_03(36)
DIFFIO_TX80n T13 se0t_03(37)
DIFFIO_TX81p N10 se0t_03(38)
DIFFIO_TX81n N9 se0t_03(39)
DIFFIO_TX82p P9 se0t_03(40)
DIFFIO_TX82n P10 se0t_03(41)
DIFFIO_TX83p K9 se0t_03(42)
DIFFIO_TX83n K10 se0t_03(43)
DIFFIO_TX84p M10 LVDS0_03p(13)
DIFFIO_TX84n M9 LVDS0_03n(13)
DIFFIO_TX85p J7 LVDS0_03p(18)
DIFFIO_TX85n J8 LVDS0_03n(18)
DIFFIO_TX86p K8 LVDS0_03p(16)
DIFFIO_TX86n K7 LVDS0_03n(16)
DIFFIO_TX87p L7 LVDS0_03p(14)
DIFFIO_TX87n L8 LVDS0_03n(14)
DIFFIO_TX88p K6 LVDS0_03p(19)
DIFFIO_TX88n K5 LVDS0_03n(19)
DIFFIO_TX89p M6 LVDS0_03p(11)
DIFFIO_TX89n M7 LVDS0_03n(11)
DIFFIO_TX90p L6 LVDS0_03p(17)
DIFFIO_TX90n L5 LVDS0_03n(17)
DIFFIO_TX91p K6 LVDS0_03p(15)
DIFFIO_TX91n K7 LVDS0_03n(15)
DIFFIO_TX92p N7 LVDS0_03p(12)
DIFFIO_TX92n N8 LVDS0_03n(12)
DIFFIO_TX93p N6 LVDS0_03p(9)
DIFFIO_TX93n N5 LVDS0_03n(9)
DIFFIO_TX94p P8 LVDS0_03p(10)
DIFFIO_TX94n P7 LVDS0_03n(10)
DIFFIO_TX95p P8 LVDS0_03p(8)
DIFFIO_TX95n P7 LVDS0_03n(8)
DIFFIO_TX96p R8 LVDS0_03p(6)
DIFFIO_TX96n R6 LVDS0_03n(7)
DIFFIO_TX97p R5 LVDS0_03p(7)
DIFFIO_TX97n T10 LVDS0_03p(4)
DIFFIO_TX98p T9 LVDS0_03n(4)
DIFFIO_TX99p T8 LVDS0_03p(2)
DIFFIO_TX99n T7 LVDS0_03n(2)
DIFFIO_TX100p T6 LVDS0_03p(5)
DIFFIO_TX100n T5 LVDS0_03n(5)
DIFFIO_TX101p U6 LVDS0_03p(3)
DIFFIO_TX101n U7 LVDS0_03n(3)
DIFFIO_TX102p U8 LVDS0_03n(1)
DIFFIO_TX102n V6 LVDS0_03p(0)
DIFFIO_TX103p V6 LVDS0_03n(0)
DIFFIO_TX103n U11 se0t_03(44)
DIFFIO_TX104p U12 se0t_03(45)
DIFFIO_TX104n U10 se0t_03(46)
DIFFIO_TX105p U9 se0t_03(47)
DIFFIO_TX105n V13 se0t_03(48)
DIFFIO_TX106p V13 se0t_03(49)
DIFFIO_TX106n V11 se0t_03(51)
DIFFIO_TX107p V10 se0t_03(52)
DIFFIO_TX107n V9 se0t_03(53)
DIFFIO_TX108p V8 LVDS0_03p(6)
DIFFIO_TX108n V7 LVDS0_03n(6)
DIFFIO_TX109p V14 se0t_03(54)
DIFFIO_TX109n V14 se0t_03(55)
DIFFIO_TX110p V13 se0t_03(56)
DIFFIO_TX110n V13 se0t_03(57)
DIFFIO_TX111p V14 se0t_03(58)
DIFFIO_TX111n V14 se0t_03(59)
DIFFIO_TX112p W3 se0t_03(60)
DIFFIO_TX112n W3 se0t_03(61)
DIFFIO_TX113p W4 se0t_03(62)
DIFFIO_TX113n W4 se0t_03(63)
  
```

PLL10 Low Speed TX (8)

PLL10 Highspeed TX (20)

BANK 5

PLL4 Highspeed RX (20)

```

LVDS3_0a0p(0) J1 DIFFIO_RX94p
LVDS3_0a0n(0) J3 DIFFIO_RX94n
LVDS3_0a0p(1) K1 DIFFIO_RX95p
LVDS3_0a0n(1) K3 DIFFIO_RX95n
LVDS3_0a0p(2) K2 DIFFIO_RX96p
LVDS3_0a0n(2) K4 DIFFIO_RX96n
LVDS3_0a0p(3) L2 DIFFIO_RX97p
LVDS3_0a0n(3) L3 DIFFIO_RX97n
LVDS3_0a0p(4) L4 DIFFIO_RX98p
LVDS3_0a0n(4) L5 DIFFIO_RX98n
LVDS3_0a0p(5) M1 DIFFIO_RX99p
LVDS3_0a0n(5) M3 DIFFIO_RX99n
LVDS3_0a0p(6) M2 DIFFIO_RX100p
LVDS3_0a0n(6) M4 DIFFIO_RX100n
LVDS3_0a0p(7) N2 DIFFIO_RX101p
LVDS3_0a0n(7) N4 DIFFIO_RX101n
LVDS3_0a0p(8) N3 DIFFIO_RX102p
LVDS3_0a0n(8) P2 DIFFIO_RX102n
LVDS3_0a0p(9) P1 DIFFIO_RX102n
LVDS3_0a0n(9) R2 DIFFIO_RX103p
LVDS3_0a0p(10) P4 DIFFIO_RX103n
LVDS3_0a0p(10) P3 DIFFIO_RX104p
LVDS3_0a0n(10) R4 DIFFIO_RX104n
LVDS3_0a0p(11) R1 DIFFIO_RX105p
LVDS3_0a0n(11) R3 DIFFIO_RX105n
LVDS3_0a0p(12) T4 DIFFIO_RX106p
LVDS3_0a0n(12) T2 DIFFIO_RX106n
LVDS3_0a0p(13) T3 DIFFIO_RX107p
LVDS3_0a0n(13) T5 DIFFIO_RX107n
LVDS3_0a0p(14) U2 DIFFIO_RX108p
LVDS3_0a0n(14) U3 DIFFIO_RX108n
LVDS3_0a0p(15) U4 DIFFIO_RX109p
LVDS3_0a0n(15) U5 DIFFIO_RX109n
LVDS3_0a0p(16) V4 DIFFIO_RX110p
LVDS3_0a0n(16) V3 DIFFIO_RX110n
LVDS3_0a0p(17) V2 DIFFIO_RX111p
LVDS3_0a0n(17) V1 DIFFIO_RX111n
LVDS3_0a0p(18) W3 DIFFIO_RX112p
LVDS3_0a0n(18) W2 DIFFIO_RX112n
LVDS3_0a0p(19) W4 DIFFIO_RX113p
LVDS3_0a0n(19) W1 DIFFIO_RX113n
  
```

se0t_03(62) P13 GPIO_B5_0
S80F1508B5

PLL4 Low Speed TX (10)

```

LVDS2_0a0p(13) AA1 DIFFIO_RX114p
LVDS2_0a0n(13) AA2 DIFFIO_RX114n
LVDS2_0a0p(18) AA3 DIFFIO_RX115p
LVDS2_0a0n(18) AA4 DIFFIO_RX115n
LVDS2_0a0p(12) AB2 DIFFIO_RX116p
LVDS2_0a0n(12) AB1 DIFFIO_RX116n
LVDS2_0a0p(17) AB3 DIFFIO_RX117p
LVDS2_0a0n(17) AB4 DIFFIO_RX117n
LVDS2_0a0p(11) AC2 DIFFIO_RX118p
LVDS2_0a0n(11) AC1 DIFFIO_RX118n
LVDS2_0a0p(16) AC3 DIFFIO_RX118n
LVDS2_0a0n(16) AC4 DIFFIO_RX119p
LVDS2_0a0p(18) AD1 DIFFIO_RX119n
LVDS2_0a0n(18) AD2 DIFFIO_RX120p
LVDS2_0a0p(19) AD3 DIFFIO_RX121p
LVDS2_0a0n(19) AD4 DIFFIO_RX121n
LVDS2_0a0p(15) AE3 DIFFIO_RX122p
LVDS2_0a0n(15) AE4 DIFFIO_RX122n
LVDS2_0a0p(14) AF3 DIFFIO_RX123p
LVDS2_0a0n(14) AF4 DIFFIO_RX123n
LVDS2_0a0p(8) AF2 DIFFIO_RX124p
LVDS2_0a0n(8) AF1 DIFFIO_RX124n
LVDS2_0a0p(6) AF2 DIFFIO_RX125p
LVDS2_0a0n(6) AF2 DIFFIO_RX125n
LVDS2_0a0p(9) AG3 DIFFIO_RX125n
LVDS2_0a0n(9) AG4 DIFFIO_RX126p
LVDS2_0a0p(3) AH2 DIFFIO_RX127p
LVDS2_0a0n(3) AH1 DIFFIO_RX127n
LVDS2_0a0p(7) AH3 DIFFIO_RX128p
LVDS2_0a0n(7) AH4 DIFFIO_RX128n
LVDS2_0a0p(2) AJ2 DIFFIO_RX129p
LVDS2_0a0n(2) AJ3 DIFFIO_RX129n
LVDS2_0a0p(5) AJ3 DIFFIO_RX130p
LVDS2_0a0n(5) AJ4 DIFFIO_RX130n
LVDS2_0a0p(0) AK2 DIFFIO_RX131p
LVDS2_0a0n(0) AK1 DIFFIO_RX131n
LVDS2_0a0p(4) AK3 DIFFIO_RX132p
LVDS2_0a0n(4) AK4 DIFFIO_RX132n
LVDS2_0a0p(1) AL3 DIFFIO_RX133p
LVDS2_0a0n(1) AL4 DIFFIO_RX133n
  
```

PLL3 Highspeed RX (20)

BANK 6

PLL3 Low Speed TX (10)

PLL3 Highspeed TX (20)

```

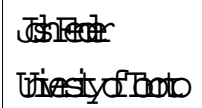
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se0t_02(43) AN1 DIFFIO_RX139p
se0t_02(37) AN2 DIFFIO_RX139n
se0t_02(57) AP2 DIFFIO_RX140p
se0t_02(46) AP1 DIFFIO_RX140n
se0t_02(16) AP1 DIFFIO_RX140n
se0t_02(11) AP2 DIFFIO_RX141p
se0t_02(18) AT1 DIFFIO_RX141n
se0t_02(19) AT2 DIFFIO_RX142p
se0t_02(47) AH3 DIFFIO_RX143p
se0t_02(9) AH4 DIFFIO_RX143n
se0t_02(13) AN3 DIFFIO_RX144p
se0t_02(17) AN4 DIFFIO_RX144n
se0t_02(15) AP4 DIFFIO_RX145p
se0t_02(8) AP3 DIFFIO_RX145n
se0t_02(2) U2 DIFFIO_RX146p
se0t_02(14) AT3 DIFFIO_RX146n
se0t_02(39) AP3 DIFFIO_RX146n
se0t_02(3) AP4 DIFFIO_RX147p
se0t_02(35) AL5 DIFFIO_RX147n
se0t_02(55) AL6 DIFFIO_RX148p
se0t_02(12) AH5 DIFFIO_RX149p
se0t_02(10) AH6 DIFFIO_RX149n
se0t_02(1) AH6 DIFFIO_RX150p
se0t_02(4) AH5 DIFFIO_RX150n
se0t_02(0) AP5 DIFFIO_RX151p
se0t_02(39) AP6 DIFFIO_RX151n
  
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se0t_02(32) AF13 GPIO_B6_0
S80F1508B6

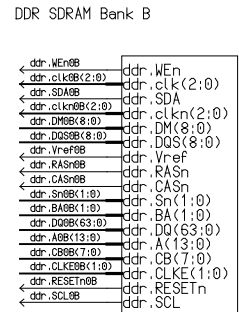
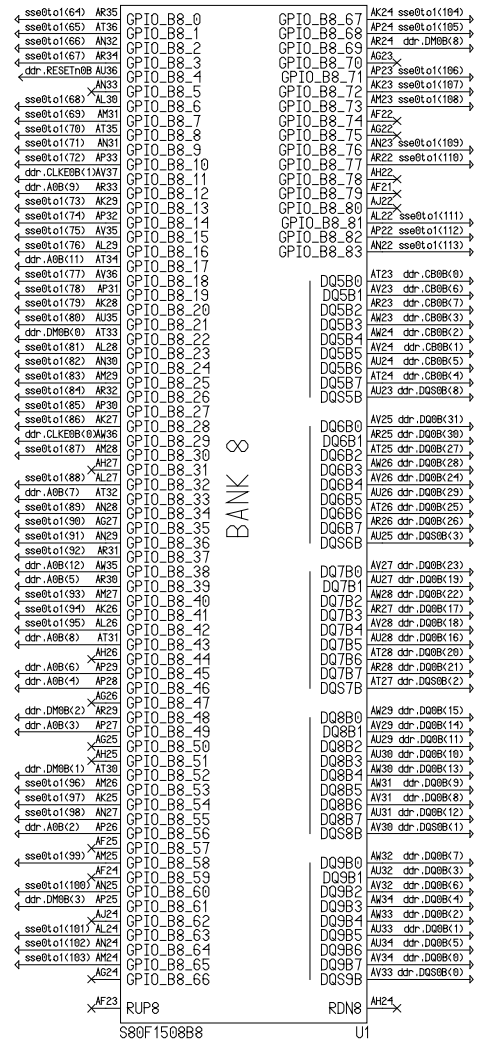
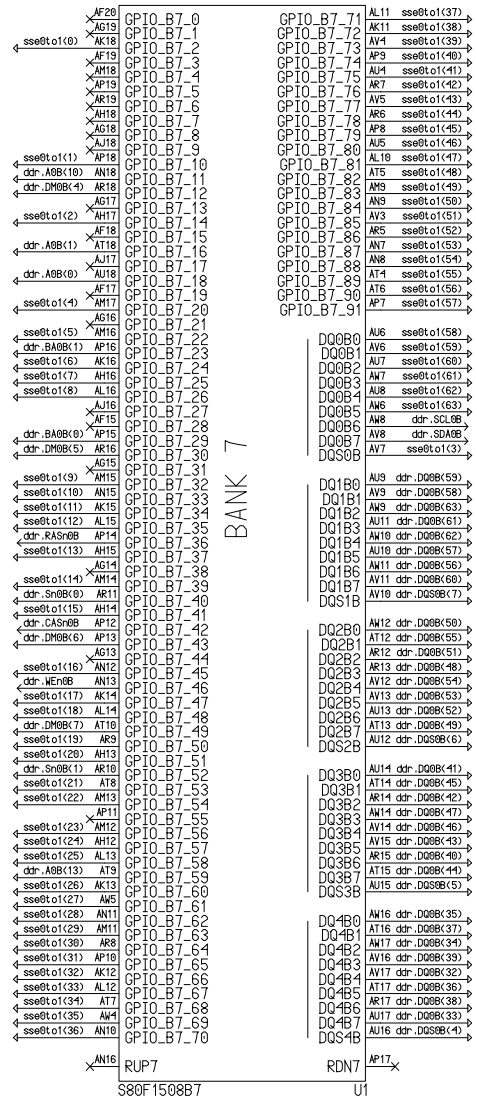
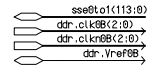
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DIFFIO_TX114p AA6 se0t_02(40)
DIFFIO_TX114n AB7 se0t_02(42)
DIFFIO_TX115p AA8 se0t_02(60)
DIFFIO_TX115n AA9 se0t_02(59)
DIFFIO_TX116p AA10 se0t_02(51)
DIFFIO_TX116n AA11 se0t_02(34)
DIFFIO_TX117p AA13 se0t_02(44)
DIFFIO_TX117n AA12 se0t_02(53)
DIFFIO_TX118p AB9 se0t_02(58)
DIFFIO_TX118n AB8 se0t_02(56)
DIFFIO_TX119p AB11 se0t_02(45)
DIFFIO_TX119n AB10 se0t_02(49)
DIFFIO_TX120p AB12 se0t_02(61)
DIFFIO_TX120n AB13 se0t_02(29)
DIFFIO_TX121p AB14 se0t_02(36)
DIFFIO_TX121n AC14 se0t_02(46)
DIFFIO_TX122p AC10 se0t_02(58)
DIFFIO_TX122n AC9 se0t_02(54)
DIFFIO_TX123p AC11 se0t_02(31)
DIFFIO_TX123n AC12 se0t_02(60)
DIFFIO_TX124p AB5 LVDS0_02p(0)
DIFFIO_TX124n AC8 LVDS0_02n(0)
DIFFIO_TX125p AC7 LVDS0_02n(1)
DIFFIO_TX125n AC6 LVDS0_02p(2)
DIFFIO_TX126p AC5 LVDS0_02n(2)
DIFFIO_TX126n AC4 LVDS0_02p(3)
DIFFIO_TX127p AD6 LVDS0_02p(3)
DIFFIO_TX127n AD5 LVDS0_02n(3)
DIFFIO_TX128p AD7 LVDS0_02p(4)
DIFFIO_TX128n AD8 LVDS0_02n(4)
DIFFIO_TX129p AD9 LVDS0_02p(5)
DIFFIO_TX129n AE5 LVDS0_02p(6)
DIFFIO_TX130p AE6 LVDS0_02p(6)
DIFFIO_TX130n AE7 LVDS0_02p(7)
DIFFIO_TX131p AE8 LVDS0_02n(7)
DIFFIO_TX132p AF5 LVDS0_02p(8)
DIFFIO_TX132n AF6 LVDS0_02n(8)
DIFFIO_TX133p AF7 LVDS0_02p(9)
DIFFIO_TX133n AF8 LVDS0_02n(9)
DIFFIO_TX134p AG5 LVDS0_02p(10)
DIFFIO_TX134n AG6 LVDS0_02n(10)
DIFFIO_TX135p AH6 LVDS0_02p(11)
DIFFIO_TX135n AH5 LVDS0_02n(11)
DIFFIO_TX136p AJ6 LVDS0_02p(12)
DIFFIO_TX136n AJ5 LVDS0_02n(12)
DIFFIO_TX137p AK5 LVDS0_02p(13)
DIFFIO_TX137n AK6 LVDS0_02n(13)
DIFFIO_TX138p AG7 LVDS0_02p(14)
DIFFIO_TX138n AG8 LVDS0_02n(14)
DIFFIO_TX139p AH7 LVDS0_02p(15)
DIFFIO_TX139n AH8 LVDS0_02n(15)
DIFFIO_TX140p AJ8 LVDS0_02p(16)
DIFFIO_TX140n AJ7 LVDS0_02n(16)
DIFFIO_TX141p AK8 LVDS0_02p(17)
DIFFIO_TX141n AK7 LVDS0_02n(17)
DIFFIO_TX142p AL7 LVDS0_02p(18)
DIFFIO_TX142n AL8 LVDS0_02n(18)
DIFFIO_TX143p AH9 LVDS0_02p(19)
DIFFIO_TX143n AH10 LVDS0_02n(19)
DIFFIO_TX144p AD11 se0t_02(28)
DIFFIO_TX144n AD12 se0t_02(38)
DIFFIO_TX145p AD13 se0t_02(24)
DIFFIO_TX145n AE10 se0t_02(52)
DIFFIO_TX146p AE9 se0t_02(48)
DIFFIO_TX146n AD14 se0t_02(25)
DIFFIO_TX147p AE14 se0t_02(21)
DIFFIO_TX147n AF3 se0t_02(62)
DIFFIO_TX148p AF10 se0t_02(63)
DIFFIO_TX148n AG9 LVDS0_02p(6)
DIFFIO_TX149p AG10 LVDS0_02p(6)
DIFFIO_TX149n AE13 se0t_02(22)
DIFFIO_TX150p AE12 se0t_02(23)
DIFFIO_TX150n AG12 se0t_02(17)
DIFFIO_TX151p AF12 se0t_02(16)
DIFFIO_TX151n AF14 se0t_02(20)
  
```

se0t_02(32) AF13 GPIO_B6_1
S80F1508B6



Development FPGA 0 Banks 7 and 8

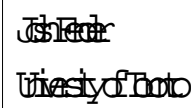
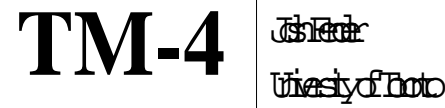
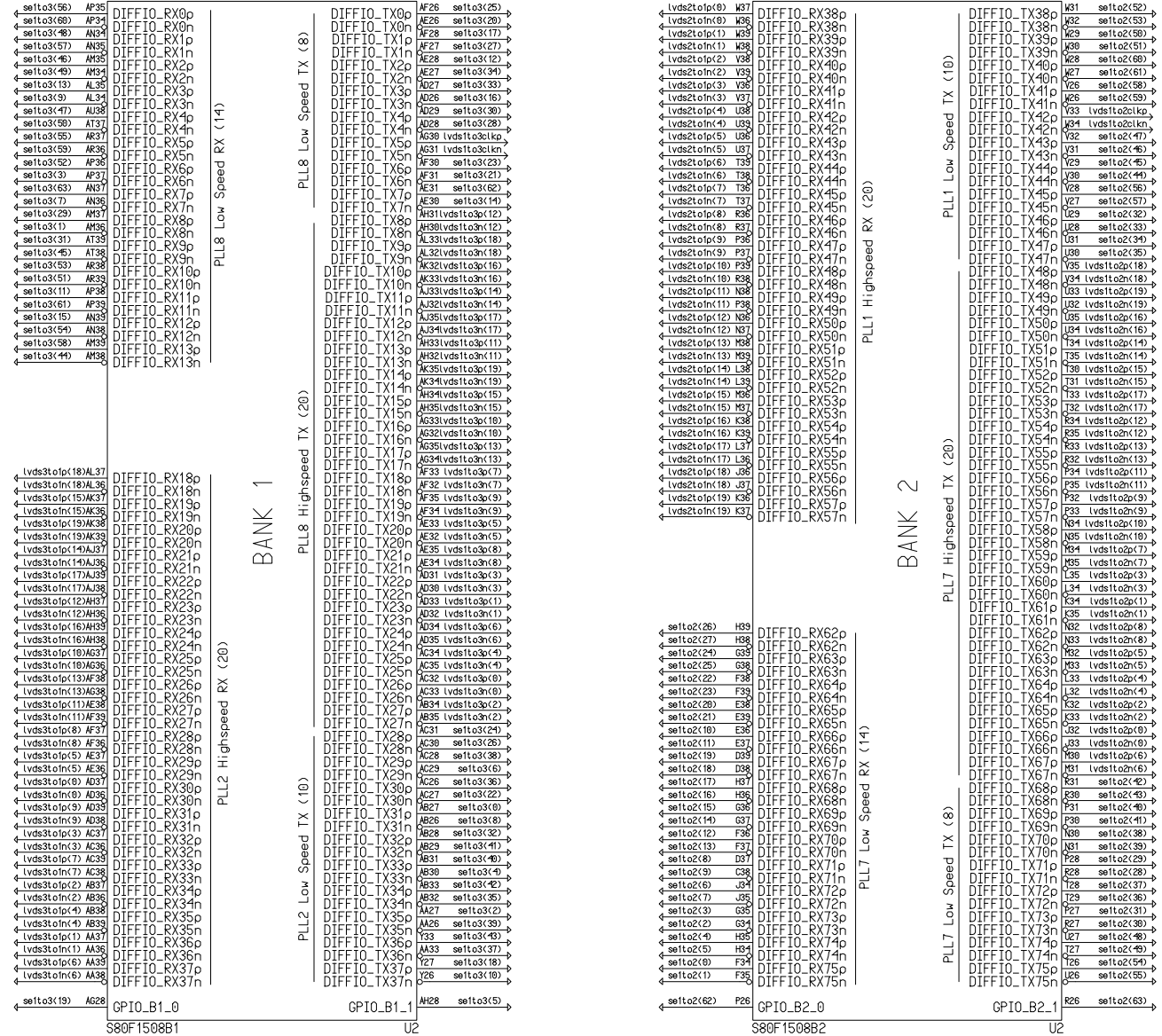
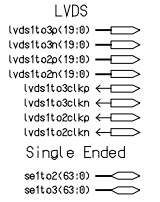


TM-4

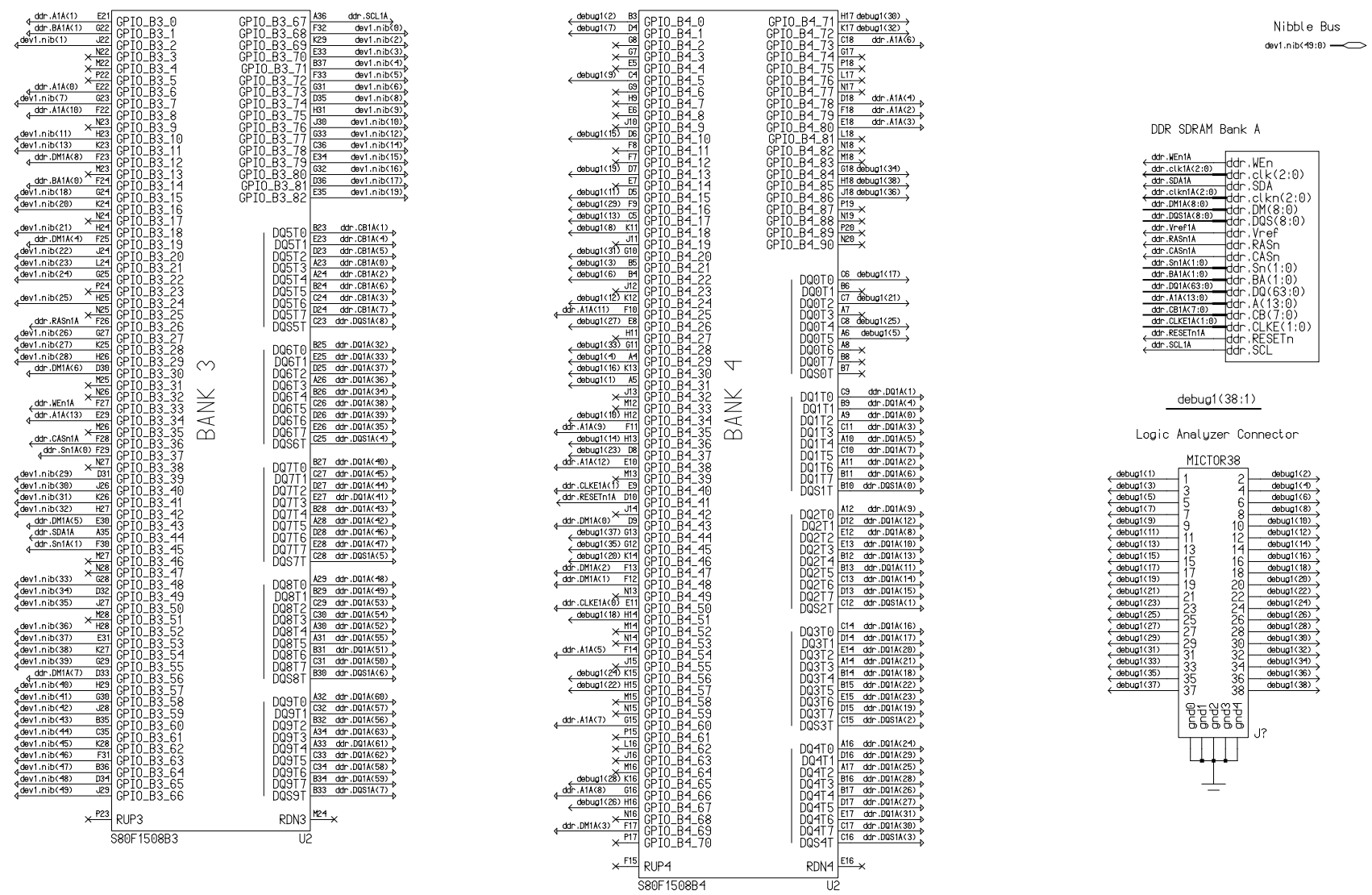
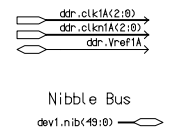
University of Toronto



Development FPGA 1 Banks 1 and 2



Development FPGA 1 Banks 3 and 4

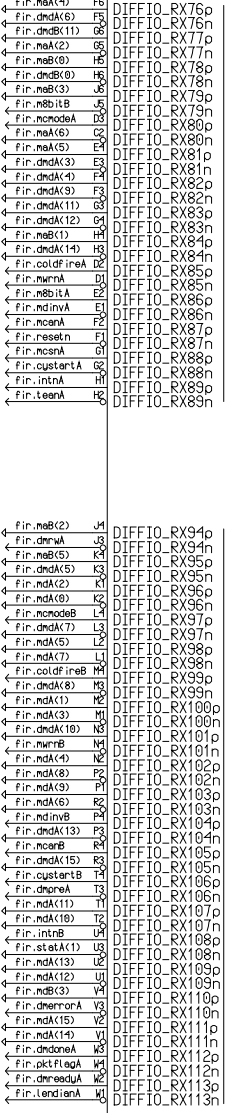
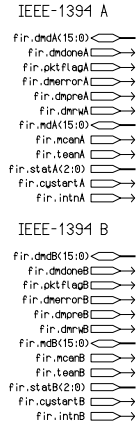


TM-4

Urbana
University of Illinois

Development FPGA 1 Banks 5 and 6

LVDS
 lvds0to1p(9:0)
 lvds0to1n(9:0)



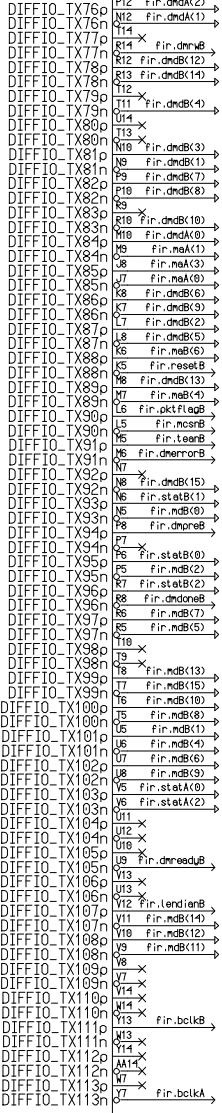
PLL10 Low Speed RX (14)

PLL10 Low Speed TX (8)

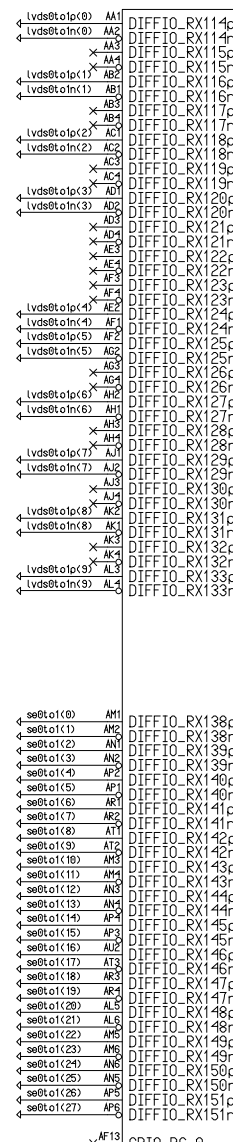
BANK 5

PLL10 Highspeed TX (20)

PLL4 Low Speed TX (10)



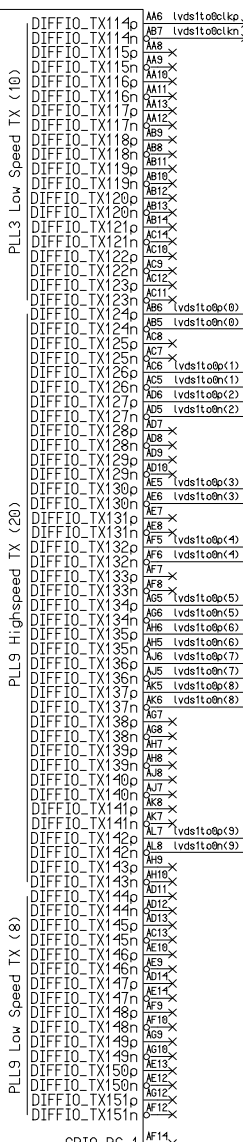
U2



PLL3 Highspeed RX (20)

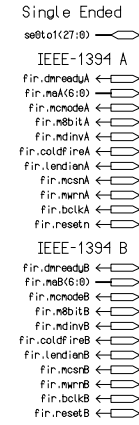
BANK 6

PLL5 Highspeed TX (20)



U2

LVDS
 lvds1to0p(9:0)
 lvds1to0n(9:0)
 lvds1to0clkp
 lvds1to0clkn



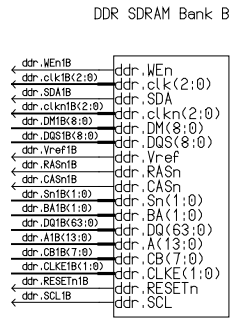
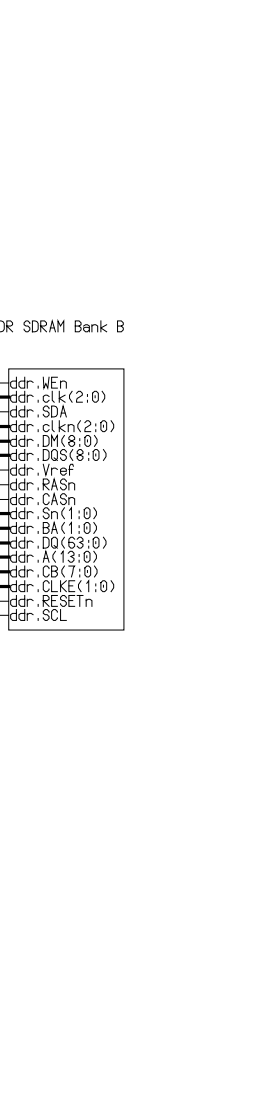
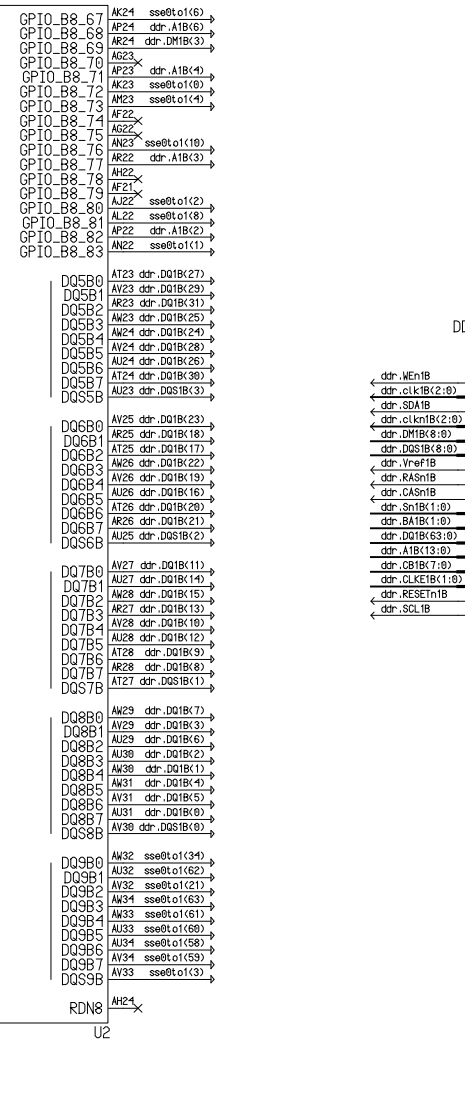
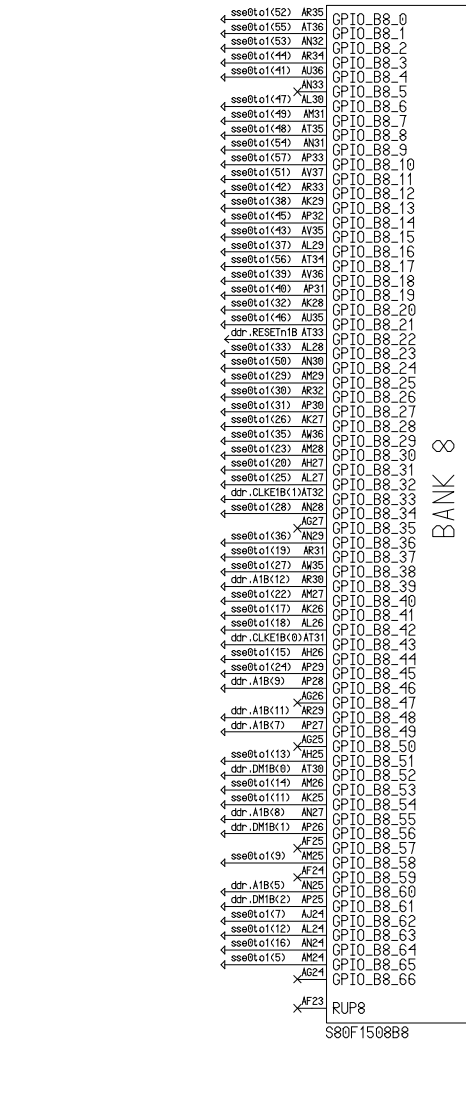
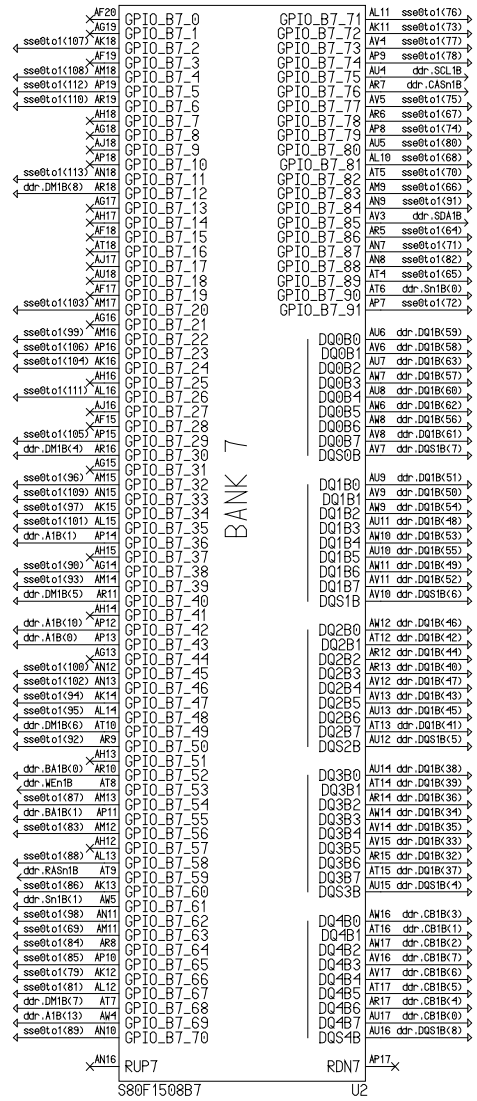
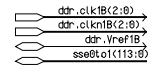
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S80F1508B6

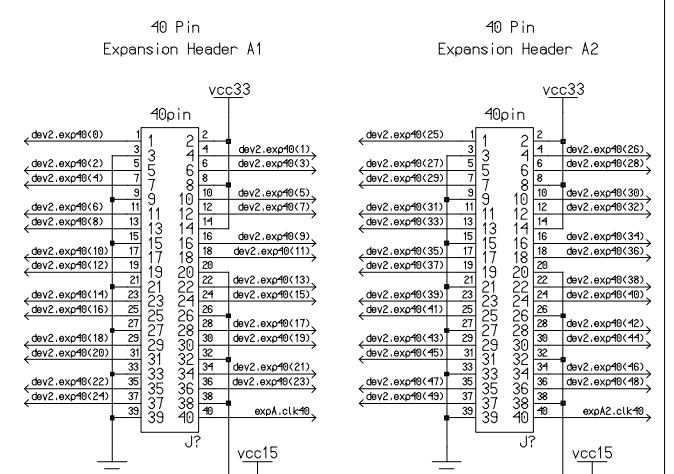
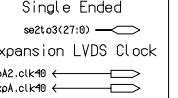
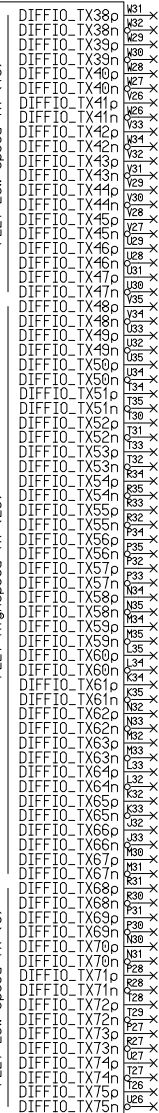
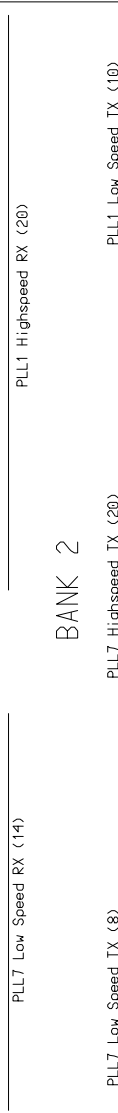
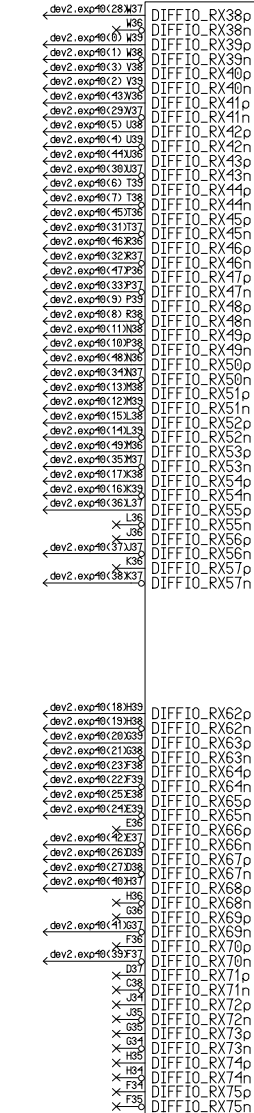
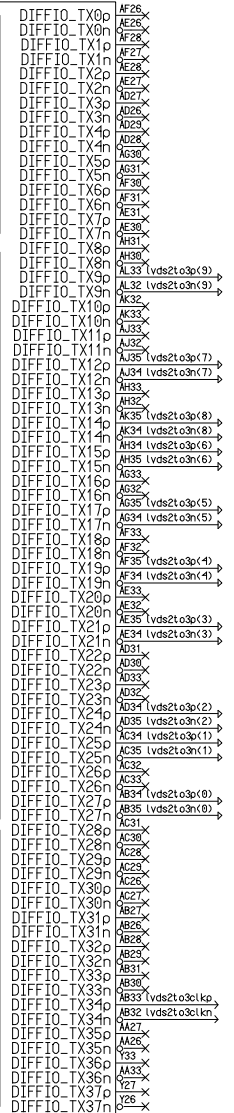
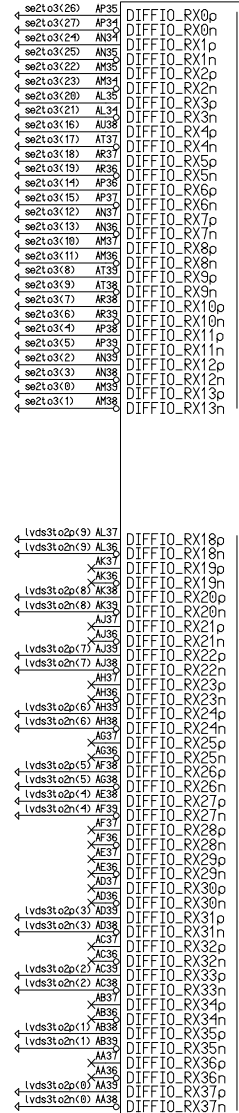
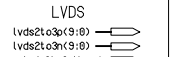
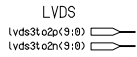
TM-4

JSTAR
University of Hiro

Development FPGA 1 Banks 7 and 8



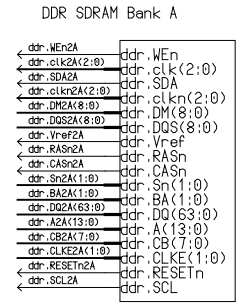
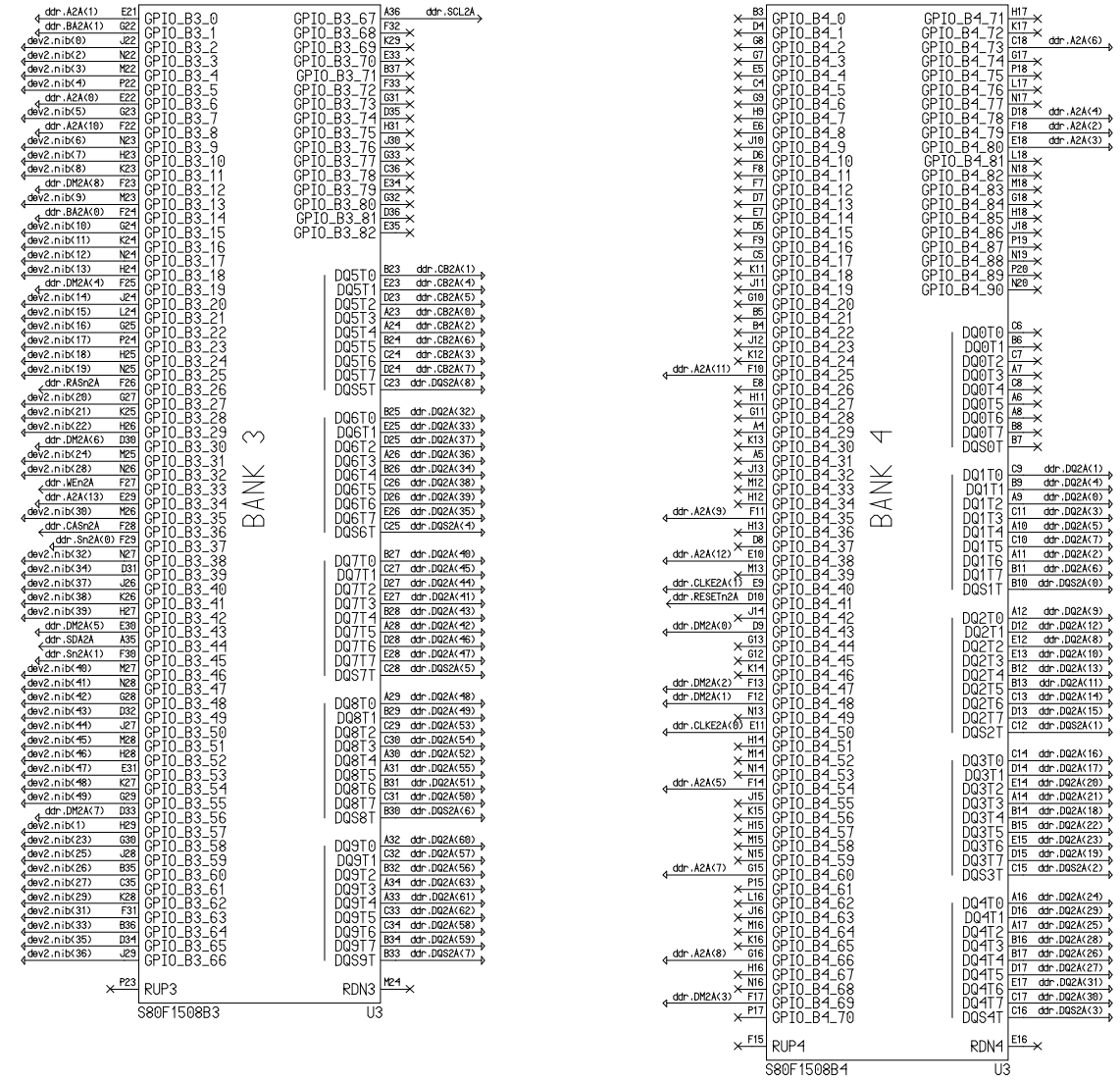
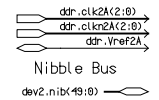
Development FPGA 2 Banks 1 and 2



TM-4

Urbair
University of Toronto

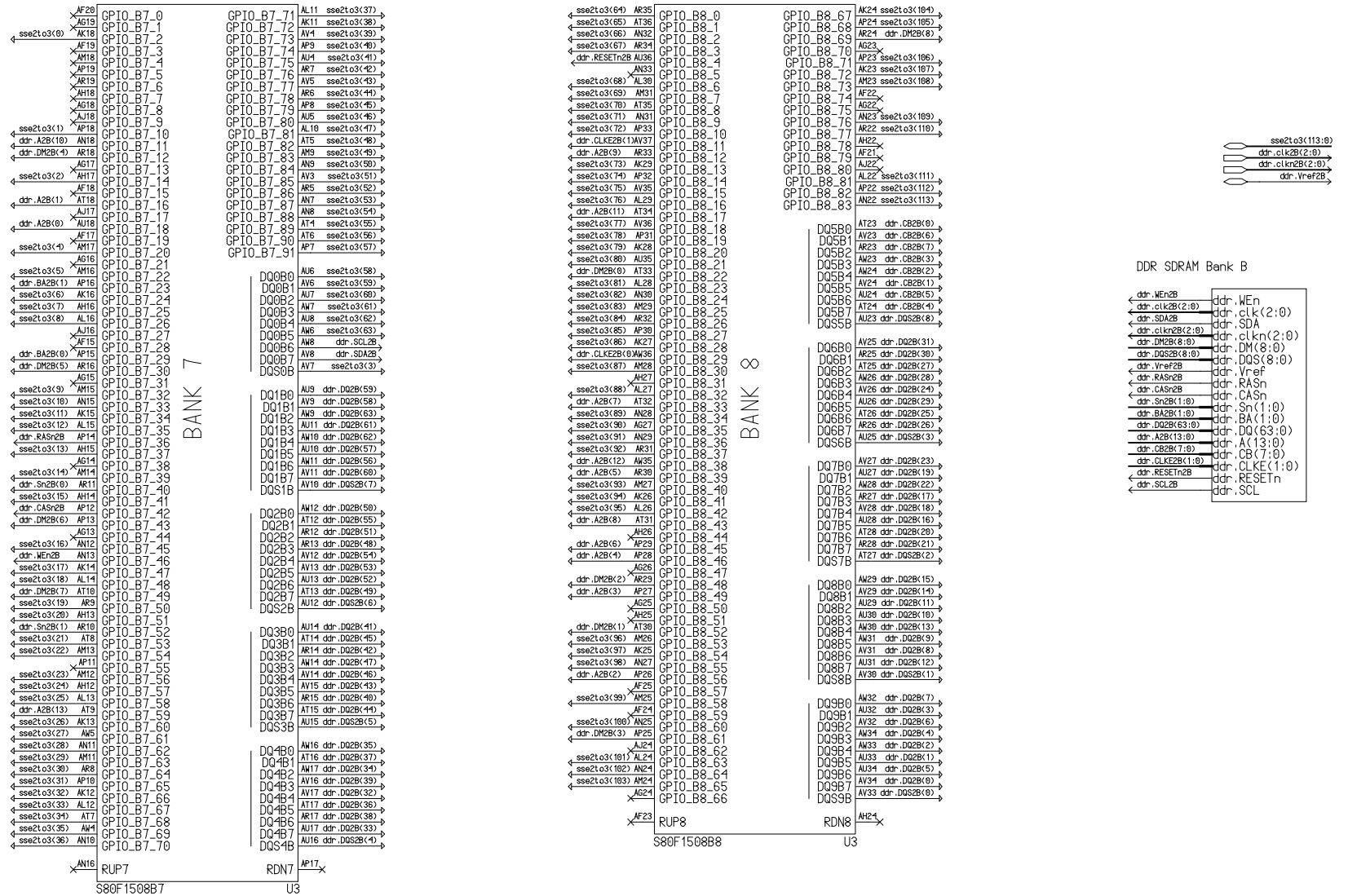
Development FPGA 2 Banks 3 and 4



TM-4

Ulsan
University of Education

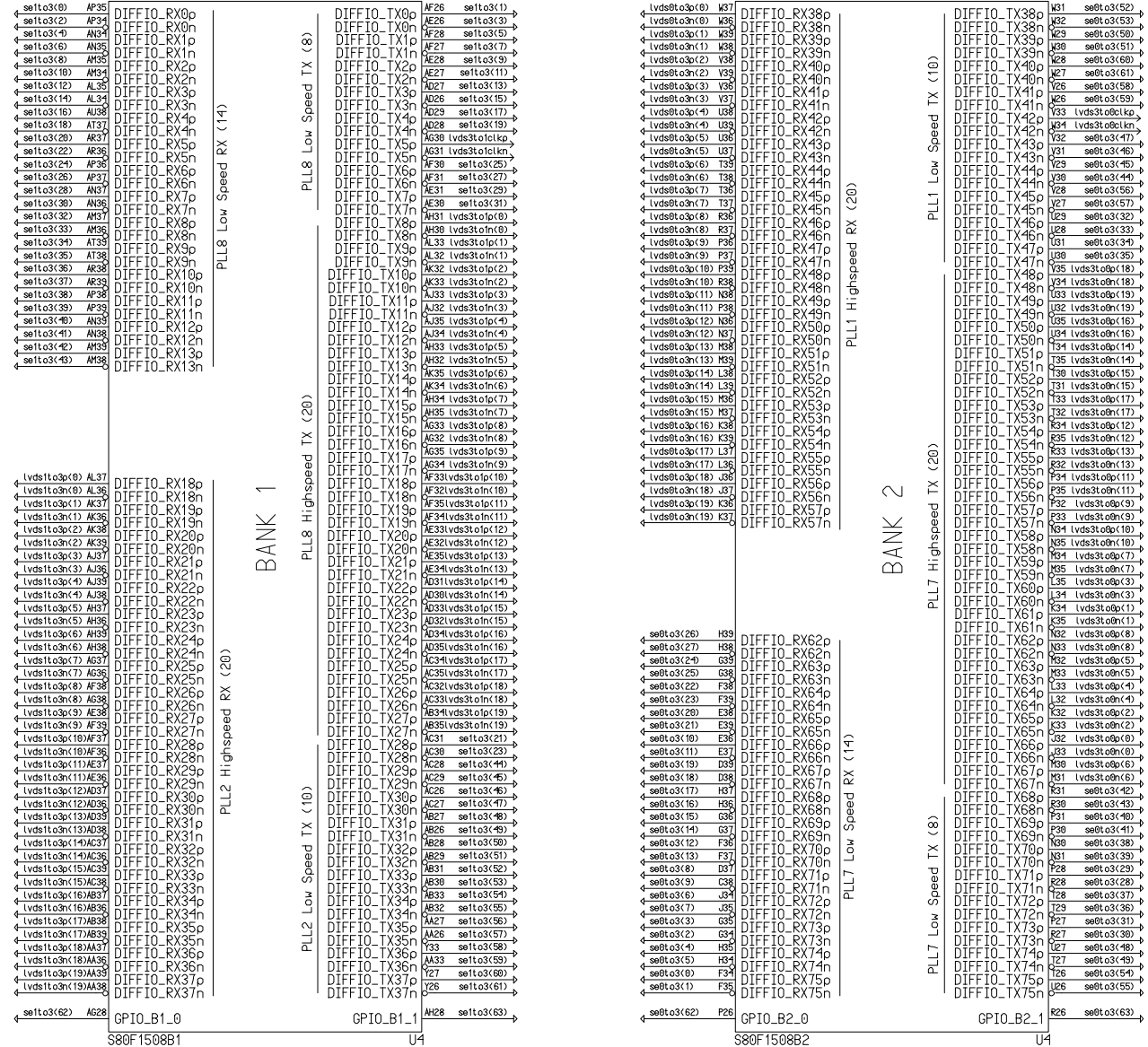
Development FPGA 2 Banks 7 and 8



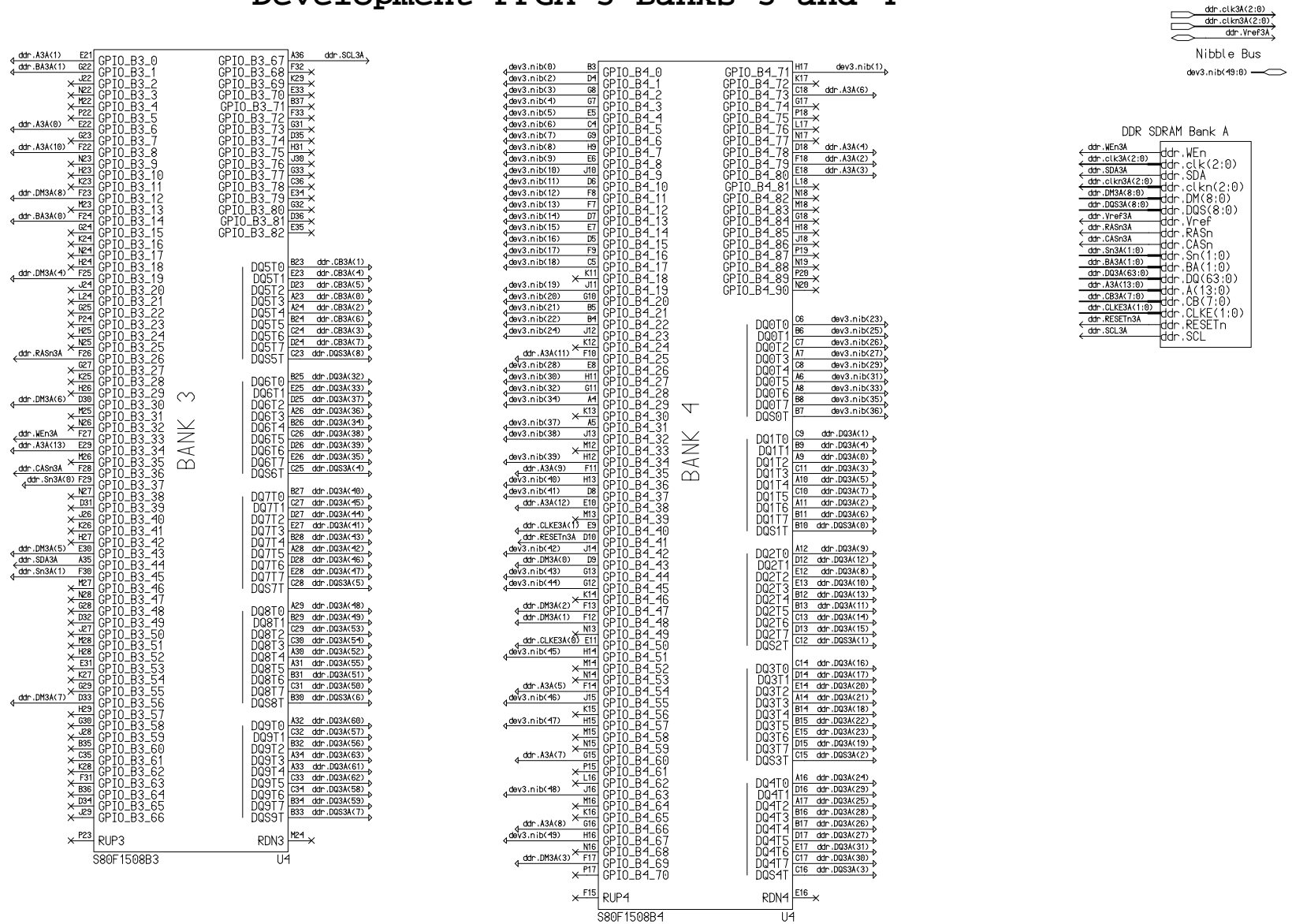
Development FPGA 3 Banks 1 and 2

LVDS
 lvds1to3p(19:0)
 lvds1to3n(19:0)
 lvds8to3p(19:0)
 lvds8to3n(19:0)

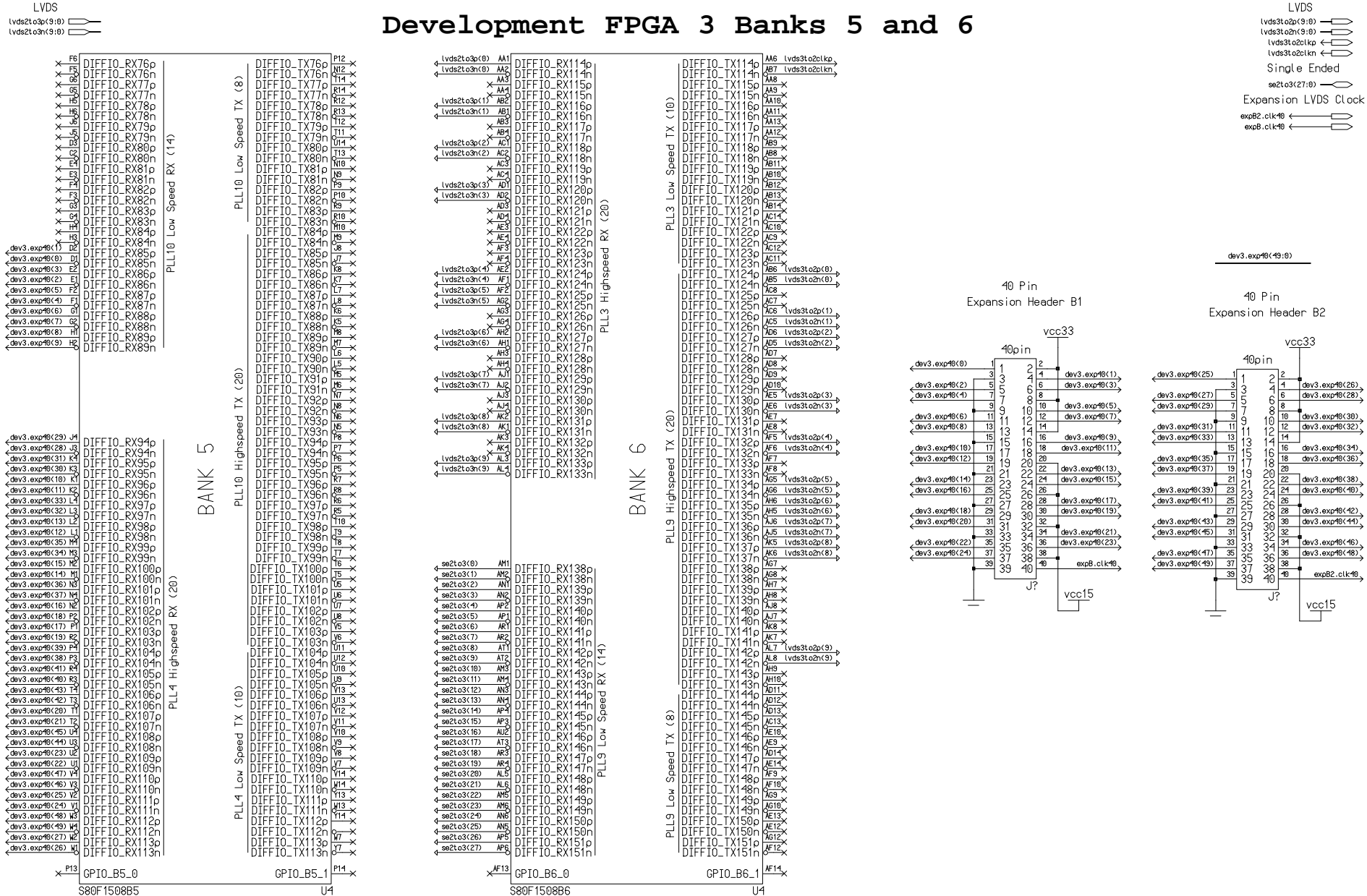
LVDS
 lvds3to1p(19:0)
 lvds3to1n(19:0)
 lvds3to0n(19:0)
 lvds3to0i(19:0)
 lvds3to1ci(19:0)
 lvds3to1cn(19:0)
 lvds3to1cl(19:0)
 lvds3to1cn(19:0)
 Single Ended
 se0to3(63:0)
 se1to3(63:0)



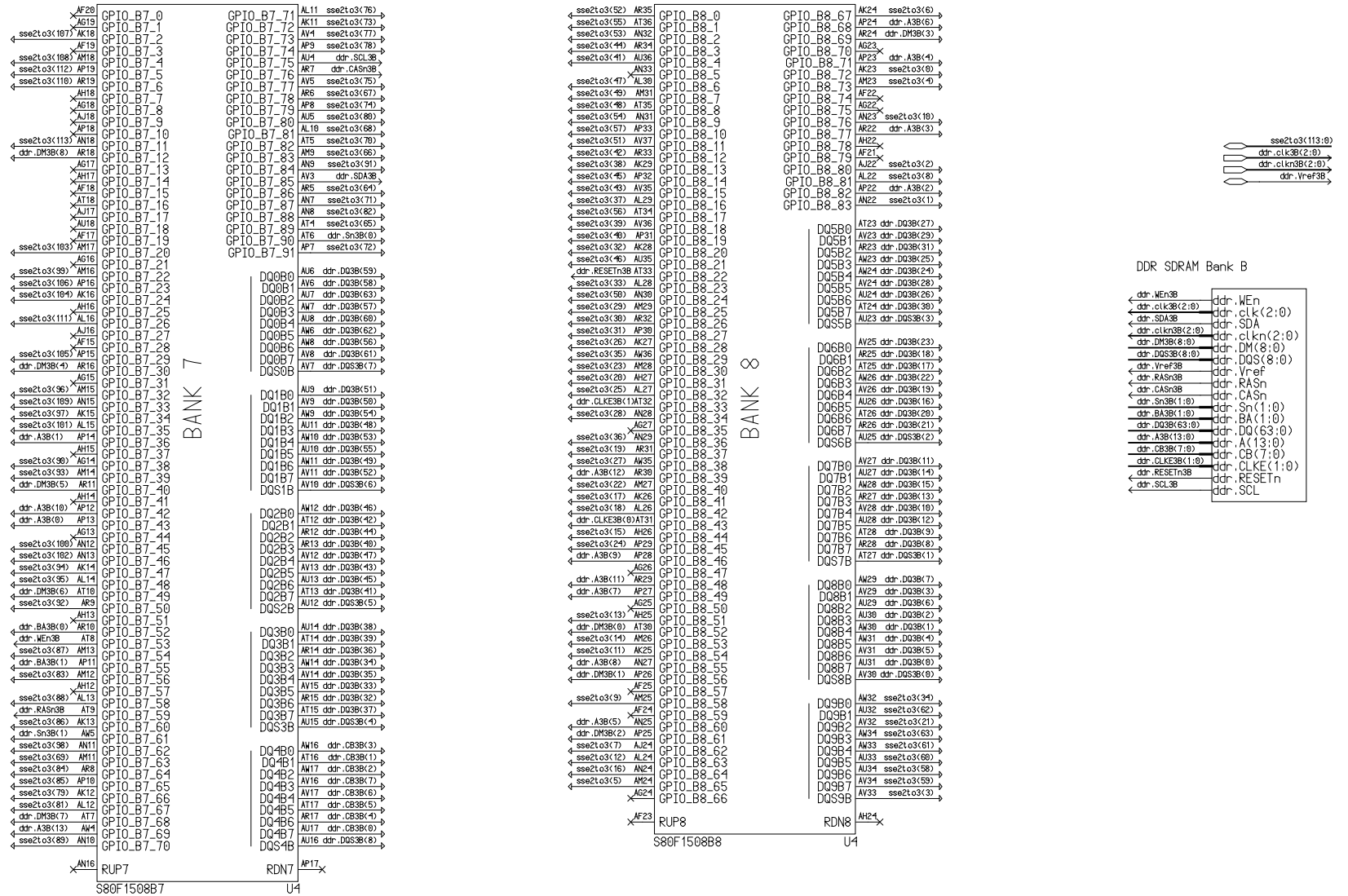
Development FPGA 3 Banks 3 and 4



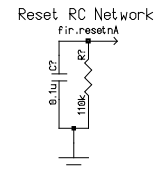
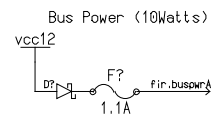
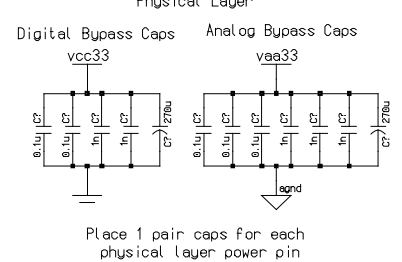
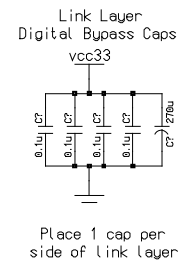
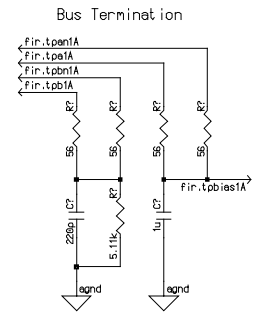
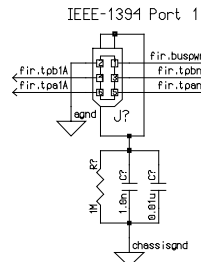
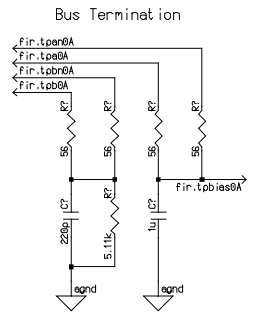
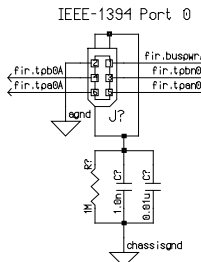
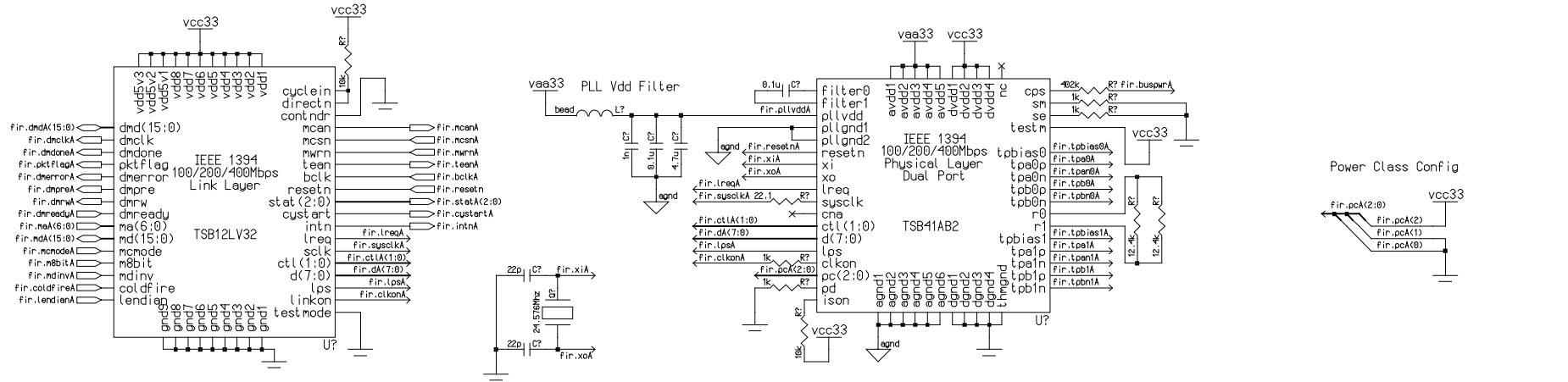
Development FPGA 3 Banks 5 and 6



Development FPGA 3 Banks 7 and 8



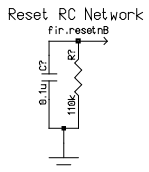
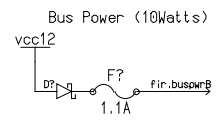
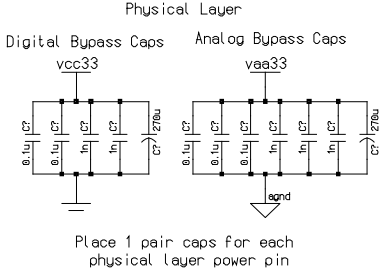
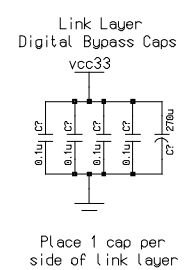
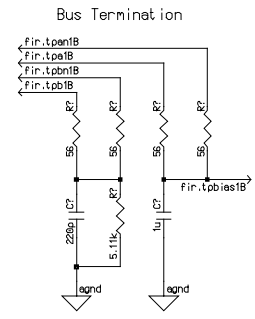
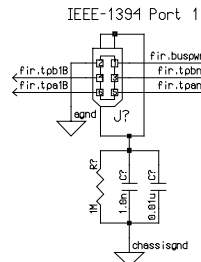
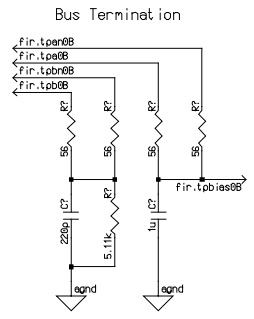
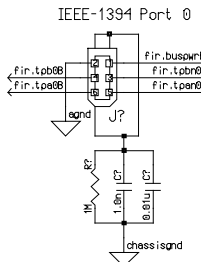
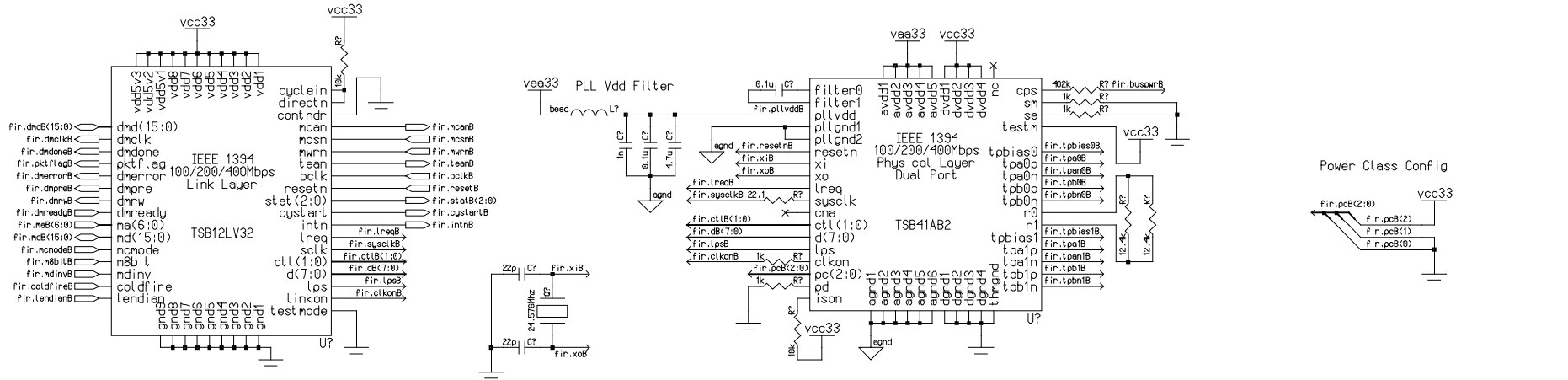
IEEE-1394 (Firewire) Channel A



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Star University of Toronto

IEEE-1394 (Firewire) Channel B

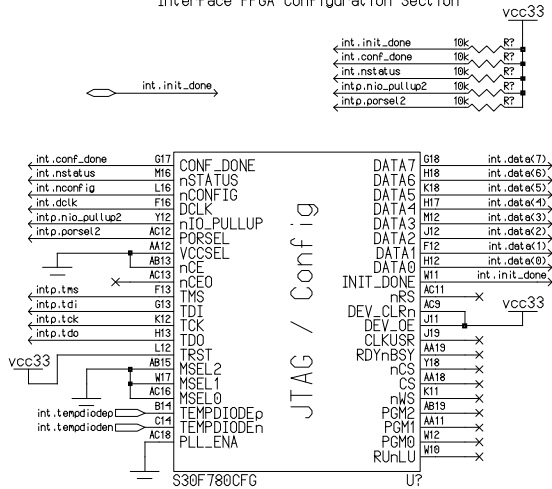


TM-4

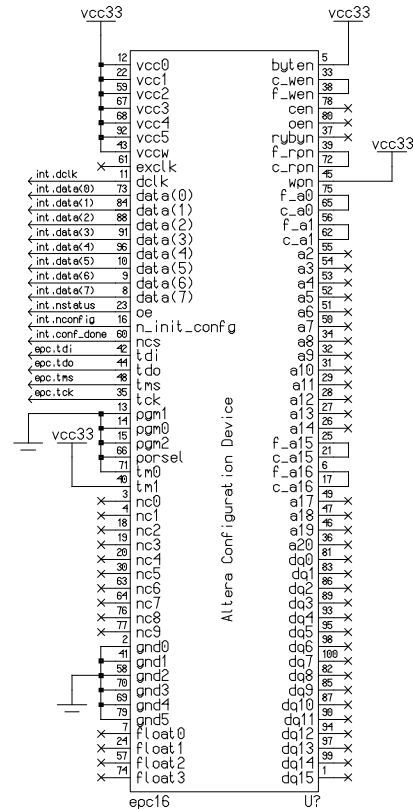
Texas Instruments

Interface FPGA Device Configuration

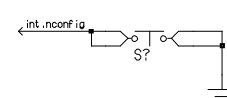
Interface FPGA Configuration Section



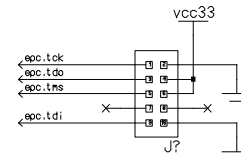
Enhanced Configuration Device and JTAG Connector



Interface FPGA Reset

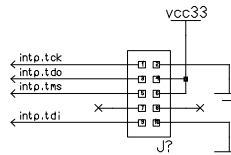


JTAG/Master Blaster Programming Header

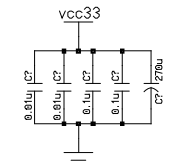


JTAG/Master Blaster Programming Header

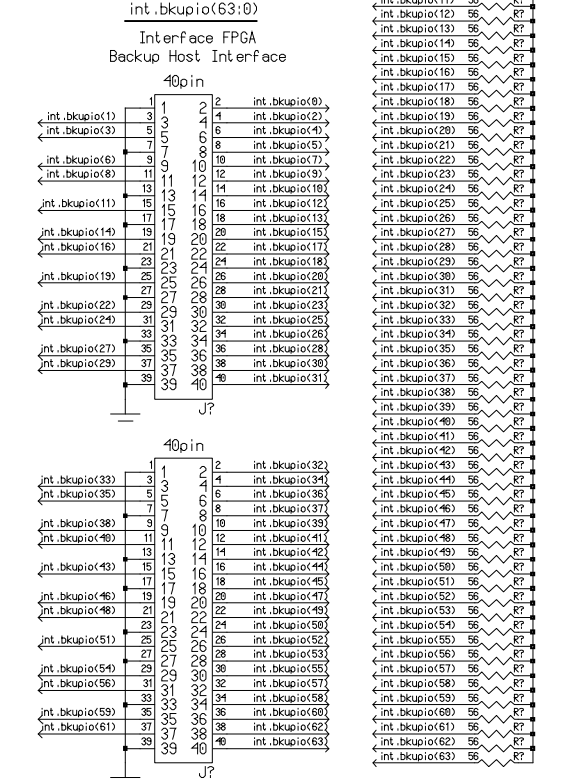
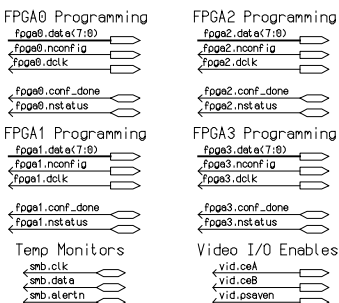
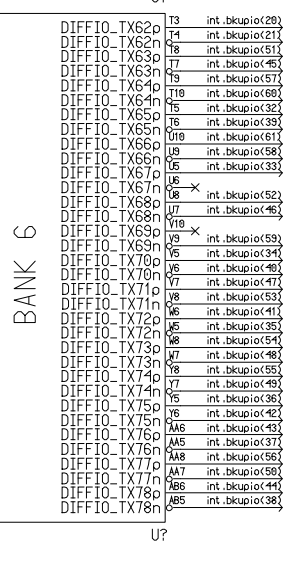
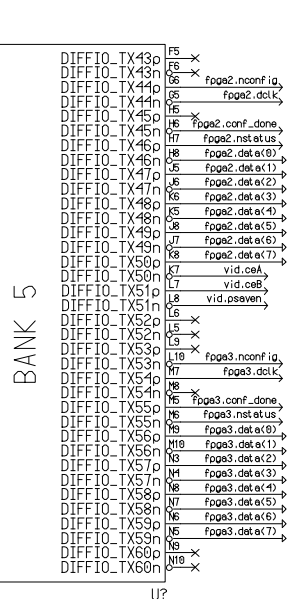
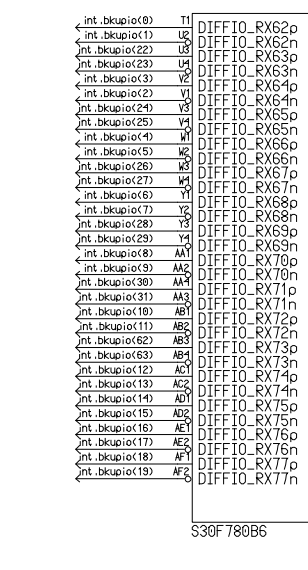
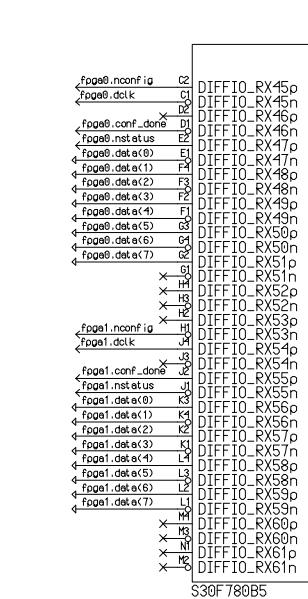
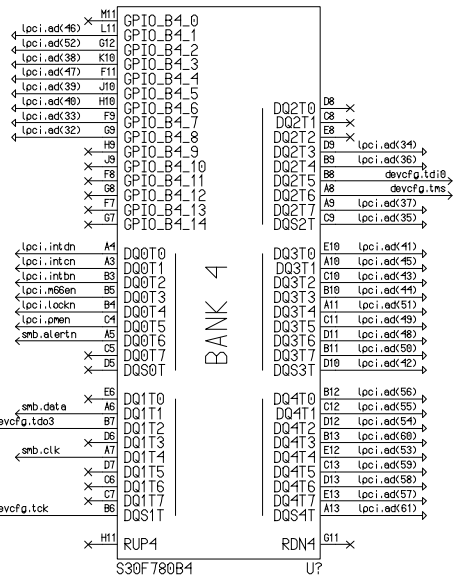
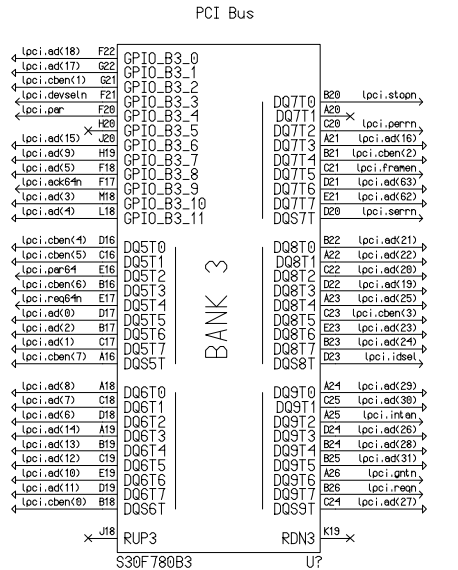
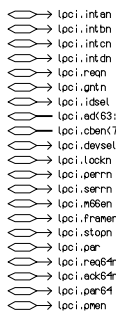
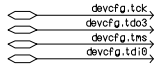
JTAG/Master Blaster Programming Header




EPC Bypass Capacitors



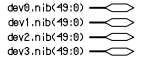
Interface FPGA IO Banks (PCI & Device Programming)



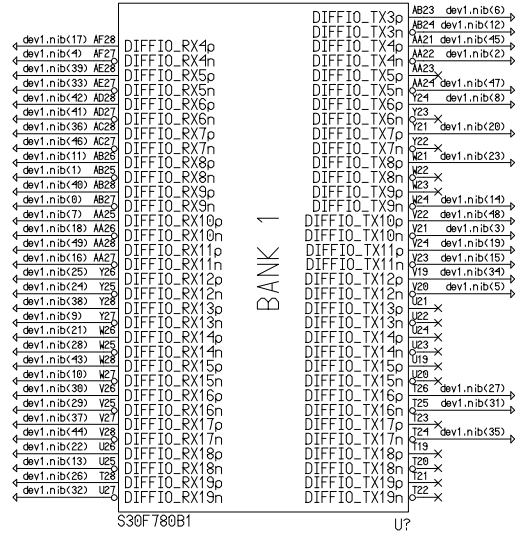
Dipswitches
int_dip(7:0) 

Interface FPGA "Nibble" Bus IO

Nibble Bus

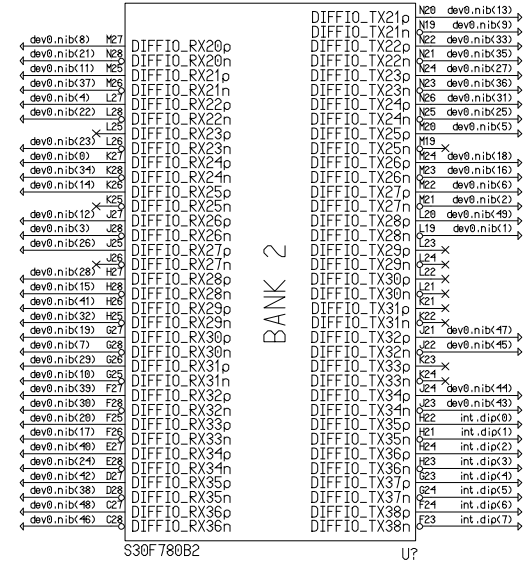


"Nibble" Bus for Dev FPGA 1





BANK 1

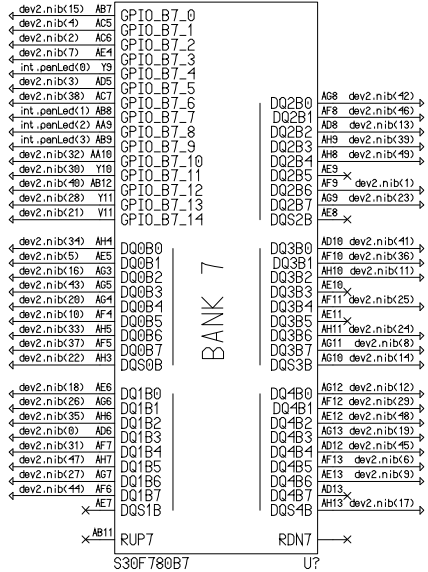
"Nibble" Bus for Dev FPGA 0



BANK 2

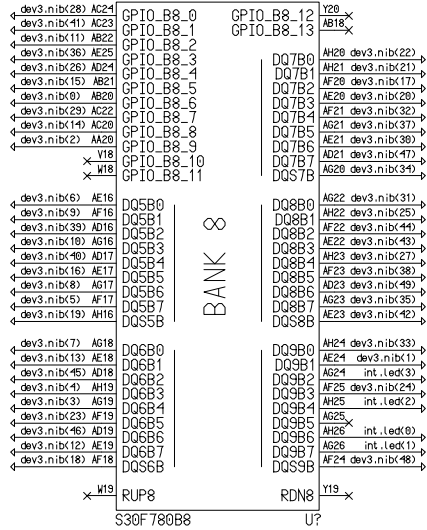
Panel LEDs
int_panLed(3:0) 
PCB LEDs
int_led(3:0) 

"Nibble" Bus for Dev FPGA 2



BANK 7

"Nibble" Bus for Dev FPGA 3

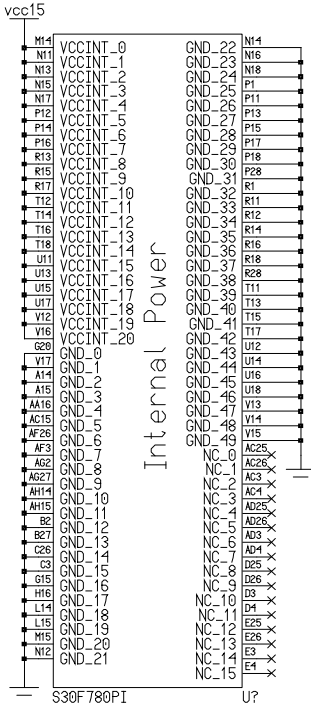
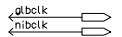
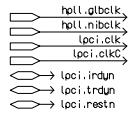


BANK 8

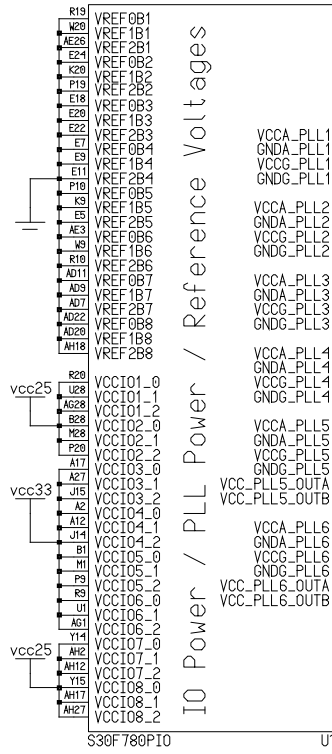
TM-4

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University of Illinois

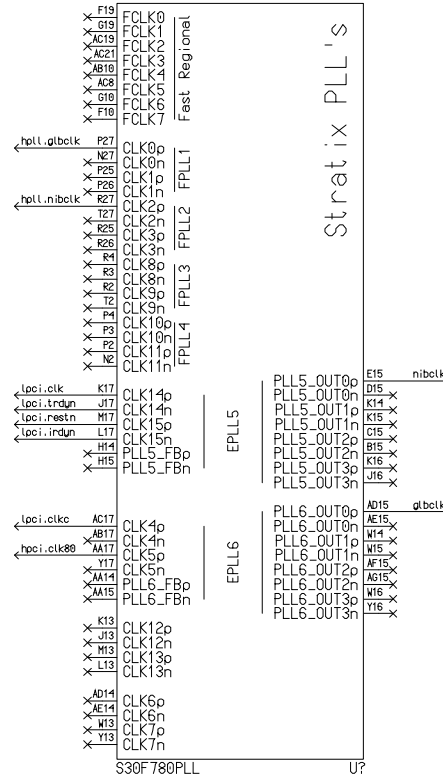
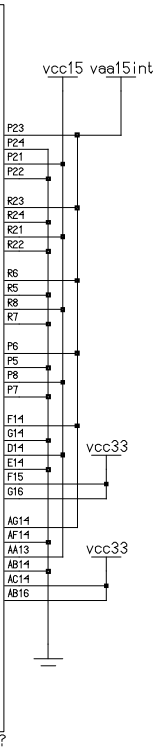
Interface FPGA Power & PLLs



Internal Power

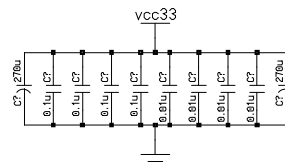


IO Power / PLL Power / Reference Voltages

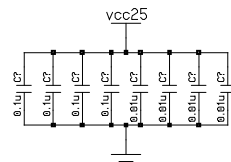


Stratix PLL's

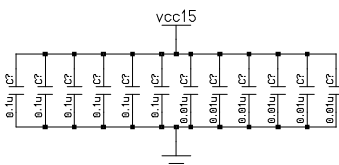
Interface FPGA vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side
Banks 3,4,5 and 6



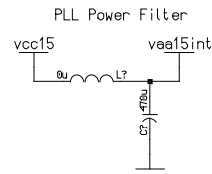
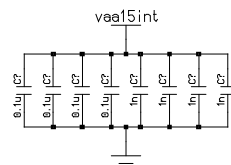
Interface FPGA vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side
Banks 1,2,7 and 8



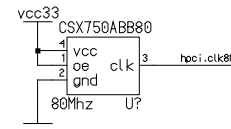
Interface FPGA Vccint Bypass Caps 0603
Place near center of FPGA bottom side



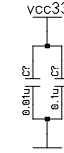
Interface FPGA Vcca_pll Bypass Caps 0603
Place pair by each of 5 power pin groups



Global Clock Reference



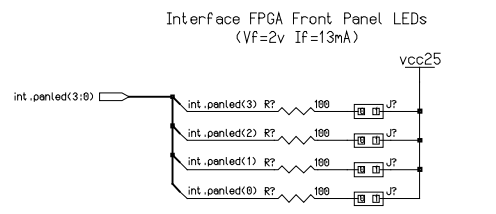
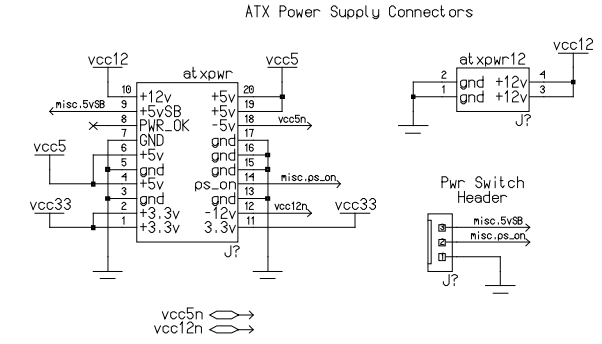
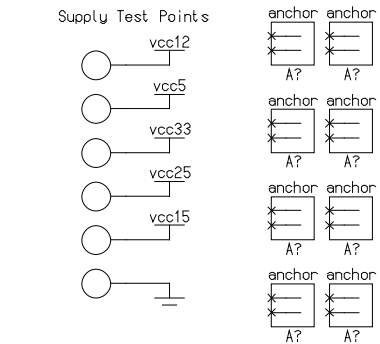
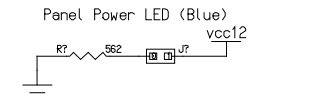
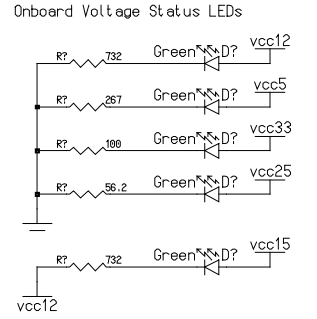
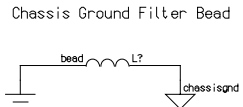
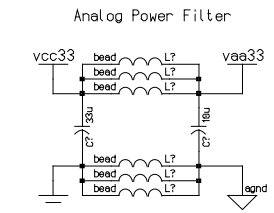
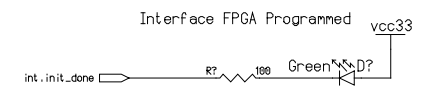
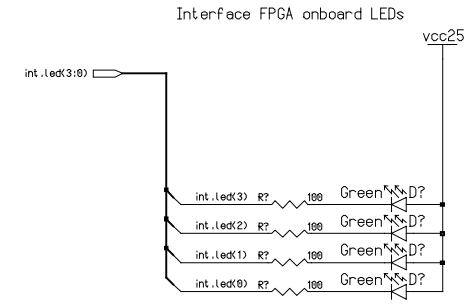
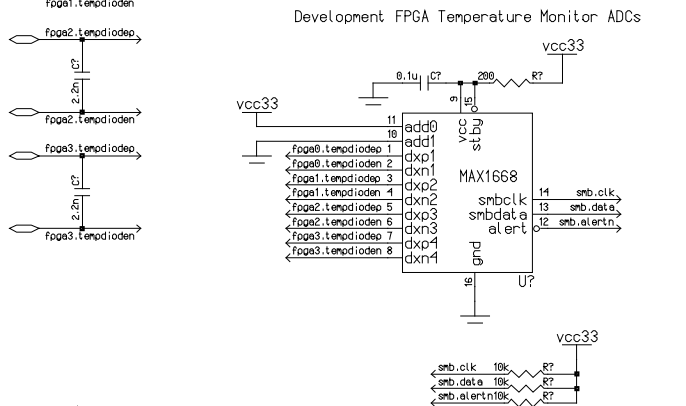
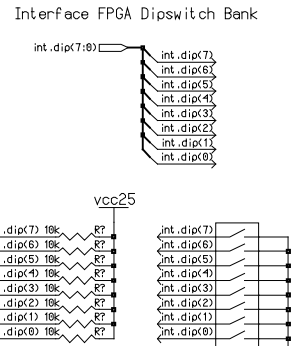
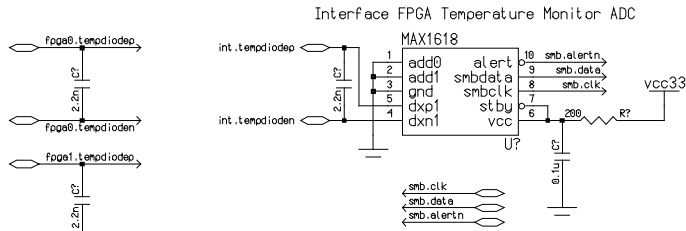
Global Reference Bypass



TM-4

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Miscellaneous Circuits



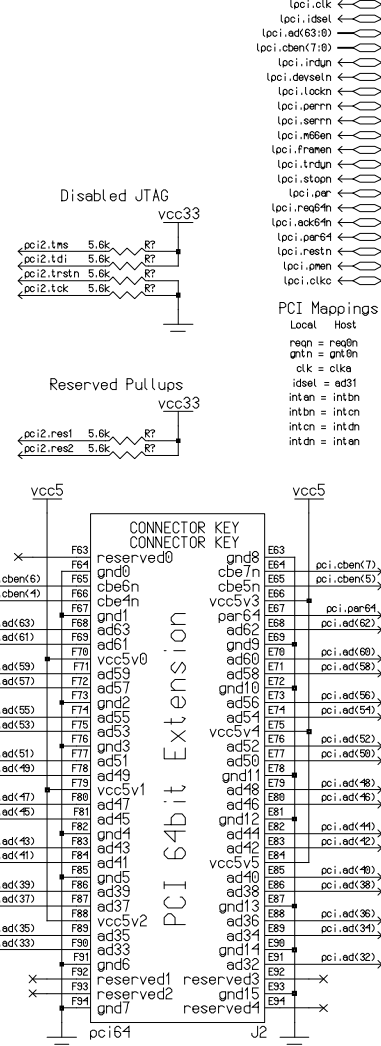
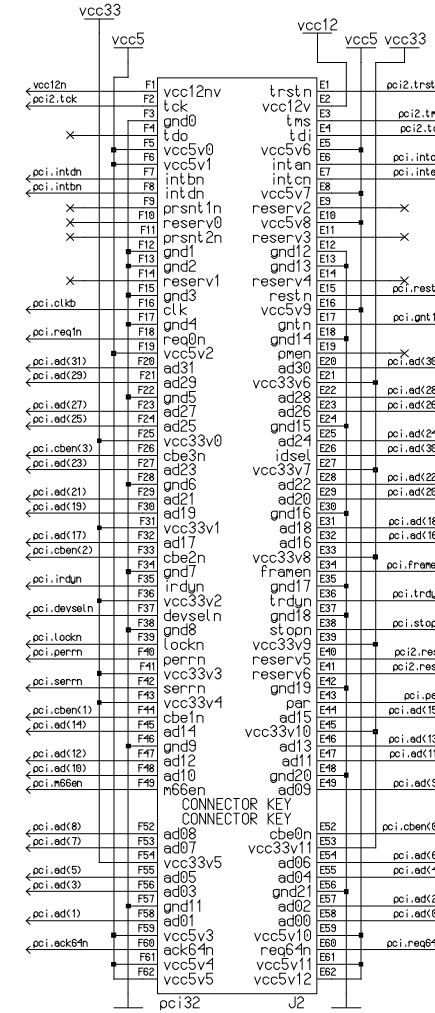
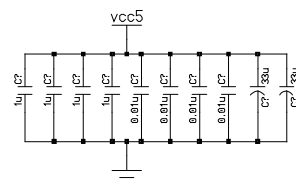
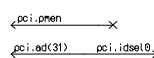
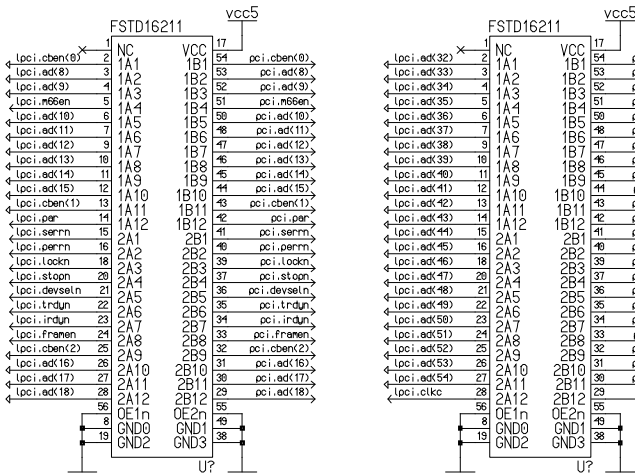
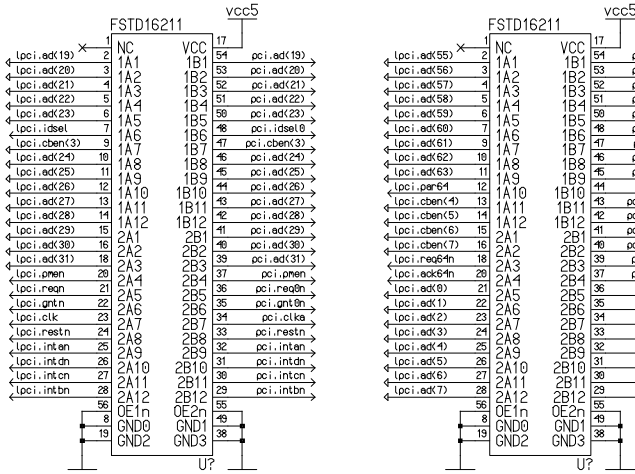
TM-4

State
University of Ohio

PCI Expansion Slot and Interface FPGA Voltage Converters

- pci.intan
- pci.intbn
- pci.intcn
- pci.intdn
- pci.reg0n
- pci.reg1n
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- pci.reg96n
- pci.reg97n
- pci.reg98n
- pci.reg99n

PCI 5v -> 3.3v Level Shifter



TM-4

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Single Board Computer and PCI

vcc5n ↔
vcc12n ↔

