Manage Performance & Power Using 40-nm FPGAs

Seyi Verma
Vaughn Betz

Agenda

- **Design requirements**
- **Stratix® IV FPGAs: Highest performance and lowest power**
  - Processing techniques
  - Architectural innovations
  - Quartus® II software CAD system
- **High-end FPGA competitive comparison**

ALTERA®

Design Requirements

Designer Goals	What You Need From Your FPGA	What You Need From Your FPGA Software
Functionality	High density	■ Ease of use ■ Maximum utilization ■ Low compile times
Meet timing constraints	High performance	■ Detailed constraint entry ■ Powerful timing analysis tool ■ Optimization of all timing requirements
Meet power budget	Low power	■ Automatic power optimization ■ Accurate power analysis/reports

Maximize performance and minimize power

ALTERA®

Stratix IV High-End FPGA Highlights

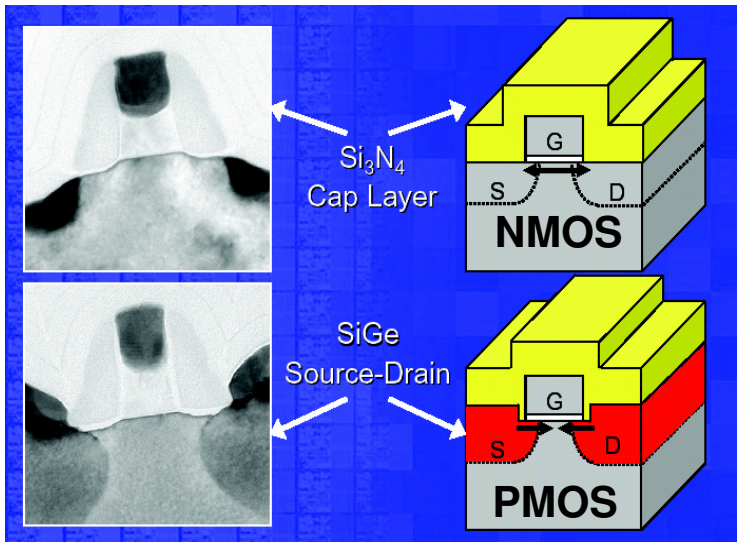
Stratix IV FPGAs

- Highest density
  - Up to 680K LEs
  - Up to 22.4-Mbits internal RAM
  - Up to 1,360 18x18 multipliers
- Highest bandwidth and performance
  - Up to 48 transceiver blocks operating at up to 8.5 Gbps
  - Maximum clock rates of 600 MHz
- Broad protocol support
  - Including hard IP for PCI Express Gen1 and Gen2
- Lowest power
  - 40-nm process benefits including 0.9-V core voltage
  - Programmable Power Technology (PPT)
  - Quartus II PowerPlay technology

Managing Performance and Power Through Process Technology

40-nm Process

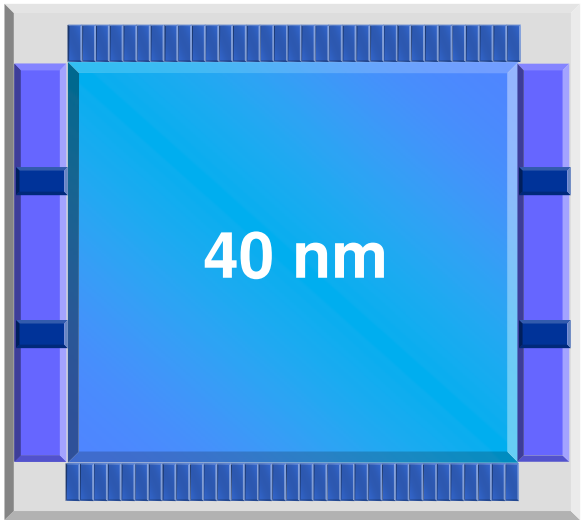
- Aggressive gate length
  - Better density and higher speed than 45 nm
- Second-generation strained silicon
  - Increases electron mobility by up to 30%
  - Transistor level performance is up to 40% higher
- Strained silicon benefit can be converted to
  - Higher speed
  - Lower power (standby and dynamic)



In 40 nm, Altera converts benefits of strain to lower power

ALTERA®

Leading Edge Process Technology at 40 nm



- **Advanced 40-nm process at 0.9 V**
  - Lower voltage → reduces dynamic power by 33%
  - 30% capacitance reduction → reduces dynamic power
  - 39% shorter channel length compared to 65 nm → increases performance
- **Multiple-gate oxide thicknesses (triple oxide)**
  - Trade-off static power vs. speed per transistor
- **Multiple-threshold voltages**
  - Trade-off static power vs. speed per transistor
- **Low-k inter-metal dielectric**
  - Reduces dynamic power, increases performance
- **Super strained silicon**
  - Increases electron and hole mobility by 30%
  - Balance between power and performance
- **Copper interconnect**
  - Increased performance, reduced IR drop

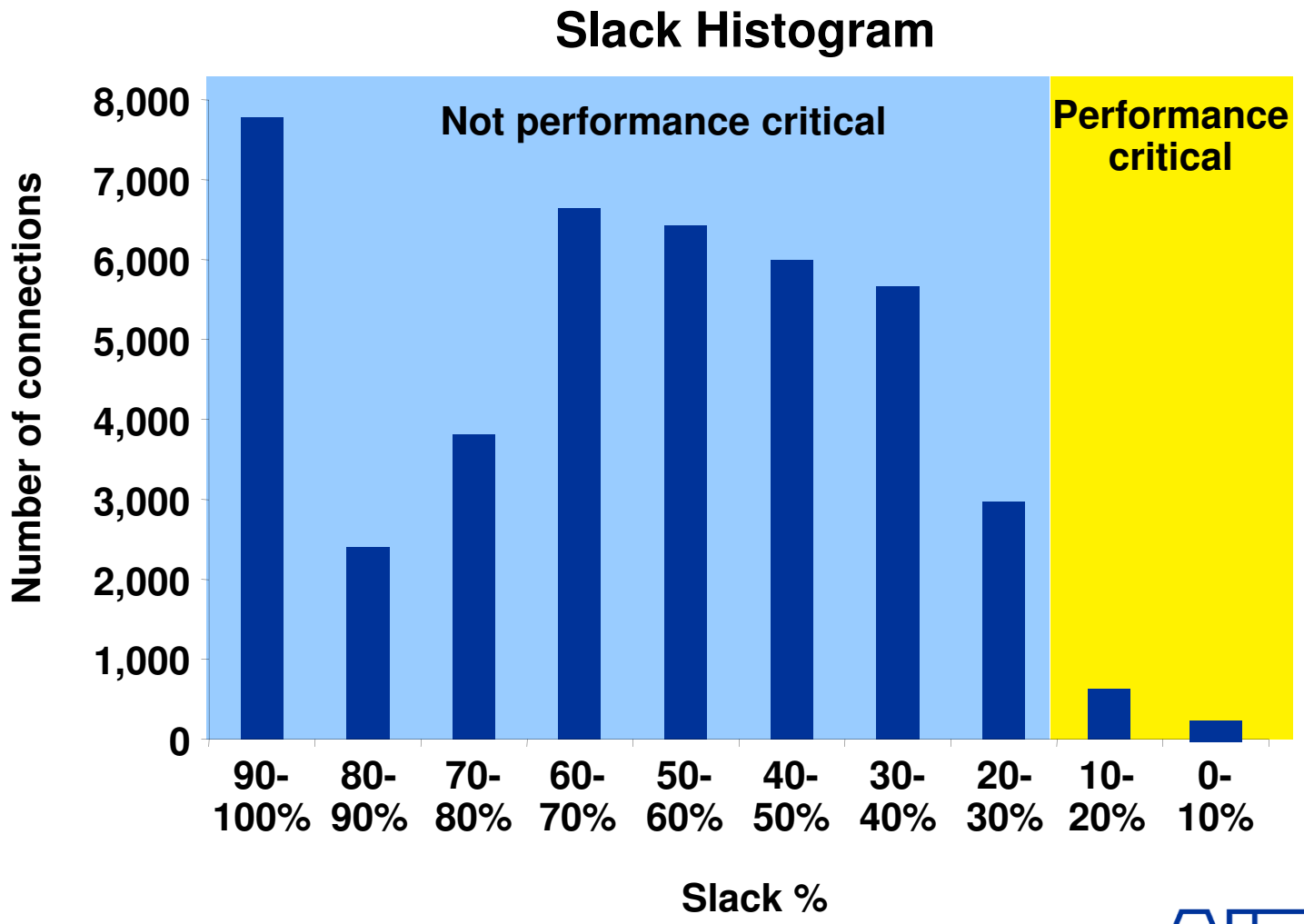
Best-in-class process for power and performance

ALTERA®

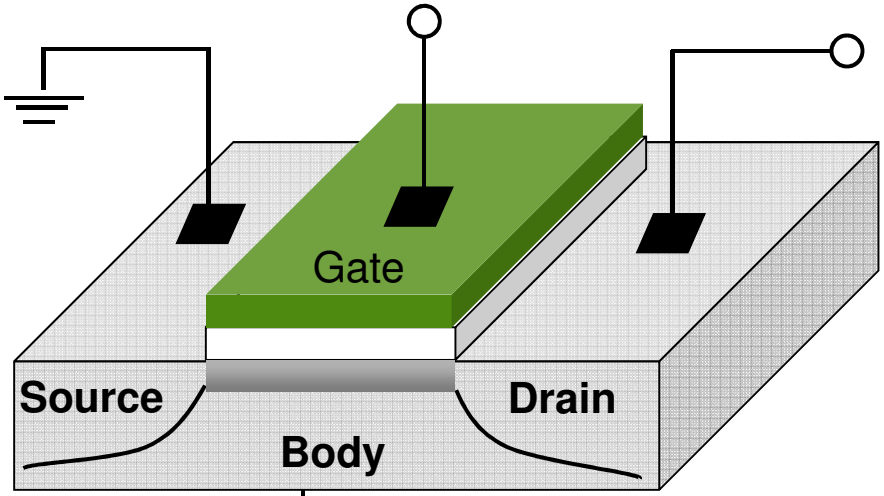
Architecture Innovation:
Better Performance, Reduced Power

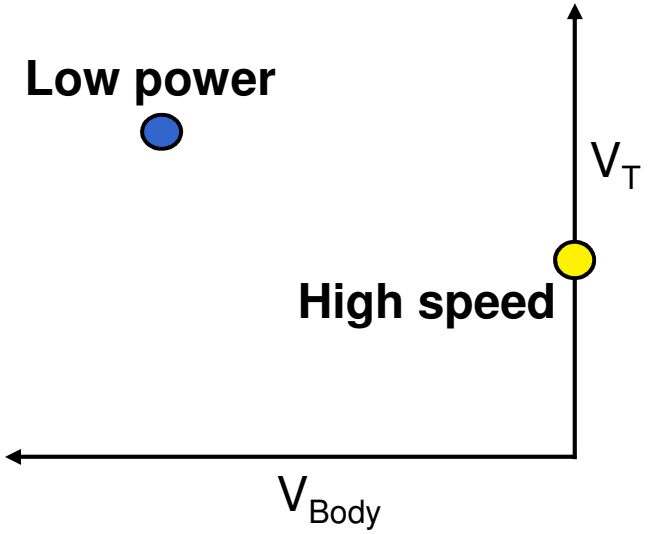
Design-Specific Power Optimization

- Only a small fraction of logic is performance critical



Programmable Speed vs. Leakage





0 V

High speed (HS)

V_{Body} – **Automatically controlled by software**

QUARTUS® II

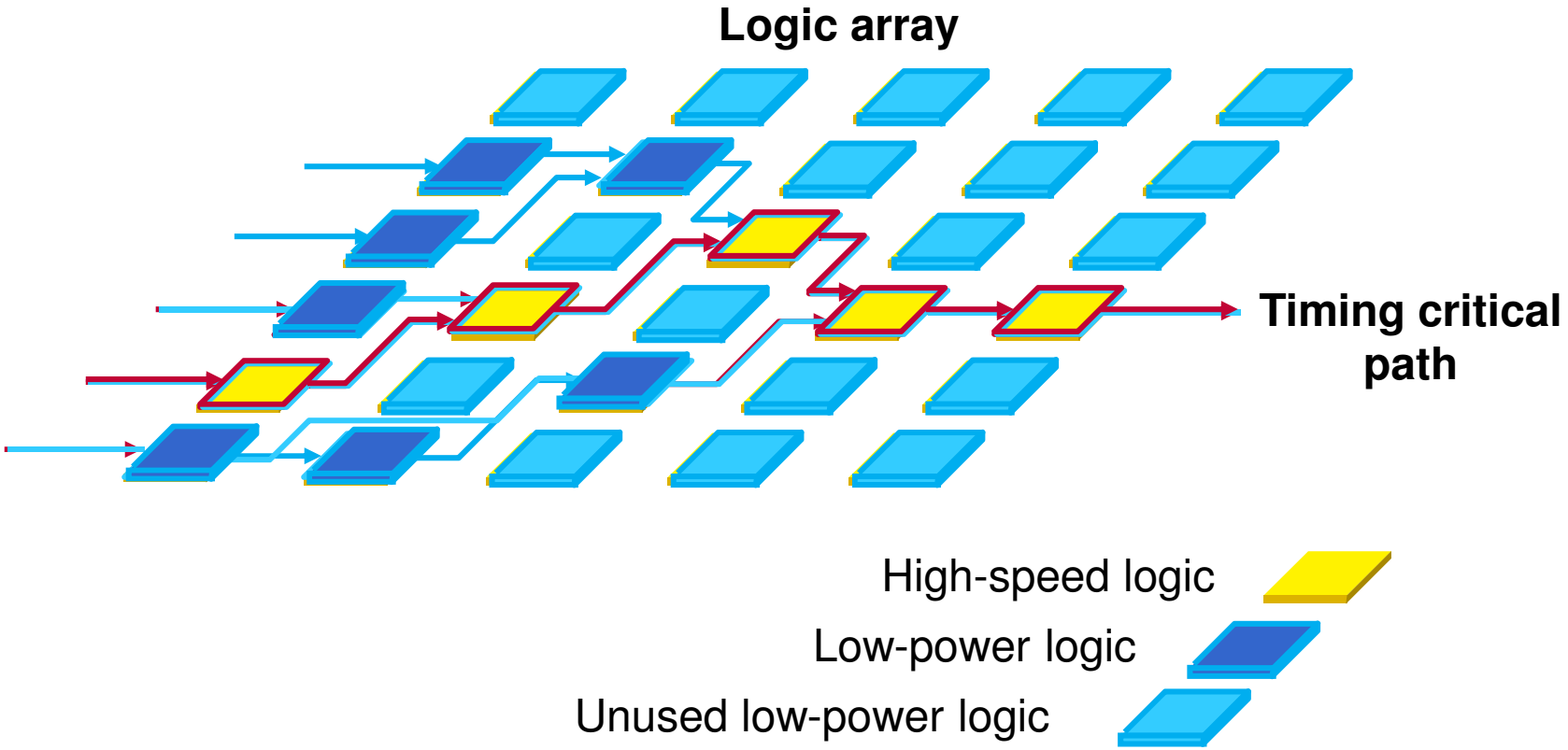
Low power (LP)

< 0 V

Note: A simple "model" showing Programmable Power Technology. Actual implementation varies and is patented.

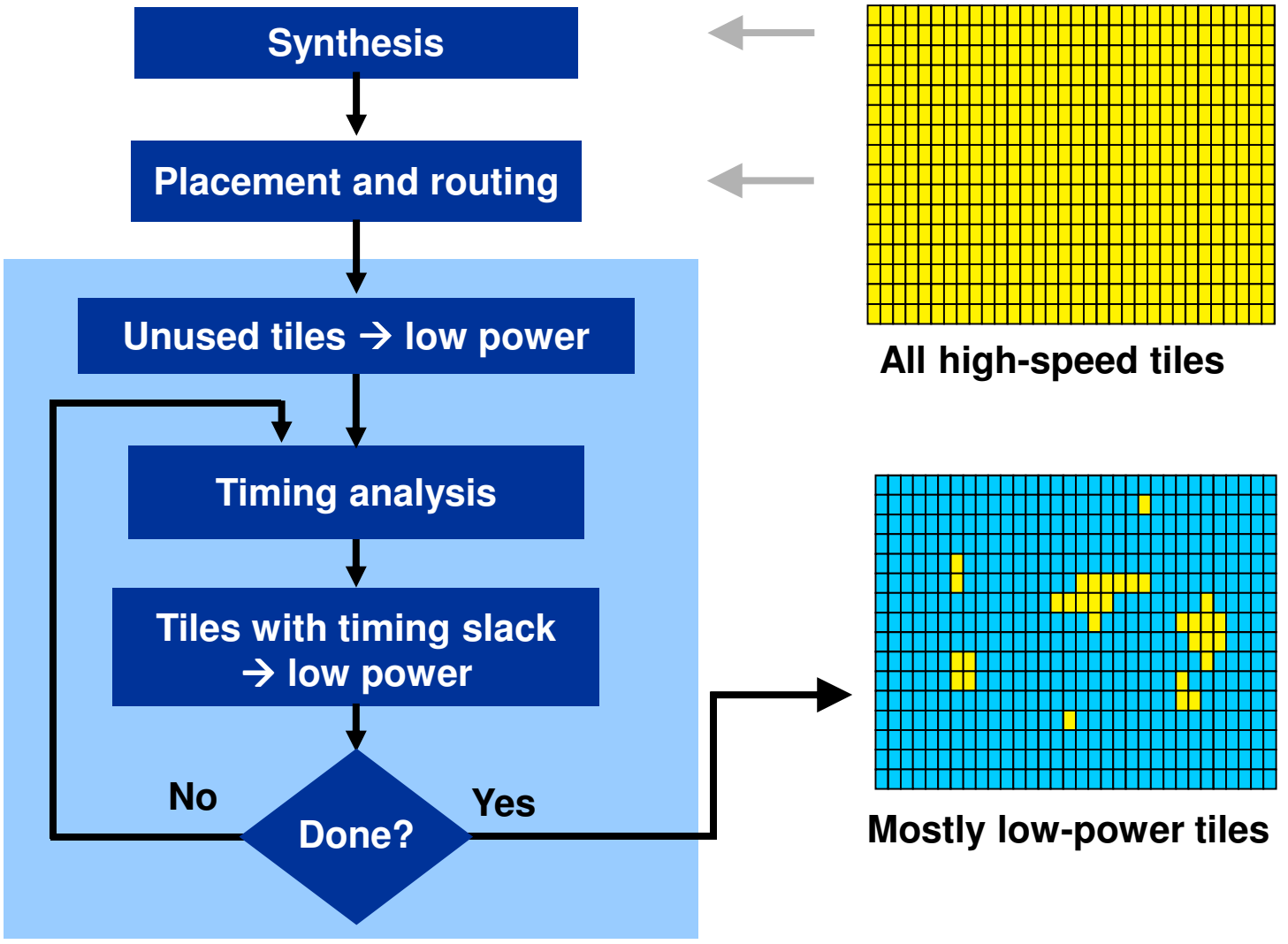
ALTERA®

Programmable Power Technology



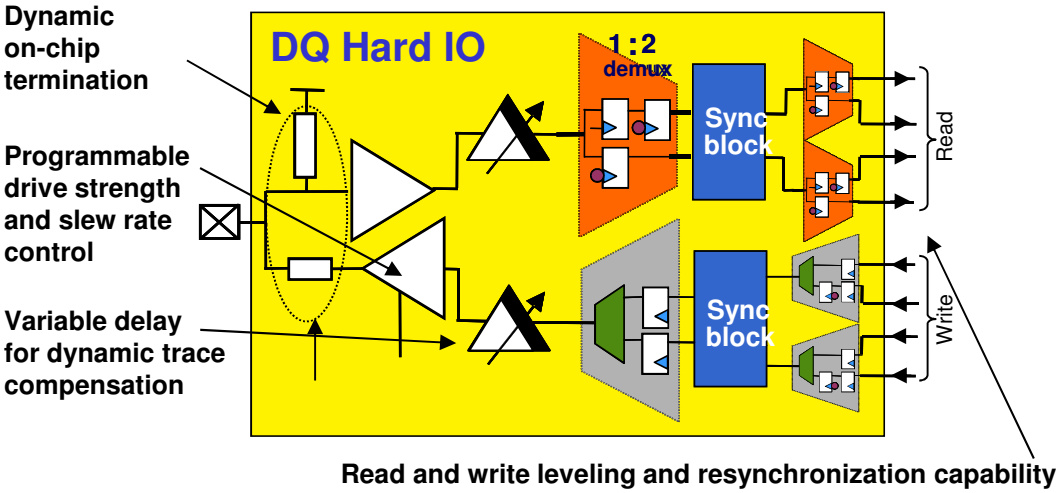
Performance where you need it, lowest power everywhere else

Quartus II Software Automatically Uses PPT



ALTERA®

Stratix IV FPGA DDR3 Support



Interconnect	Performance
DDR3	>533 MHz/1067 Mbps
DDR2	400 MHz/800 Mbps
QDR II	350 MHz
QDR II+	400 MHz
RLDRAM II	400 MHz
LVDS	1.60 Gbps

I/O Feature	Stratix IV FPGAs	Benefit
Dynamic On-Chip Termination (OCT)	✓	Saves power
DDR3 Read/Write Leveling	✓	Required for DIMM support
Variable I/O Delay	✓	Allows signal de-skew

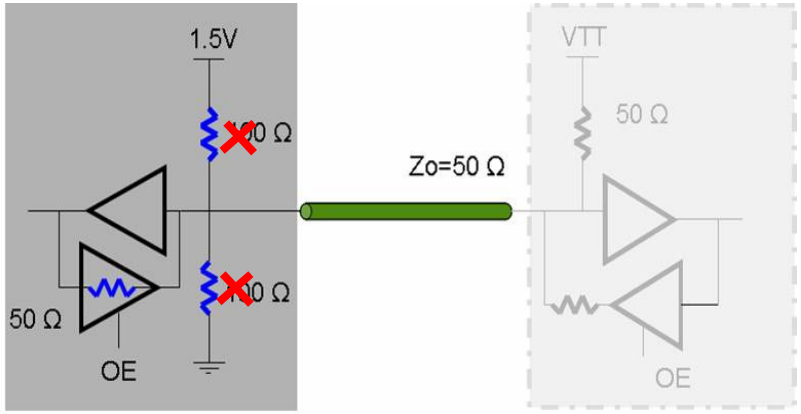
DDR3 DIMM support at 533 MHz through read/write leveling

ALTERA®

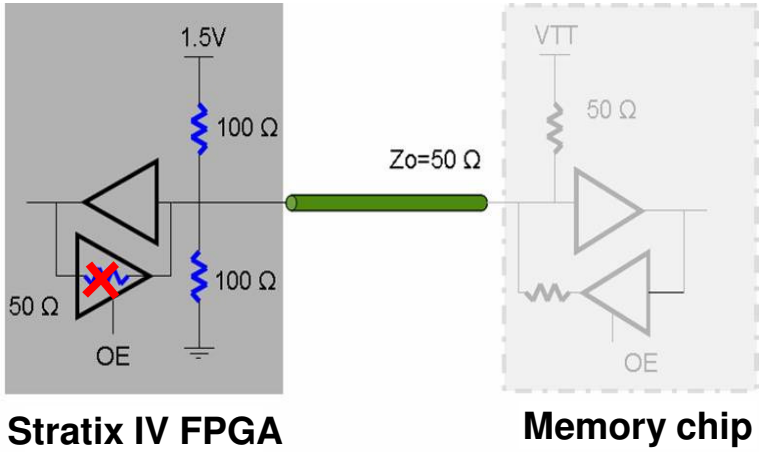
Dynamic OCT

- Write: Rs on, Rt off → Matching line impedance
- Read: Rs off, Rt on → Terminating far end

Write



Read



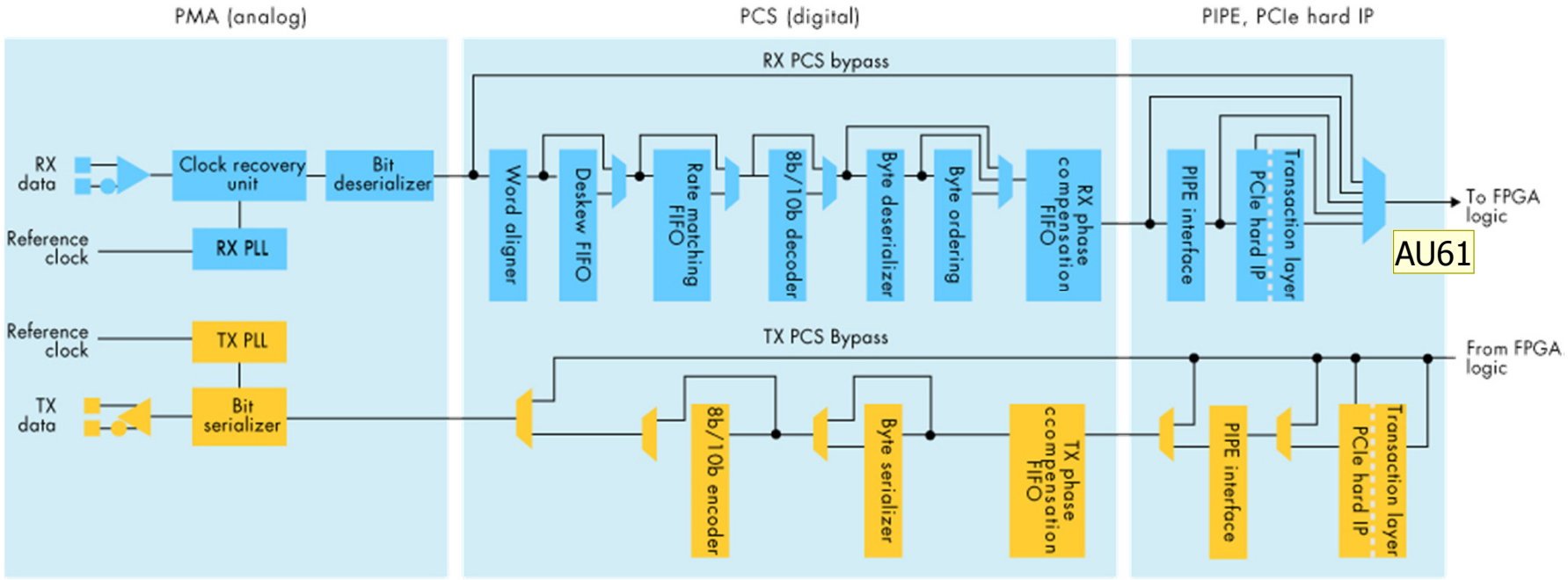
Power Reduction with DDR3 and Dynamic OCT

- **DDR3 consumes 30% lower power than DDR2**
  - DDR2 requires 1.8-V VCC rails
  - DDR3 requires 1.5-V VCC rails
- **Dynamic OCT reduces termination power by 1 W/72-bits**

Save 1.9W per 72-bit DIMM at 1067 Mbps

ALTERA®

Stratix IV GX Embedded Transceivers



- **Up to 48 transceivers**
  - 3G, 6G, and 8G channels
- **Comprehensive protocol support**

Data Rate	Transceiver Power
3.125 Gbps	100 mW
6.375 Gbps	135 mW
8.5 Gbps	165 mW

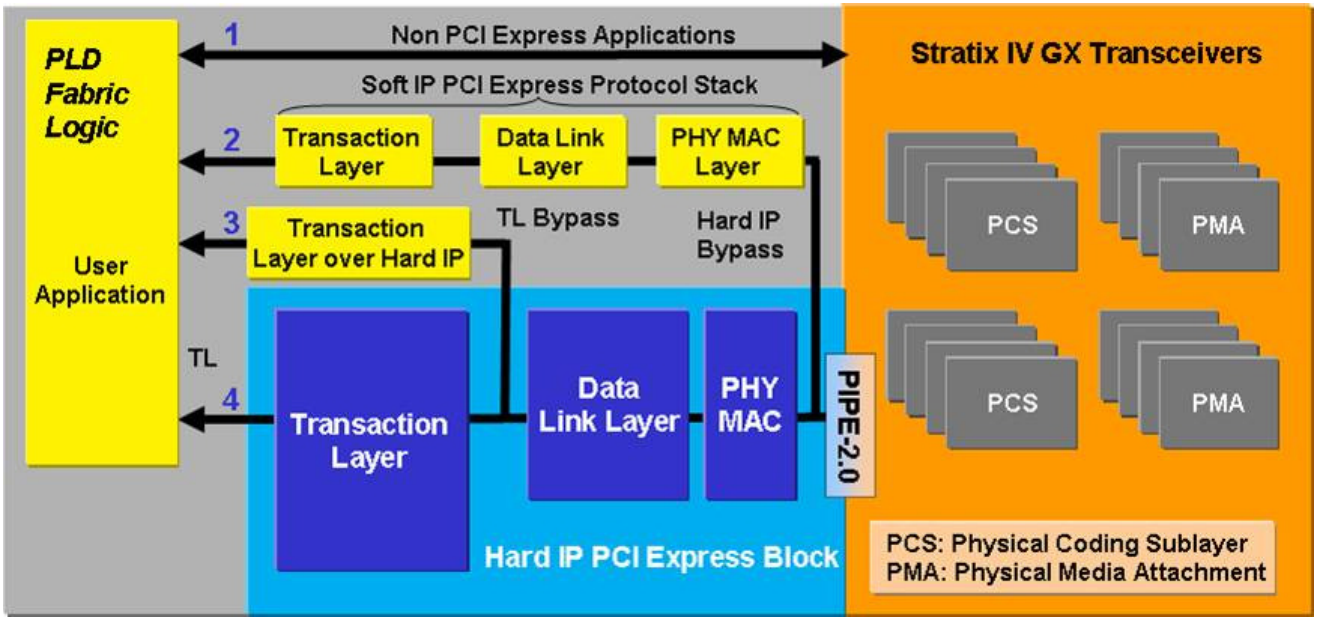
Highest system bandwidth and power efficiency

ALTERA®

Slide 17

AU61 In figure (which I can't change), please change the following:
Delete extra "c" in TX phase compensation... box.
Change 8b / 10b to 8B/10B
Altera User, 24/06/2008

Complete PCI Express Solution (Hard IP)



Legend

- Soft Logic
- PCI Express Hard IP
- PCS/PMA

- **Gen1 and Gen2 hard IP protocol stack (x2, x4, and x8)**
  - Guaranteed timing closure
  - Low latency
  - Minimizes power
  - Saves logic and memory
  - No IP fee

PCI Express Gen2			
Feature	**x8**	**x4**	**x2**
Bandwidth	**40 Gbps**	**20 Gbps**	**10 Gbps**
Dynamic Power	**600 mW**	**440 mW**	**350 mW**

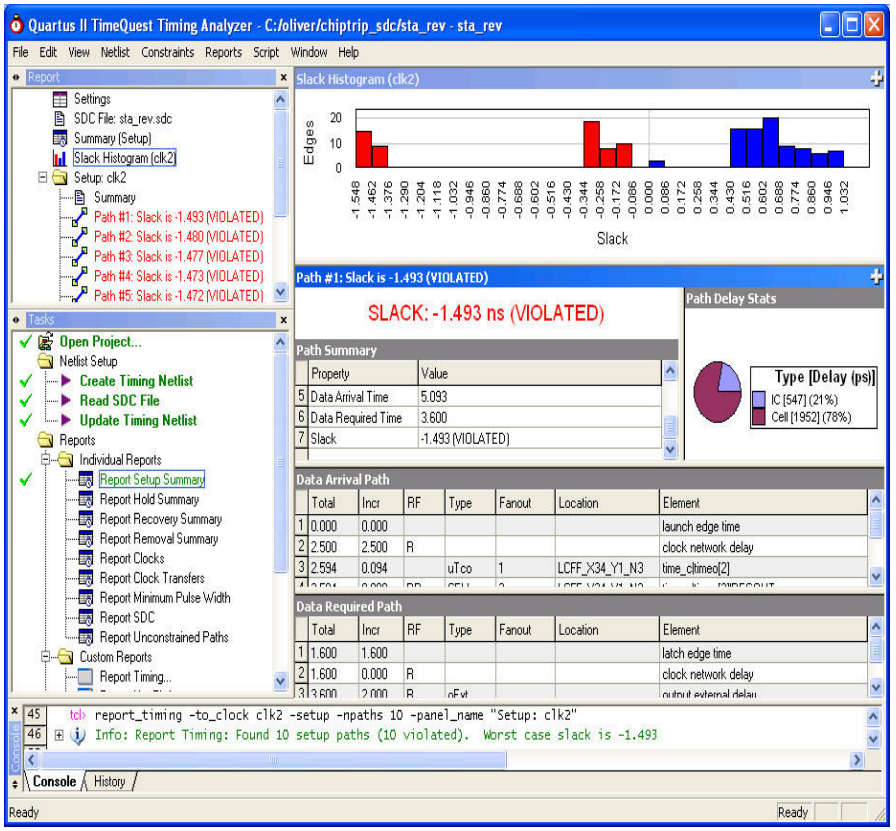
Integrated Gen1/Gen2 support

ALTERA®

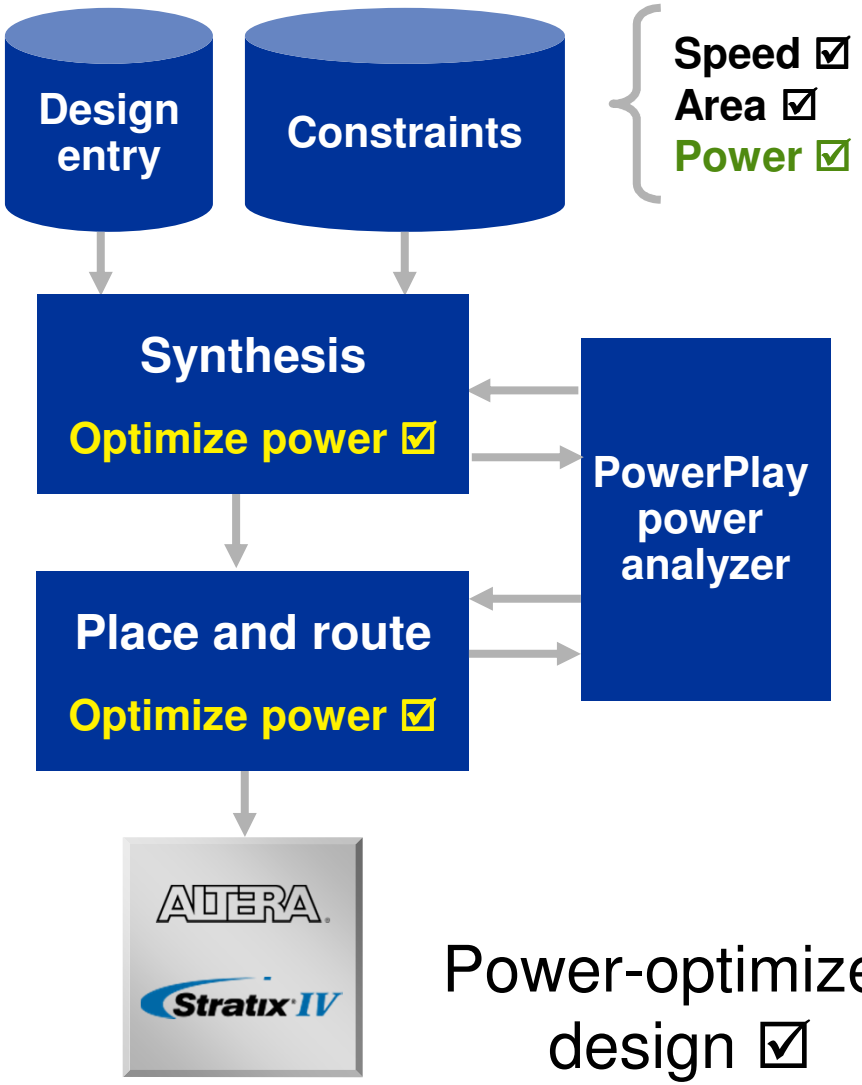
Quartus II Software CAD Takes Full Advantage Of Silicon

Timing Analysis and Closure

- **Easy to use**
  - Enter constraints via script or GUI
  - Extensive reports and visualization
- **Powerful timing constraints**
  - Uses SDC syntax
  - Complex clocking schemes
  - Source-synchronous design
- **Complete analysis**
  - Rise/fall delays
  - On-die variation (min/max)
  - Jitter models
  - Multiple corners (3 for Stratix IV FPGAs)
- **Accurate delays**
  - Full non-linear circuit simulator
  - Within 1% of SPICE, but 10,000 times faster
  - Complex end-of-life effects modeled
- **Full optimization**
  - Optimize all timing constraints
  - Across all process corners



Power: Analysis and Optimization



Power-optimized design ☑

Accurate power modeling

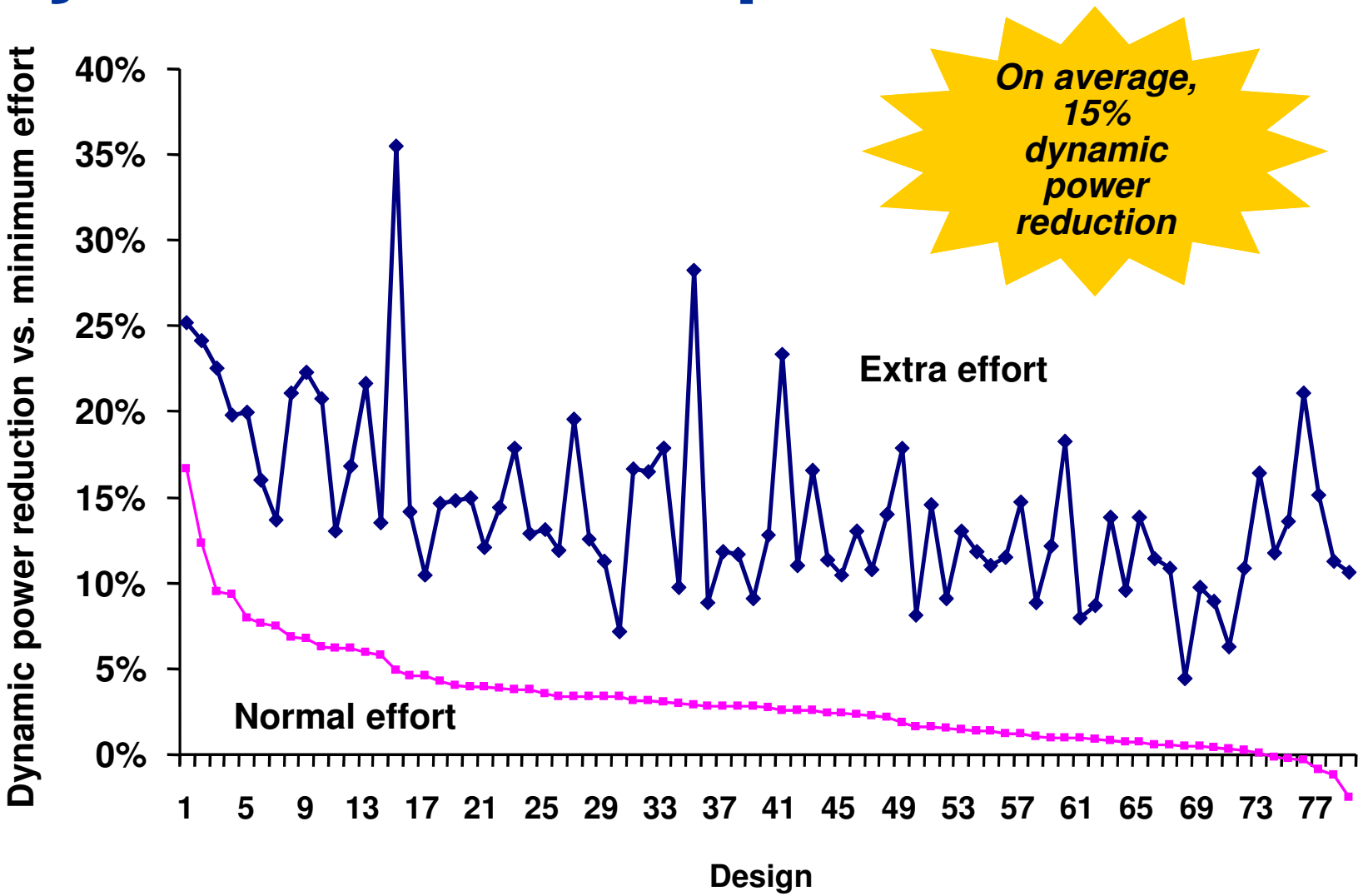
- Physics-based models
- Proven methodology and correlation

Accurate modeling enables good optimization

- Routing, logic, RAM, static

ALTERA®

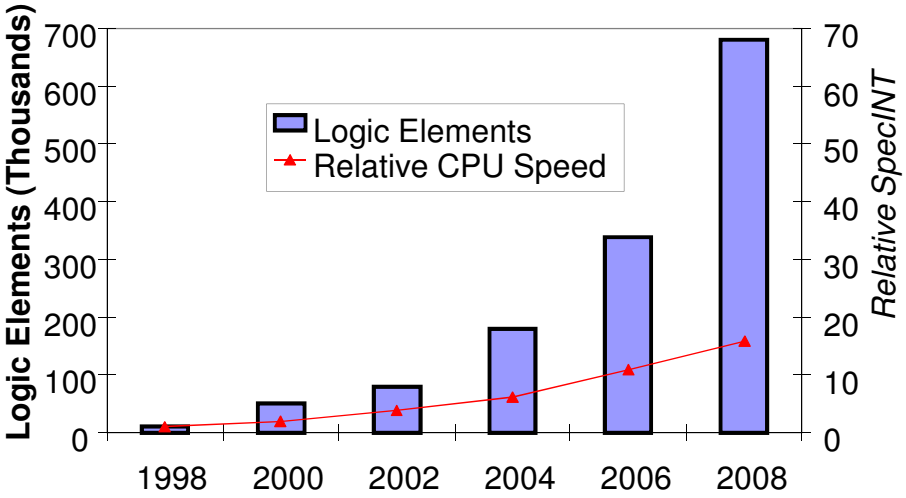
Dynamic Power Optimization



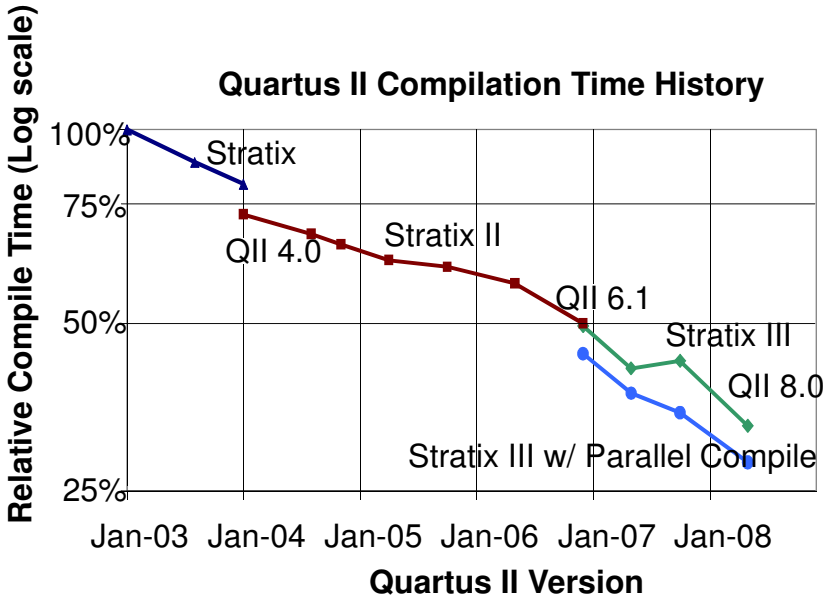
ALTERA®

Higher Productivity Through Lower Compile Times

- Problem:
  - FPGA capacity outpacing CPUs
  - 68x FPGA logic
  - 16x CPU speed
  - 4.3x gap



- Solution:
  - Faster algorithms
  - Parallel code
  - Incremental compile



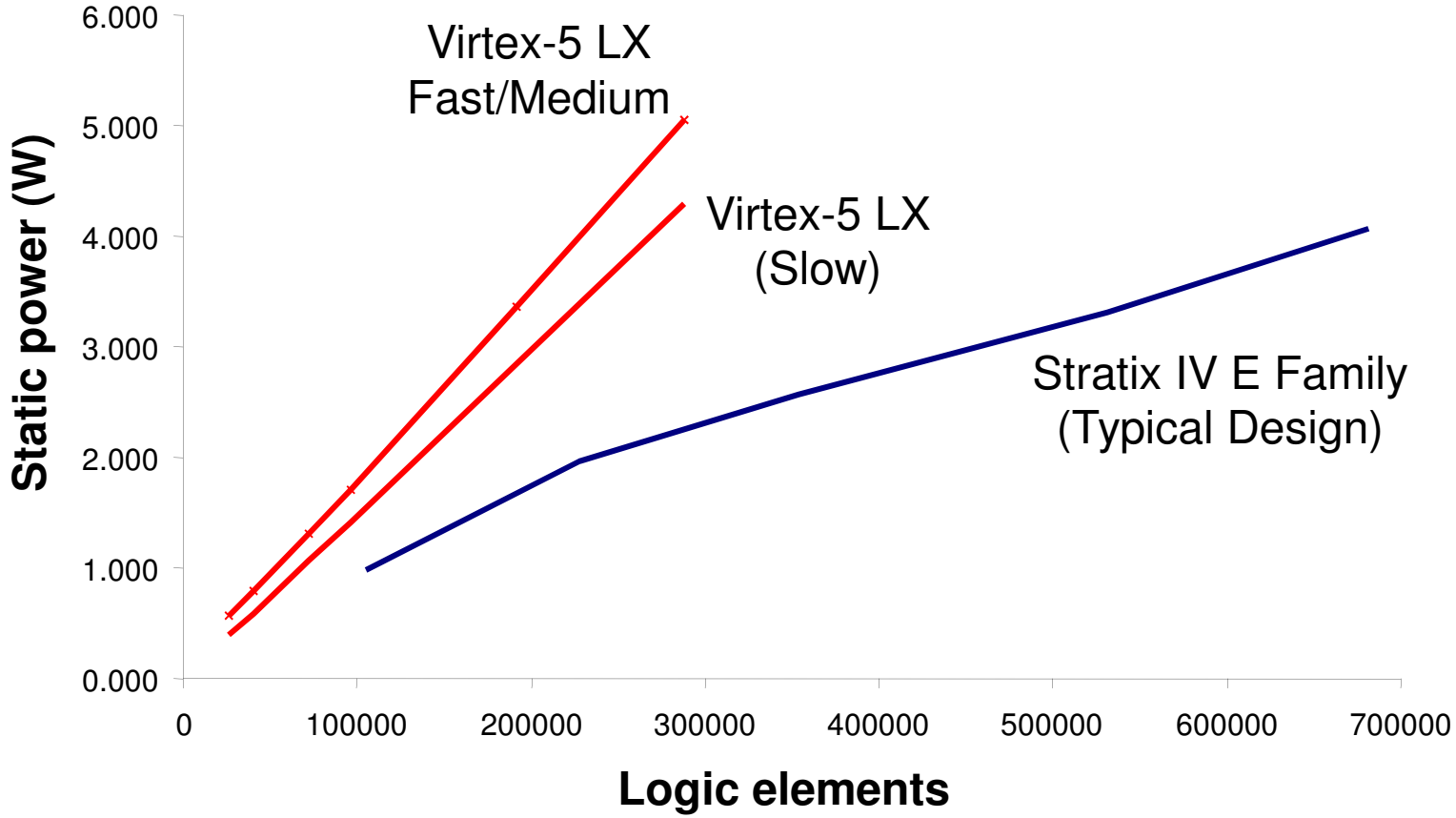
Competitive Comparison

Stratix IV FPGAs and
Virtex-5 FPGAs

Stratix IV FPGA Power Saving Techniques

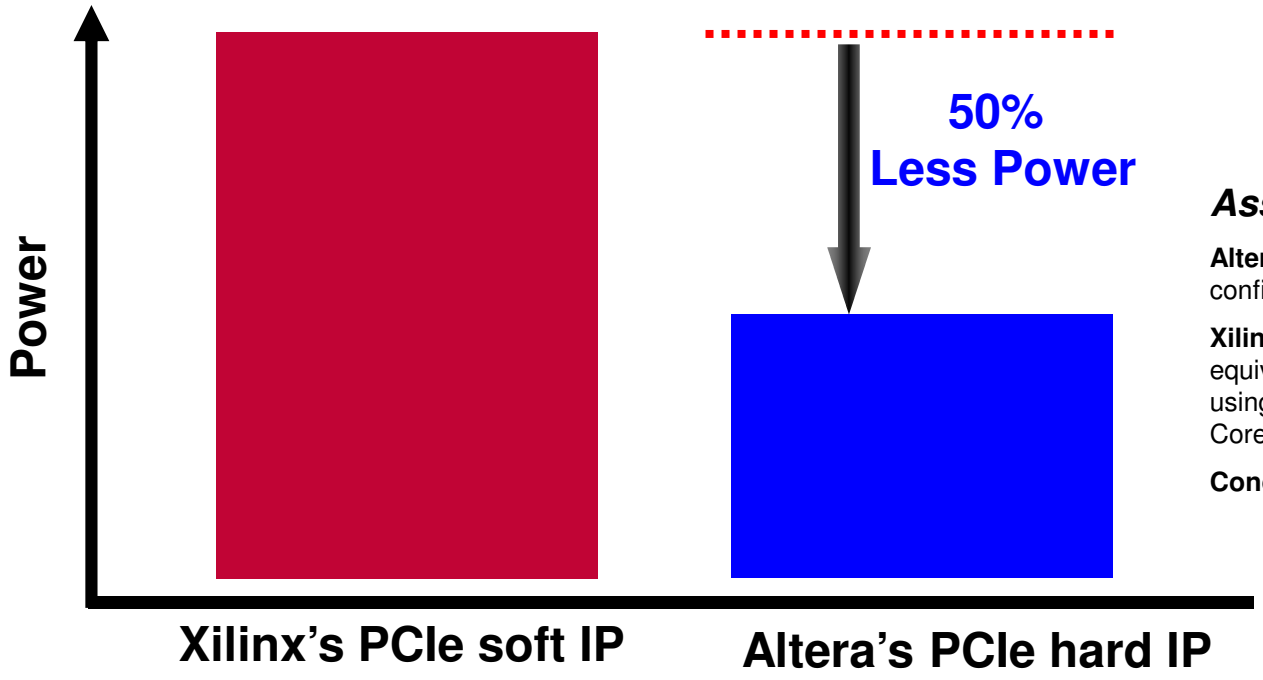
Power Minimizing Technique	Stratix IV FPGAs	Virtex-5 FPGAs
Silicon process optimizations	✓	✓
Programmable power technology	✓	✗
DDR3 with dynamic OCT	✓	✗
PCI Express Gen2 hard IP	✓	✗
Software static power optimization	✓	✗

Static Power Comparison



Stratix IV FPGAs double the density AND minimize static power

PCI Express Hard IP Minimizes Core Power



Assumptions:

Altera: Hard IP in Gen2 x4 configuration

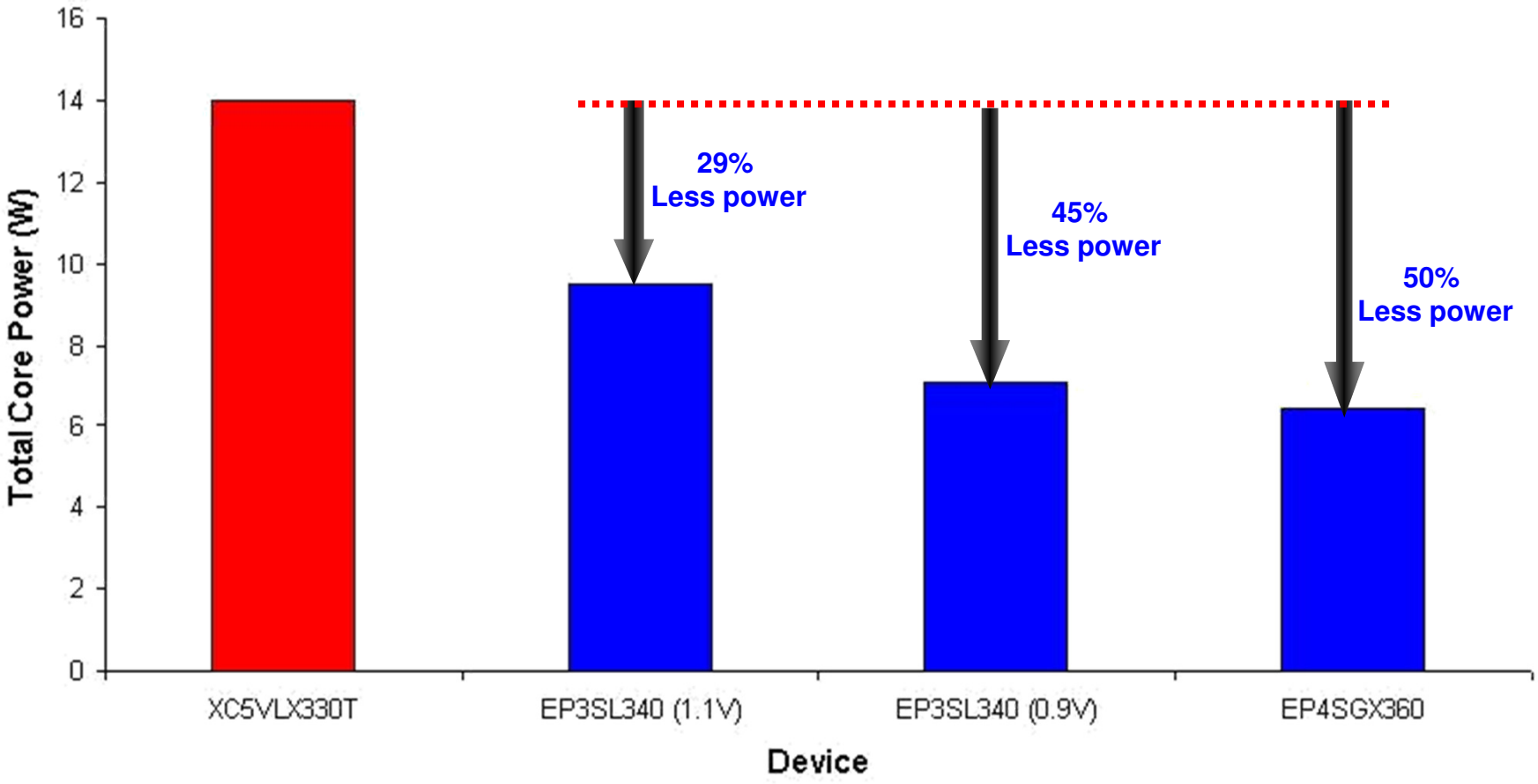
Xilinx: Soft IP with bandwidth equivalent to Gen2 x4 derived using resource count from Xilinx CoreGen and XPE v10.1

Conditions: Toggle Rate = 20%

FPGA industry's lowest power PCI Express solution

ALTERA®

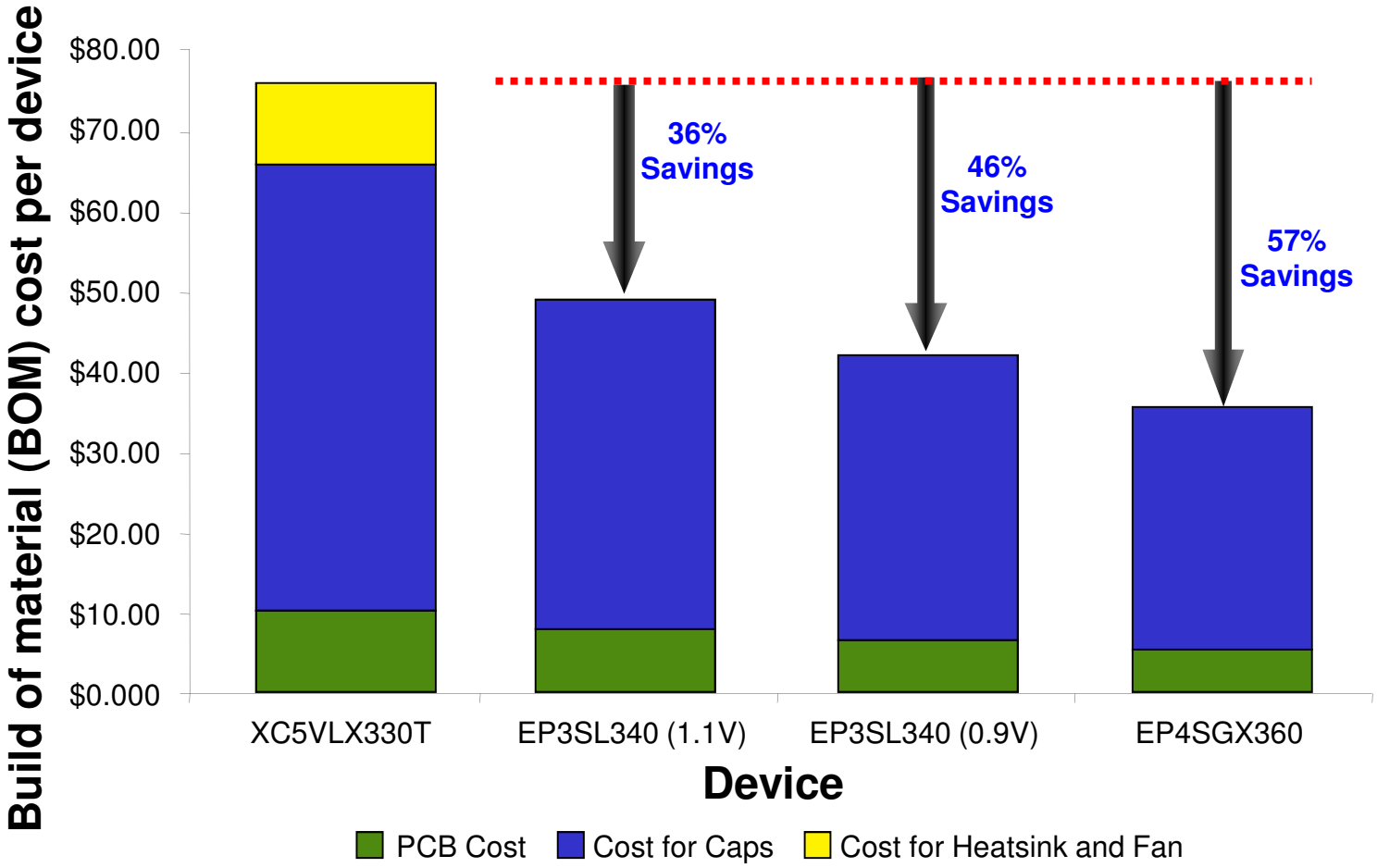
Save Multiple Watts/Device (300K LEs)



Reduce power consumption by 50%

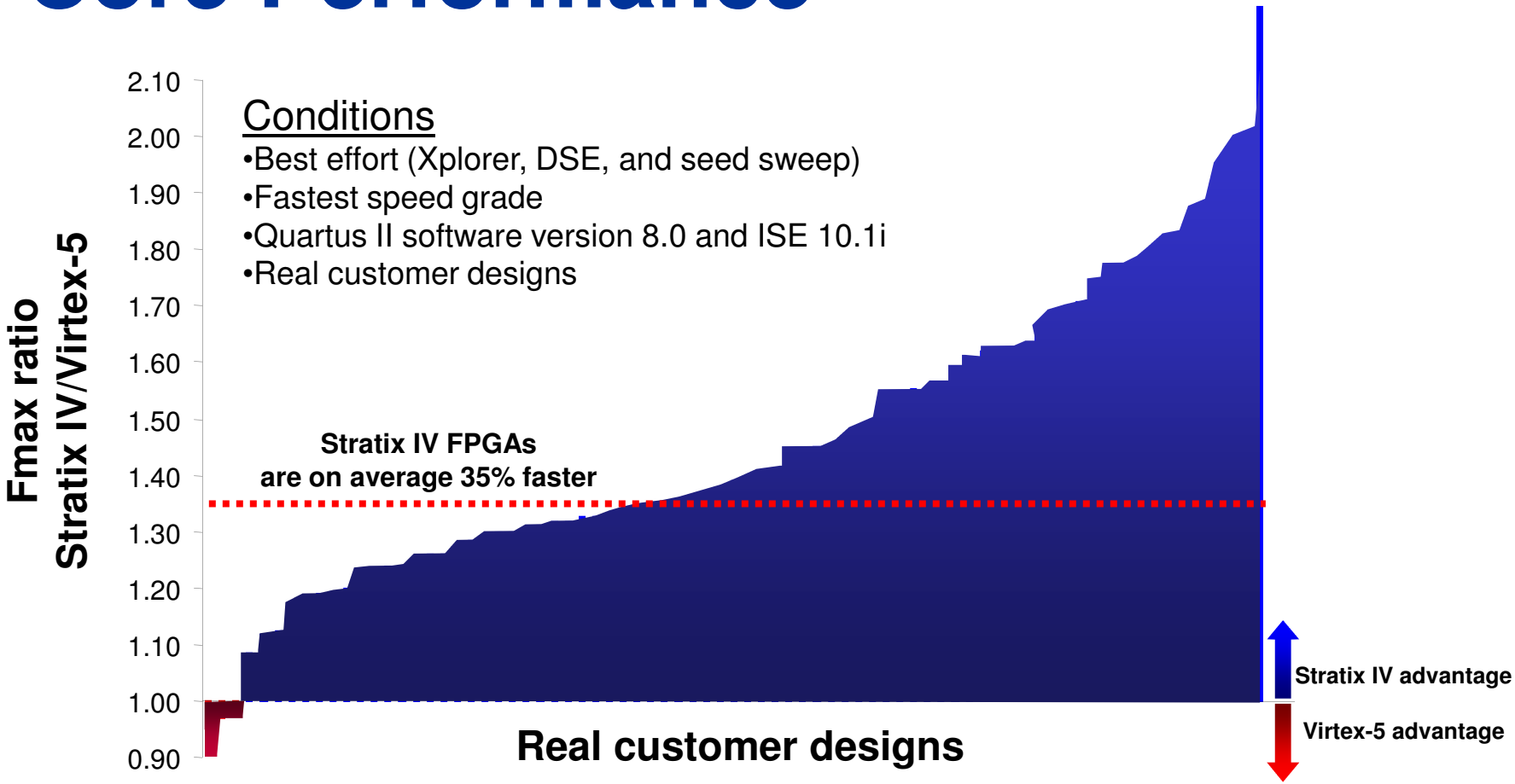
ALTERA®

Hidden Costs



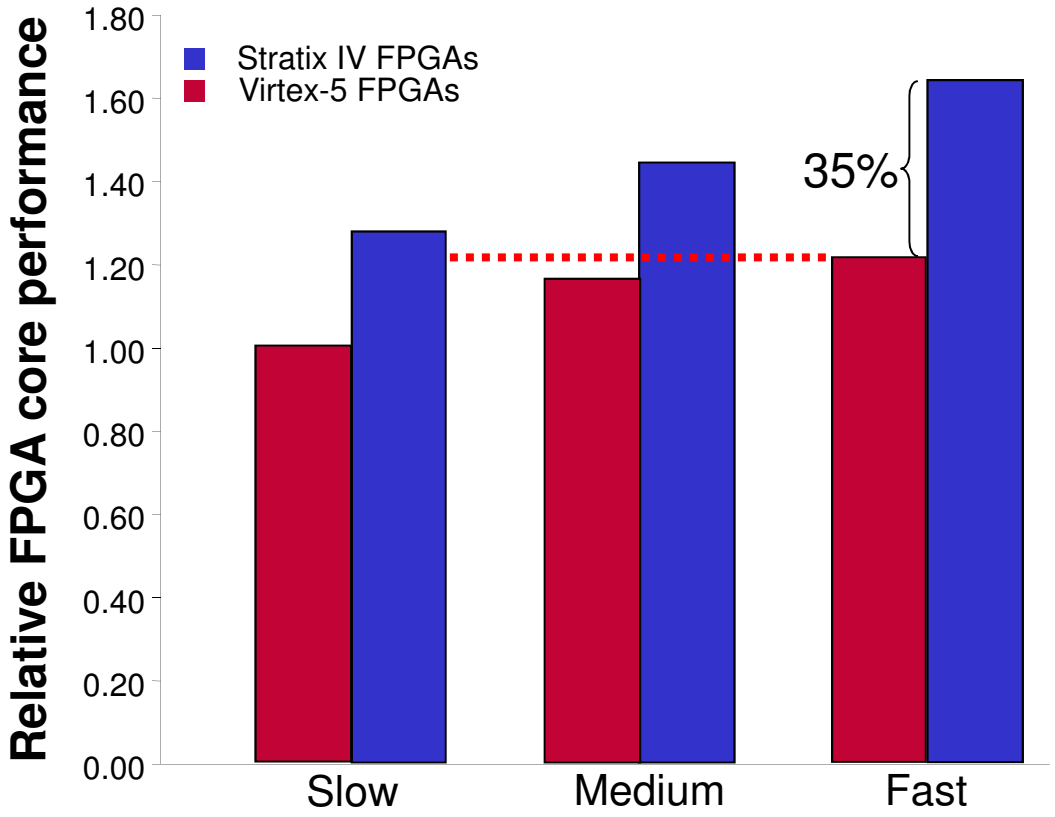
Reduce hidden costs with Stratix IV FPGAs by 57% per device!

Core Performance



On average, Stratix IV FPGAs are 35% faster than Virtex-5 FPGAs

Stratix IV FPGAs: Unprecedented Core Performance



Achieve higher performance and lower costs with Stratix IV FPGAs

ALTERA®

Stratix IV FPGAs: Unprecedented I/O Performance

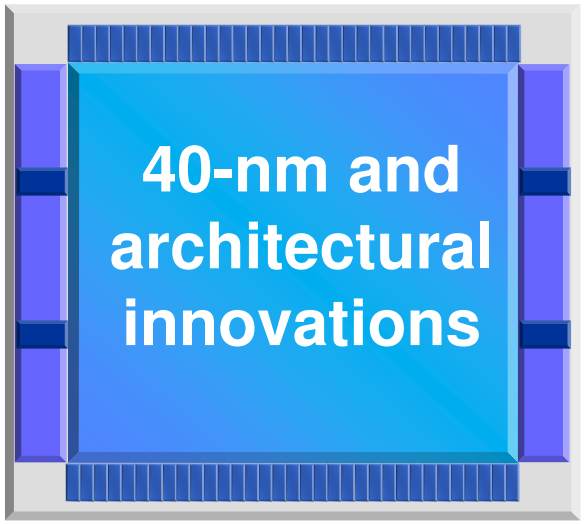
Interconnect	Virtex-5 FPGAs (65 nm)	Stratix IV FPGAs (40 nm)
DDR2	333 MHz	400+ MHz
DDR3	No DIMM support	533 MHz
QDR II	300 MHz	350 MHz
QDR II+	No DIMM support	400 MHz
RLDRAM II	300 MHz	400 MHz
LVDS	1.25 Gbps	1.6 Gbps
Transceivers	3G, 6G	3G, 6G, 8G
PCI-Express Hard IP x8	No solution	40G

Higher bandwidth with Stratix IV FPGAs

ALTERA®

Summary

Stratix IV FPGAs



- **Highest bandwidth and performance**
  - Core clock speeds of 600 MHz
  - Up to 48 transceiver blocks operating at up to 8.5 Gbps
  - DDR3 at 1067 Mbps
  - LVDS at 1.6 Gbps
  - Quartus II software performance optimization
- **Lowest power**
  - 0.9-V core voltage on an optimal 40-nm process
  - Programmable Power Technology
  - Lowest transceiver power
  - DDR3 with dynamic OCT
  - Integration of hard IP for PCI Express Gen1 and Gen2
  - Quartus II PowerPlay technology

Highest system bandwidth and power efficiency

ALTERA®

Resources

- Visit Stratix IV FPGA power web page
  - http://www.altera.com/products/devices/stratix-fpgas/stratix-iv/overview/power/stxiv-power.html
- Visit Stratix IV FPGA performance web page
  - http://www.altera.com/products/devices/stratix-fpgas/stratix-iv/overview/performance/stxiv-performance.html
- See Stratix IV FPGA transceiver (8G) and LVDS (1.5 Gbps) demos
  - http://www.altera.com/b/40-nm-stratix-iv-video.html
- Download Stratix IV FPGA power white paper
  - http://www.altera.com/literature/wp/wp-01059-stratix-iv-40nm-power-management.pdf
- Stratix IV EPE – power estimation spreadsheet
  - http://www.altera.com/support/devices/estimator/pow-powerplay.jsp
- See what Programmable Power Technology did for Stratix III FPGAs
  - http://www.altera.com/products/devices/stratix-fpgas/stratix-iii/overview/power/st3-power.html

ALTERA®

Additional Resources

- How Altera performs FPGA benchmarks
  - http://www.altera.com/literature/wp/wpfpgapbm.pdf
- Guidance on accurately benchmarking FPGAs white paper
  - http://www.altera.com/literature/wp/wp-01040.pdf
- Reproduce results through open cores
  - http://www.altera.com/products/devices/stratix-fpgas/stratix-iii/overview/architecture/performance/st3-opencores.html

ALTERA®

Thank You!

For more information visit:
www.altera.com