Manage Performance & Power Using 40-nm FPGAs

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Agenda

■ Design requirements
■ Stratix® IV FPGAs: Highest performance and lowest power
  – Processing techniques
  – Architectural innovations
  – Quartus® II software CAD system
■ High-end FPGA competitive comparison
## Design Requirements

<table>
<thead>
<tr>
<th>Designer Goals</th>
<th>What You Need From Your FPGA</th>
<th>What You Need From Your FPGA Software</th>
</tr>
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<tbody>
<tr>
<td>Functionality</td>
<td>High density</td>
<td>Ease of use</td>
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<tr>
<td></td>
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<td>Maximum utilization</td>
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<tr>
<td></td>
<td></td>
<td>Low compile times</td>
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<tr>
<td>Meet timing constraints</td>
<td>High performance</td>
<td>Detailed constraint entry</td>
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<tr>
<td></td>
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<td>Powerful timing analysis tool</td>
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<tr>
<td></td>
<td></td>
<td>Optimization of all timing requirements</td>
</tr>
<tr>
<td>Meet power budget</td>
<td>Low power</td>
<td>Automatic power optimization</td>
</tr>
<tr>
<td></td>
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<td>Accurate power analysis/reports</td>
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</tbody>
</table>

*Maximize performance and minimize power*
Stratix IV High-End FPGA Highlights
Stratix IV FPGAs

- Highest density
  - Up to 680K LEs
  - Up to 22.4-Mbits internal RAM
  - Up to 1,360 18x18 multipliers

- Highest bandwidth and performance
  - Up to 48 transceiver blocks operating at up to 8.5 Gbps
  - Maximum clock rates of 600 MHz

- Broad protocol support
  - Including hard IP for PCI Express Gen1 and Gen2

- Lowest power
  - 40-nm process benefits including 0.9-V core voltage
  - Programmable Power Technology (PPT)
  - Quartus II PowerPlay technology
Managing Performance and Power Through Process Technology
40-nm Process

- Aggressive gate length
  - Better density and higher speed than 45 nm

- Second-generation strained silicon
  - Increases electron mobility by up to 30%
  - Transistor level performance is up to 40% higher

- Strained silicon benefit can be converted to
  - Higher speed
  - Lower power (standby and dynamic)

In 40 nm, Altera converts benefits of strain to lower power
Leading Edge Process Technology at 40 nm

- **Advanced 40-nm process at 0.9 V**
  - Lower voltage → reduces dynamic power by 33%
  - 30% capacitance reduction → reduces dynamic power
  - 39% shorter channel length compared to 65 nm → increases performance

- **Multiple-gate oxide thicknesses (triple oxide)**
  - Trade-off static power vs. speed per transistor

- **Multiple-threshold voltages**
  - Trade-off static power vs. speed per transistor

- **Low-k inter-metal dielectric**
  - Reduces dynamic power, increases performance

- **Super strained silicon**
  - Increases electron and hole mobility by 30%
  - Balance between power and performance

- **Copper interconnect**
  - Increased performance, reduced IR drop

Best-in-class process for power and performance
Architecture Innovation:
Better Performance, Reduced Power
Design-Specific Power Optimization

- Only a small fraction of logic is performance critical

Slack Histogram

- **Not performance critical**
  - 90-100%: 8,000
  - 80-90%: 7,000
  - 70-80%: 6,000
  - 60-70%: 5,000
  - 50-60%: 4,000
  - 40-50%: 3,000
  - 30-40%: 2,000
  - 20-30%: 1,000
  - 10-20%: 0
  - 0-10%: 0

- **Performance critical**

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Programmable Speed vs. Leakage

Note: A simple “model” showing Programmable Power Technology. Actual implementation varies and is patented.
Programmable Power Technology

Logic array

Timing critical path

High-speed logic
Low-power logic
Unused low-power logic

Performance where you need it, lowest power everywhere else
Quartus II Software Automatically Uses PPT

Synthesis

Placement and routing

Unused tiles → low power

Timing analysis

Tiles with timing slack → low power

Done? No Yes

All high-speed tiles

Mostly low-power tiles

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Stratix IV FPGA DDR3 Support

**Interconnect** | **Performance**
--- | ---
DDR3 | >533 MHz/1067 Mbps
DDR2 | 400 MHz/800 Mbps
QDR II | 350 MHz
QDR II+ | 400 MHz
RLDRAM II | 400 MHz
LVDS | 1.60 Gbps

**I/O Feature** | **Stratix IV FPGAs** | **Benefit**
--- | --- | ---
Dynamic On-Chip Termination (OCT) | ✓ | Saves power
DDR3 Read/Write Leveling | ✓ | Required for DIMM support
Variable I/O Delay | ✓ | Allows signal de-skew

** DDR3 DIMM support at 533 MHz through read/write leveling **

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Dynamic OCT

- Write: Rs on, Rt off → Matching line impedance
- Read: Rs off, Rt on → Terminating far end
Power Reduction with DDR3 and Dynamic OCT

- DDR3 consumes 30% lower power than DDR2
  - DDR2 requires 1.8-V VCC rails
  - DDR3 requires 1.5-V VCC rails
- Dynamic OCT reduces termination power by 1 W/72-bits

*Save 1.9W per 72-bit DIMM at 1067 Mbps*
Stratix IV GX Embedded Transceivers

- Up to 48 transceivers
  - 3G, 6G, and 8G channels
- Comprehensive protocol support

### Data Rate Transceiver Power

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>Transceiver Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.125 Gbps</td>
<td>100 mW</td>
</tr>
<tr>
<td>6.375 Gbps</td>
<td>135 mW</td>
</tr>
<tr>
<td>8.5 Gbps</td>
<td>165 mW</td>
</tr>
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</table>

**Highest system bandwidth and power efficiency**

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In figure (which I can't change), please change the following:
Delete extra "c" in TX phase compensation... box.
Change 8b / 10b to 8B/10B

Alter User, 24/06/2008
Complete PCI Express Solution (Hard IP)

Legend

Soft Logic

PCI Express Hard IP
PCS/PMA

Gen1 and Gen2 hard IP protocol stack (x2, x4, and x8)
- Guaranteed timing closure
- Low latency
- Minimizes power
- Saves logic and memory
- No IP fee

Integrated Gen1/Gen2 support

<table>
<thead>
<tr>
<th>Feature</th>
<th>x8</th>
<th>x4</th>
<th>x2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>40 Gbps</td>
<td>20 Gbps</td>
<td>10 Gbps</td>
</tr>
<tr>
<td>Dynamic Power</td>
<td>600 mW</td>
<td>440 mW</td>
<td>350 mW</td>
</tr>
</tbody>
</table>

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Quartus II Software CAD Takes Full Advantage Of Silicon
Timing Analysis and Closure

- **Easy to use**
  - Enter constraints via script or GUI
  - Extensive reports and visualization

- **Powerful timing constraints**
  - Uses SDC syntax
  - Complex clocking schemes
  - Source-synchronous design

- **Complete analysis**
  - Rise/fall delays
  - On-die variation (min/max)
  - Jitter models
  - Multiple corners (3 for Stratix IV FPGAs)

- **Accurate delays**
  - Full non-linear circuit simulator
  - Within 1% of SPICE, but 10,000 times faster
  - Complex end-of-life effects modeled

- **Full optimization**
  - Optimize all timing constraints
  - Across all process corners
Power: Analysis and Optimization

- Design entry
- Constraints
  - Speed ✓
  - Area ✓
  - Power ✓

1. Synthesis
   - Optimize power ✓

2. Place and route
   - Optimize power ✓

3. PowerPlay power analyzer

Power-optimized design ✓

Accurate power modeling
- Physics-based models
- Proven methodology and correlation

Accurate modeling enables good optimization
- Routing, logic, RAM, static

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Dynamic Power Optimization

On average, 15% dynamic power reduction

Design

Dynamic power reduction vs. minimum effort

Extra effort

Normal effort

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Higher Productivity Through Lower Compile Times

Problem:
- FPGA capacity outpacing CPUs
- 68x FPGA logic
- 16x CPU speed
- 4.3x gap

Solution:
- Faster algorithms
- Parallel code
- Incremental compile

Quartus II Compilation Time History

Logic Elements (Thousands) vs. Relative SpecINT

Quartus II Version
- Stratix
- QII 4.0
- Stratix II
- QII 6.1
- Stratix III
- QII 8.0
- Stratix III w/ Parallel Compile

Relative Compile Time (Log scale)

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Competitive Comparison

Stratix IV FPGAs and
Virtex-5 FPGAs
## Stratix IV FPGA Power Saving Techniques

<table>
<thead>
<tr>
<th>Power Minimizing Technique</th>
<th>Stratix IV FPGAs</th>
<th>Virtex-5 FPGAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon process optimizations</td>
<td>✅</td>
<td>✅</td>
</tr>
<tr>
<td>Programmable power technology</td>
<td>✅</td>
<td>✗</td>
</tr>
<tr>
<td>DDR3 with dynamic OCT</td>
<td>✅</td>
<td>✗</td>
</tr>
<tr>
<td>PCI Express Gen2 hard IP</td>
<td>✅</td>
<td>✗</td>
</tr>
<tr>
<td>Software static power optimization</td>
<td>✅</td>
<td>✗</td>
</tr>
</tbody>
</table>
Static Power Comparison

Stratix IV FPGAs double the density AND minimize static power
PCI Express Hard IP Minimizes Core Power

Assumptions:
Altera: Hard IP in Gen2 x4 configuration
Xilinx: Soft IP with bandwidth equivalent to Gen2 x4 derived using resource count from Xilinx CoreGen and XPE v10.1

Conditions: Toggle Rate = 20%

FPGA industry’s lowest power
PCI Express solution
Save Multiple Watts/Device (300K LEs)

Reduce power consumption by 50%
Hidden Costs

Reduce hidden costs with Stratix IV FPGAs by 57% per device!
Core Performance

On average, Stratix IV FPGAs are 35% faster than Virtex-5 FPGAs.

Conditions
• Best effort (Xplorer, DSE, and seed sweep)
• Fastest speed grade
• Quartus II software version 8.0 and ISE 10.1i
• Real customer designs
Stratix IV FPGAs: Unprecedented Core Performance

Achieve higher performance and lower costs with Stratix IV FPGAs

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## Stratix IV FPGAs: Unprecedented I/O Performance

<table>
<thead>
<tr>
<th>Interconnect</th>
<th>Virtex-5 FPGAs (65 nm)</th>
<th>Stratix IV FPGAs (40 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR2</td>
<td>333 MHz</td>
<td>400+ MHz</td>
</tr>
<tr>
<td>DDR3</td>
<td>No DIMM support</td>
<td>533 MHz</td>
</tr>
<tr>
<td>QDR II</td>
<td>300 MHz</td>
<td>350 MHz</td>
</tr>
<tr>
<td>QDR II+</td>
<td>No DIMM support</td>
<td>400 MHz</td>
</tr>
<tr>
<td>RLDGRAM II</td>
<td>300 MHz</td>
<td>400 MHz</td>
</tr>
<tr>
<td>LVDS</td>
<td>1.25 Gbps</td>
<td>1.6 Gbps</td>
</tr>
<tr>
<td>Transceivers</td>
<td>3G, 6G</td>
<td>3G, 6G, 8G</td>
</tr>
<tr>
<td>PCI-Express Hard IP x8</td>
<td>No solution</td>
<td>40G</td>
</tr>
</tbody>
</table>

*Higher bandwidth with Stratix IV FPGAs*
Summary

Stratix IV FPGAs

40-nm and architectural innovations

- **Highest bandwidth and performance**
  - Core clock speeds of 600 MHz
  - Up to 48 transceiver blocks operating at up to 8.5 Gbps
  - DDR3 at 1067 Mbps
  - LVDS at 1.6 Gbps
  - Quartus II software performance optimization

- **Lowest power**
  - 0.9-V core voltage on an optimal 40-nm process
  - Programmable Power Technology
  - Lowest transceiver power
  - DDR3 with dynamic OCT
  - Integration of hard IP for PCI Express Gen1 and Gen2
  - Quartus II PowerPlay technology

*Highest system bandwidth and power efficiency*

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Resources

- Visit Stratix IV FPGA power web page

- Visit Stratix IV FPGA performance web page

- See Stratix IV FPGA transceiver (8G) and LVDS (1.5 Gbps) demos

- Download Stratix IV FPGA power white paper

- Stratix IV EPE – power estimation spreadsheet

- See what Programmable Power Technology did for Stratix III FPGAs
Additional Resources

- How Altera performs FPGA benchmarks

- Guidance on accurately benchmarking FPGAs white paper

- Reproduce results through open cores
Thank You!

For more information visit:
www.altera.com