Power Solutions for Leading-Edge FPGAs

Vaughn Betz & Paul Ekas
Agenda

- 90 nm Power Overview
- Stratix II®: Power Optimization Without Sacrificing Performance
  - Technical Features & Competitive Results
    - Dynamic Power
    - Static Power
    - I/O Power
- HardCopy® II Structured ASICs: The Path to Lowest Power
- Summary & Wrap Up
90 nm Power Overview
90 nm: Operating Power Reduced

Relative Power vs. Frequency (MHz)

- Green line: 130 nm
- Blue line: 90 nm

Lower Operating Power
Power Breakdown: 90 nm vs. 130nm

- 130 nm (Stratix)
- 90 nm (Stratix II)

- I/O
- Static Core
- Dynamic Core
Power: 90 nm vs. 130 nm

- Large Dynamic Power Reduction
  - Dominant Power, so Most Important

- Static Power Increases
  - Need to Architect FPGA to Minimize Increase
  - Without Sacrificing 90 nm Performance

- I/O Power Does Not Scale with Process
  - Need to Improve Circuit Design to Get Gains
Stratix II FPGAs

Power Optimization Without Sacrificing Performance
Power Versus Performance
The Major Challenge for 90-nm High-Performance FPGAs

- Stratix II: Most Performance Within Power Budget
  - Minimize Power for Non-Performance Critical Circuitry
    - “Black Diamond” Low-K Dielectric
    - Increased $V_T$
    - Increased Gate Length
  - Maximize Performance Where Needed
    - Adaptive Logic Module (ALM) Architecture
    - “Black Diamond” Low-K Dielectric
    - Lower $V_T$ Only Where Needed
    - Shorter Gate Length Only for Most Performance Critical
  - Redesign I/Os for Minimum Power
1. Dynamic Power
Core Dynamic Power

- Usually Most Important Power Component
- Power Proportional to Clock Frequency

\[ P_{\text{dynamic}} = \left[ \frac{1}{2} CV^2 + Q_{\text{ShortCircuit}} V \right] f \cdot \text{activity} \]

- 1\textsuperscript{st} Term: Capacitance Charging
  - Dominant Dynamic Power Component

- 2\textsuperscript{nd} Term: Short Circuit Charge During Switching
  - Smaller Component

- Activity: % of Circuit That Switches Each Cycle
  - Highly Design Dependent

- Little Dependence on Temperature or Process Variation
Core Dynamic Power

- Typical Breakdown (112 Customer Design Average)

- Routing 40%
- ALM Combinational 23%
- ALM Registers 16%
- RAM Blocks 14%
- Clock Networks 7%
- DSP Blocks 1%*

*DSP Block Power: 5% of Dynamic Power for Designs that Use DSP Blocks

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Minimizing Dynamic Power: Low-k

- Stratix II: Black Diamond Low-k Dielectric
  - Metal Capacitance $\propto k$ (Dielectric Constant)
  - Dynamic Power $\propto$ Capacitance Charged
    - Metal Capacitance is Dominant
  - Black Diamond: $k = 2.9$
  - FSG (“Reduced-k”): $k = 3.6$
  - Black Diamond Reduces Metal Capacitance by \textbf{20\%} vs. FSG Used by Competing FPGAs!

- Result: 14\% Dynamic Power Reduction \textit{and} 12\% Speed Improvement

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Minimizing Dynamic Power: Clocking

- Stratix II FPGA Shuts Down Unused Parts of Clock Networks
  - With Fine Control Granularity (Nearly 800 Regions!)
  - Automatically Implemented for Each Design by Quartus® II Software
Minimizing Dynamic Power: RAM

- Tri-Matrix Memory
  - Power Inefficient to Use a Large Physical RAM for a Small Memory or Vice Versa
  - Stratix II FPGA: 3 RAM Sizes
  - Quartus II Software Automatically Picks Good Physical RAM

- Shut Down RAM Core When Clk Enable Low
  - Near 0 Dynamic Power on Cycles Where RAM Not Accessed
  - Quartus II Release 5.0 Automates When Possible
Basic Blocks: Power Estimators

- Compare Component Power for Stratix II & Virtex-4 FPGAs
- Using Latest Power Estimators
  - Altera Early Power Estimator Version 2.1
  - Xilinx Power WebTool Version 4.1
- Measure All Power Sources
  - Stratix II FPGA
    - $V_{CCINT}$: Internal Core Power
    - $V_{CCIO}$: I/O Power
    - $V_{CCPD}$: Pre-Drive Power for I/O
  - Virtex-4 FPGA
    - $V_{CCINT}$: Internal Core Power (Most Internal Circuitry)
    - $V_{CCO}$: I/O Power
    - $V_{CCAUX}$: Powers Some Internal Circuitry
Dynamic Power: Logic & Routing

- Power = # LUTs x Power per (LUT + Routing)

<table>
<thead>
<tr>
<th>200 MHz, 30% Toggle</th>
<th>Stratix II (mW)</th>
<th>Virtex-4 (mW)</th>
<th>% Diff</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 LUT/ALUT + FF + Typical Routing</td>
<td>0.147</td>
<td>0.157</td>
<td>-6%</td>
</tr>
<tr>
<td>Stratix II: 18% Fewer ALUTs per Circuit</td>
<td>0.121 (eq. logic)</td>
<td>0.157</td>
<td>-23%</td>
</tr>
</tbody>
</table>

Stratix II Family Has Lower Power in Logic & Routing
## Dynamic Power: Memory

- 200 MHz Dual-Port (1 Read, 1 Write) Synchronous RAM

<table>
<thead>
<tr>
<th>Size (bits)</th>
<th>Width x Depth</th>
<th>Stratix II (mW)</th>
<th>Virtex-4 (mW)</th>
<th>% Diff</th>
</tr>
</thead>
<tbody>
<tr>
<td>512</td>
<td>16 x 32</td>
<td>4.1</td>
<td>9.9</td>
<td>-58%</td>
</tr>
<tr>
<td>4K</td>
<td>8 x 512</td>
<td>6.9</td>
<td>11.3</td>
<td>-39%</td>
</tr>
<tr>
<td>16K</td>
<td>16 x 1024</td>
<td>15.6</td>
<td>12.3</td>
<td>+27%</td>
</tr>
<tr>
<td>16K</td>
<td>128 x 128</td>
<td>33.8</td>
<td>62.4</td>
<td>-46%</td>
</tr>
<tr>
<td>512K</td>
<td>64 x 8192</td>
<td>218</td>
<td>339</td>
<td>-36%</td>
</tr>
</tbody>
</table>
## Dynamic Power: DSP & PLL

<table>
<thead>
<tr>
<th>Block @ 200 Mhz</th>
<th>Stratix II (mW)</th>
<th>Virtex-4 (mW)</th>
<th>% Diff</th>
</tr>
</thead>
<tbody>
<tr>
<td>18x18 Multiplier</td>
<td>8.0</td>
<td>10.0</td>
<td>-20%</td>
</tr>
<tr>
<td>9x9 Multiplier</td>
<td>3.5</td>
<td>&lt;10.0</td>
<td>-65%</td>
</tr>
<tr>
<td>36x36 Multiplier</td>
<td>20.5</td>
<td>45.6</td>
<td>-55%</td>
</tr>
<tr>
<td>400 MHz PLL/DCM</td>
<td>23</td>
<td>119</td>
<td>-81%</td>
</tr>
<tr>
<td>100 MHz PLL/DCM</td>
<td>17</td>
<td>38</td>
<td>-55%</td>
</tr>
</tbody>
</table>
Basic Blocks: Measured Power

- Lab Measurements of Power Consumed per Basic Block
  1. Measure Power With Only Test Circuitry
  2. Measure Power With Test Circuitry & Basic Block of Interest
  3. Subtract to Obtain Power for Basic Block

- Nominal Voltage

- Ambient Temperature = 25°C
  - Recall: Very Little Impact on Dynamic Power
# Devices & Boards Used

<table>
<thead>
<tr>
<th>Family</th>
<th>Device</th>
<th>Equiv. LEs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stratix II</td>
<td>EP2S15</td>
<td>15,600</td>
</tr>
<tr>
<td>Virtex-4</td>
<td>4VLX25</td>
<td>21,504</td>
</tr>
<tr>
<td>Stratix II</td>
<td>EP2S30</td>
<td>33,880</td>
</tr>
<tr>
<td>Stratix</td>
<td>EP1S25</td>
<td>25,660</td>
</tr>
</tbody>
</table>
Dynamic Power: Logic

931 Six-Bit Gray Code Counters

- Stratix II
- Virtex-4

Power (mW) vs. Frequency (MHz)

1.25X Power
Dynamic Power: RAM

18-Bit Wide x 32 Deep Dual-Port RAM

- **Stratix II**
- **Virtex-4**

Power (mW) vs. Frequency (MHz)

2.6X Power
Dynamic Power: DSP

32 16x16 Multipliers

Power (mW)

Frequency (MHz)

1.25X Power

Stratix II
Virtex-4

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DCM/PLL Power

- Stratix II FPLL
- Stratix II EPLL
- Virtex-4 High F DCM
- Virtex-4 Low F DCM

3.3X – 5X Power

Power (mW)

Frequency (MHz)
2. Static Power
Static Power

1. Subthreshold Leakage from Source to Drain of Off Transistors
   - Main Leakage Component at 90 nm
   - Increases Rapidly with Temperature
   - Highly Dependent on Process Variation

2. Gate Leakage (Smaller)

3. Reverse-Biased Junction Leakage (Very Small)
Leakage Power: Temperature Effect

![Graph showing the relationship between Relative Leakage and Temperature (°C)]
Stratix II Leakage Power Reduction

- High-Vt Transistors Where Not Speed-Critical
  - Especially Configuration SRAM
  - 10X Leakage Reduction

- Longer Channels for Most Transistors
  - Significant Leakage Reduction
  - Reduces Leakage Variability Across Process
    - Helps Worst-Case Leakage Most!
Channel Length Variation Due To Manufacturing

Short Gate

Large % Variation of Channel Length

Max
Min

Long Gate

Small % Variation of Channel Length

Max
Min

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Process Variation Impact On Leakage

- High Vt: Increased L
- “Typical” Vt & L
- Low Vt: Reduced L

Over 40% Worst-Case Leakage Reduction

- Short L
- Long L

Relative Leakage

Process Variation

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Static Power Comparison

- Using Latest Altera & Xilinx Power Estimators
  - Sum Static Power From All Relevant Supplies
    • Vccint & Vccpd for Stratix II FPGA
    • Vccint & Vccaux for Virtex-4 FPGA

- Most Important Comparison: Worst-Case Device Leakage Values
  - Using Typical Values Means 50% of Devices You Receive Will Have Power Greater Than You Model!
  - Stratix II Early Power Estimator Includes Worst-Case Models
  - Virtex-4 Power Tool: Multiply Typical Static Power by 2.5X (Xilinx Guidance to Customers)
## Static Power Comparison

<table>
<thead>
<tr>
<th>Part</th>
<th>Power $V_{CCINT}$</th>
<th>Power $V_{CCPD}$</th>
<th>Total Static Power</th>
<th>Part</th>
<th>Power $V_{CCINT}$</th>
<th>Power $V_{CCaux}$</th>
<th>Total Static Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>EP2S15</td>
<td>792mW</td>
<td>33mW</td>
<td><strong>825mW</strong></td>
<td>LX15</td>
<td>345mW</td>
<td>230mW</td>
<td><strong>575mW</strong></td>
</tr>
<tr>
<td>EP2S30</td>
<td>1.13W</td>
<td>66mW</td>
<td><strong>1.19W</strong></td>
<td>LX25</td>
<td>568mW</td>
<td>262mW</td>
<td><strong>830mW</strong></td>
</tr>
<tr>
<td>EP2S60</td>
<td>2.16W</td>
<td>76mW</td>
<td><strong>2.24W</strong></td>
<td>LX40</td>
<td>892mW</td>
<td>305mW</td>
<td><strong>1.20W</strong></td>
</tr>
<tr>
<td>EP2S90</td>
<td>3.16W</td>
<td>82mW</td>
<td><strong>3.24W</strong></td>
<td>LX60</td>
<td>1.22W</td>
<td>530mW</td>
<td><strong>1.74W</strong></td>
</tr>
<tr>
<td>EP2S130</td>
<td>4.32W</td>
<td>99mW</td>
<td><strong>4.42W</strong></td>
<td>LX80</td>
<td>1.60W</td>
<td>585mW</td>
<td><strong>2.18W</strong></td>
</tr>
<tr>
<td>EP2S180</td>
<td>5.34W</td>
<td>116mW</td>
<td><strong>5.46W</strong></td>
<td>LX100</td>
<td>2.12W</td>
<td>660mW</td>
<td><strong>2.78W</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LX160</td>
<td>2.79W</td>
<td>935mW</td>
<td><strong>3.73W</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LX200</td>
<td>3.96W</td>
<td>1.04W</td>
<td><strong>5.00W</strong></td>
</tr>
</tbody>
</table>

**Virtex-4: 21% to 40% of Leakage Power from Vccaux Supply**
Static Power Comparison

Stratix II:  Typical Device, 25°C
Stratix II:  Worst-Case Device, 85°C
Virtex-4:  Typical Device, 25°C
Virtex-4:  Worst-Case Device, 85°C
3. I/O Power
I/O Power

- Dynamic Power to Charge Capacitance
- Also Static Power for Resistively Terminated Standards
  - e.g., SSTL
- Terminated I/O Standards: Some Power Dissipated as Heat in Off-Chip Resistors
  - Power Models Need to Report
    1. Power Dissipated as Heat on FPGA
    2. Power Drawn From Supply (Larger)
  - Stratix II Power Models Give Both Values
  - Competition: Only One Power Number

![FPGA Output Buffer Diagram](image)
Stratix II: Low I/O Power

- I/O Pins Are Large & Drive Large Capacitance → Large Power

- Stratix II I/O Pins: Less than ½ the Pin Capacitance of Competing FPGAs
  - Cuts Stratix II Output I/O Power
  - Also Saves Power on Chips Driving Stratix II Inputs

<table>
<thead>
<tr>
<th>I/O Type</th>
<th>Stratix II (Measured)</th>
<th>Virtex-4 (Measured)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Left/Right</td>
<td>5.0 pF</td>
<td>12.5 pF</td>
</tr>
<tr>
<td>Top/Bottom</td>
<td>6.1 pF</td>
<td>12.5 pF</td>
</tr>
</tbody>
</table>
I/O Power – Stratix II vs. Virtex 4

200-MHz, Single-Data Rate, 10pF Load

Virtex-4 “Total I/O Power”
Stratix II Thermal Power

Altera Early Power Estimator v2.1
Xilinx Web Power Tool v4.1
I/O Power: HSTL

Single-Ended HSTL 1.8V Class II
12 mA Virtex-4 / 16mA Stratix II
Pseudo-Random Bit Stream
I/O Power: SSTL

Single-Ended SSTL 1.8V Class II
12 mA Virtex-4 / 8 mA Stratix II
Pseudo-Random Bit Stream

17% More Power
Total Device Power Comparison
Stratix II & Virtex-4 Total Power Comparison

■ Operating Frequency & Activity
  − 200 MHz Clock, 12.5% Logic Toggle Rate

■ Design Resource Utilization – Apples-to-Apples
  − Logic: 75% of Stratix II
    ● Virtex-4: Same LE Count
  − RAM: 50% of Stratix II
    ● Virtex-4: Same Bit Count
  − DSP: 25% of Stratix II
    ● Virtex-4: Same 18x18 Multiplier Count
  − I/O: 30% of Stratix II Max I/O
    ● Virtex-4: Same I/O Count

■ Operating Conditions
  1. 25°C Ambient Temperature, Typical Device
  2. 85°C Junction Temperature, Worst-Case Device

■ Latest Power Estimators

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Total Device Power Comparison
200-MHz System, Typical Leakage Conditions

- Stratix II I/O & Dynamic
- Stratix II Static
- Virtex-4 I/O & Dynamic
- Virtex-4 Static

Device

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Total Device Power Comparison
200 MHz System, Worst-Case Leakage Conditions

- Stratix II I/O & Dynamic
- Stratix II Static
- Virtex-4 I/O & Dynamic
- Virtex-4 Static

Device

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Measured Complete Design (DES)

- Stratix II EP2S30 Meas.
- Stratix II EP2S15 Meas.
- Virtex-4 LX25 Meas.
Measured Complete Design (Rijndael)

- Stratix II EP2S30 Meas.
- Stratix II EP2S15 Meas.
- Virtex-4 LX25 Meas.
Any Power-On Surge Current?
Start-Up / In Rush Current

- No Current Spike on Power-Up
  - Many Older FPGAs Had High Power-Up Current Requirements
  - Due to Contention in Configuration SRAM
  - Stratix II Production Devices: **Power-Up Is Contention-Free**
    - Some EP2S60 Engineering Samples Had Small Surge; Fixed in Production Silicon
Power Up: No Surge!

Typical FPGA

Stratix II

Improved Stratix II Power-Up Profile

Current

Time

Power Up

Static

Total Power (Dynamic+Static)
HardCopy II Structured ASICs
Migrate to the Lowest Power
HardCopy II Overview

- Lowest-Risk Structured ASIC
- Seamless Migration Path From Stratix II Design to HardCopy II
  - Same Design Software: Quartus II
  - Same IP Available
  - Functional Equivalence Guaranteed
HardCopy II Routing Power

- FPGA Programmable Routing
  - Long Pre-Fabricated Wires
  - Pre-Fabricated Muxes & Buffers
  → High Capacitance!

- HardCopy II: Custom Metal Routing
  - No Muxes
  - Only Exact Wires & Buffers Needed

- Logic Density Higher
  - Shorter Routes

- **20X Less Routing Capacitance!**
HardCopy II Leakage & Logic Power

- Far Fewer Transistors than an FPGA → Lower Leakage

- FPGA Logic Cells
  - Internal Multiplexers Select Mode & Logic Function

- HardCopy II HCell Architecture
  - Simpler Gates; Use Metal Connections to Configure
  - 5 to 10X Less Logic Dynamic Power
HardCopy II Power Advantage

Example: High-Speed, High-Density Stratix II Design

2.5X Total Power Reduction

Power (W)

Stratix II

HardCopy II

I/O
RAM & DSP
Leakage
Logic
Routing & Clocks

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Great Performance While Managing Power

187 Designs Conclusively Validate Altera’s Performance Advantage

Altera FPGA Design $f_{\text{MAX}}$ (MHz)

Xilinx® FPGA Design $f_{\text{MAX}}$ (MHz)

- Stratix II vs. Virtex-4
- Cyclone/Cyclone II vs. Spartan-3
- 77 Designs Target Stratix II & Virtex-4;
- 110 Designs Target Cyclone/Cyclone II & Spartan-3

For details on methodology, see Altera’s FPGA Performance Benchmarking Methodology White Paper

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Summary

- Total Device Power Is What Matters
  - 90-nm FPGAs Have Best Total Device Power

- Accurate Power Estimation
  - Requires Good Power Models
  - Sum Power of All Voltage Rails
  - Consider Worst-Case Silicon

- Stratix II
  - Best Performance at 90 nm
  - Total Device Power Better than Competition for High Speed Designs

- HardCopy II Reduces Power Even Further
  - Achieves Power Efficiency Beyond Any FPGA
Resources & More Information

  - Stratix II Early Power Estimator v2.1 (Spreadsheet)
  - Power Basics
  - Certified Power Partner Solutions
  - AN 378: Stratix II Low Power Design Techniques (PDF)
  - AN 355: Stratix II Device Power Considerations (PDF)
  - AN 358: Thermal Management for 90nm FPGAs (PDF)
  - User Guide: PowerPlay Early Power Estimator (Coming Mid-05)

- Quartus II Handbook – PowerPlay Sections
  - Early Power Estimator (Vol. 3 Chapter 7)
  - Power Analyzer (Vol. 3 Chapter 8)

- Stratix II 90-nm Silicon Power Optimization
Thank You
For More Information
Visit www.altera.com