Power Solutions for Leading-Edge FPGAs

Vaughn Betz & Paul Ekas

Agenda

- 90 nm Power Overview
- Stratix II®: Power Optimization Without Sacrificing Performance
  - Technical Features & Competitive Results
    - Dynamic Power
    - Static Power
    - I/O Power
- HardCopy® II Structured ASICs: The Path to Lowest Power
- Summary & Wrap Up

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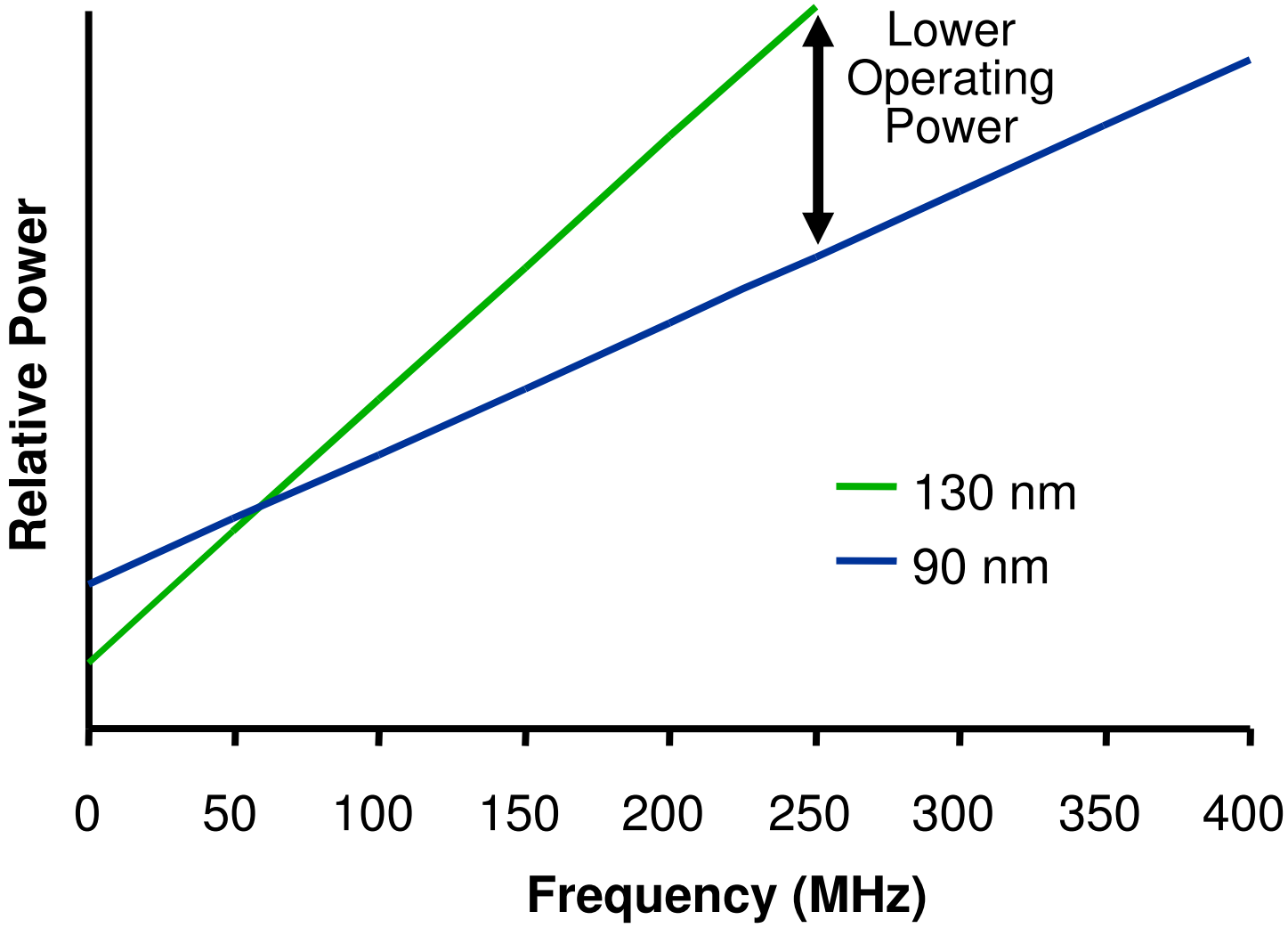
90 nm Power Overview

90 nm: Operating Power Reduced



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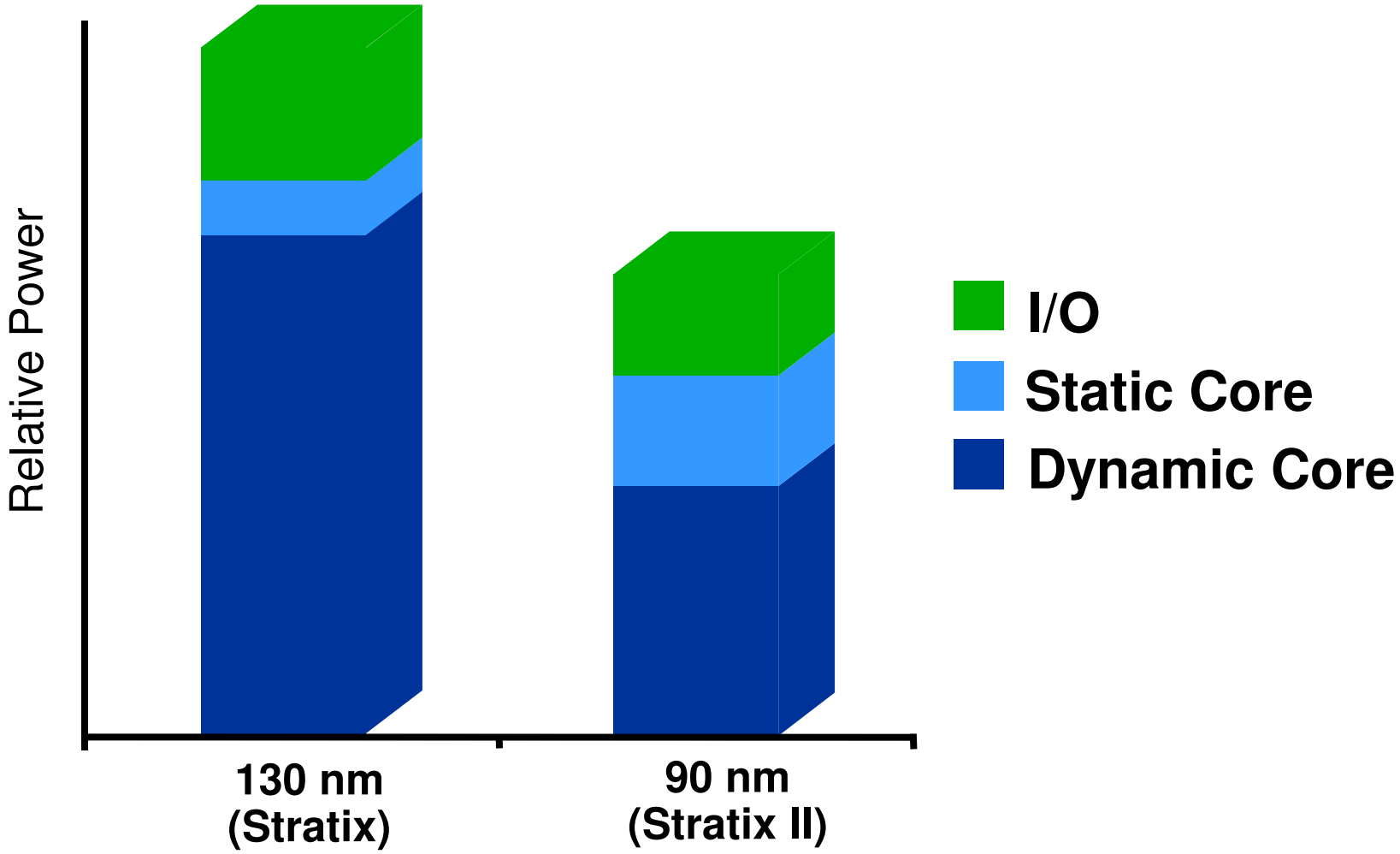
Power Breakdown: 90 nm vs. 130nm



Power: 90 nm vs. 130 nm

- Large Dynamic Power Reduction
  - Dominant Power, so Most Important
- Static Power Increases
  - Need to Architect FPGA to Minimize Increase
  - Without Sacrificing 90 nm Performance
- I/O Power Does Not Scale with Process
  - Need to Improve Circuit Design to Get Gains

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Stratix II FPGAs

Power Optimization Without Sacrificing Performance

Power Versus Performance

The Major Challenge for 90-nm High-Performance FPGAs

- Stratix II: Most Performance Within Power Budget
  - Minimize Power for Non-Performance Critical Circuitry
    - "Black Diamond" Low-K Dielectric
    - Increased V_T
    - Increased Gate Length
  - Maximize Performance Where Needed
    - Adaptive Logic Module (ALM) Architecture
    - "Black Diamond" Low-K Dielectric
    - Lower V_T Only Where Needed
    - Shorter Gate Length Only for Most Performance Critical
  - Redesign I/Os for Minimum Power

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1. Dynamic Power

Core Dynamic Power

- Usually Most Important Power Component
- Power Proportional to Clock Frequency

$$P_{dynamic} = \left[\frac{1}{2} CV^2 + Q_{ShortCircuit} V \right] f \cdot activity$$

- 1st Term: Capacitance Charging
  - Dominant Dynamic Power Component
- 2nd Term: Short Circuit Charge During Switching
  - Smaller Component
- Activity: % of Circuit That Switches Each Cycle
  - Highly Design Dependent
- Little Dependence on Temperature or Process Variation

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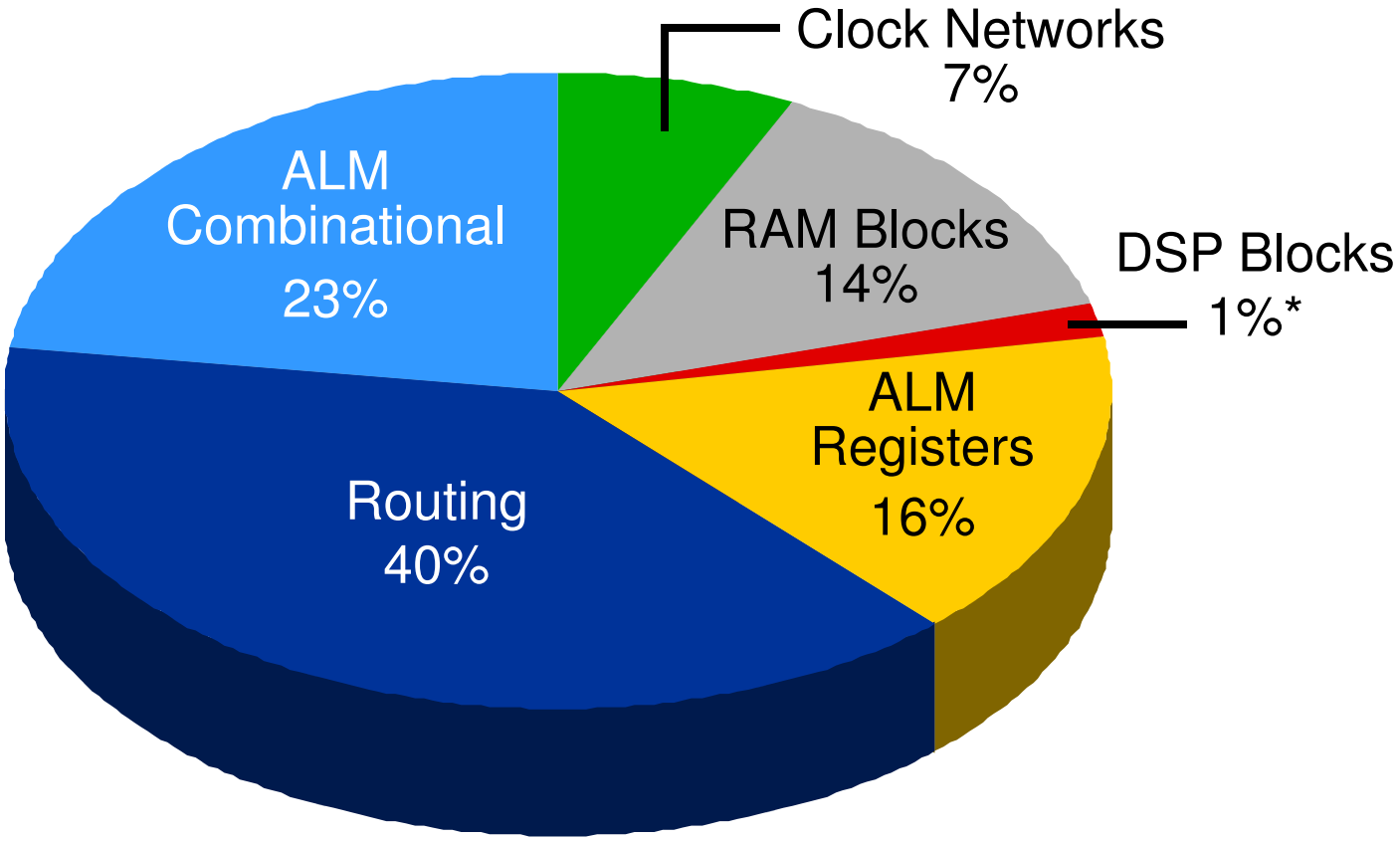
Core Dynamic Power

- Typical Breakdown (112 Customer Design Average)



*DSP Block Power: 5% of Dynamic Power for Designs that Use DSP Blocks

Minimizing Dynamic Power: Low-k

- Stratix II: Black Diamond Low-k Dielectric
  - Metal Capacitance ∝ k (Dielectric Constant)
  - Dynamic Power ∝ Capacitance Charged
    - Metal Capacitance is Dominant
  - Black Diamond: k = 2.9
  - FSG ("Reduced-k"): k = 3.6
  - Black Diamond Reduces Metal Capacitance by **20%** vs. FSG Used by Competing FPGAs!
- Result: 14% Dynamic Power Reduction ***and*** 12% Speed Improvement

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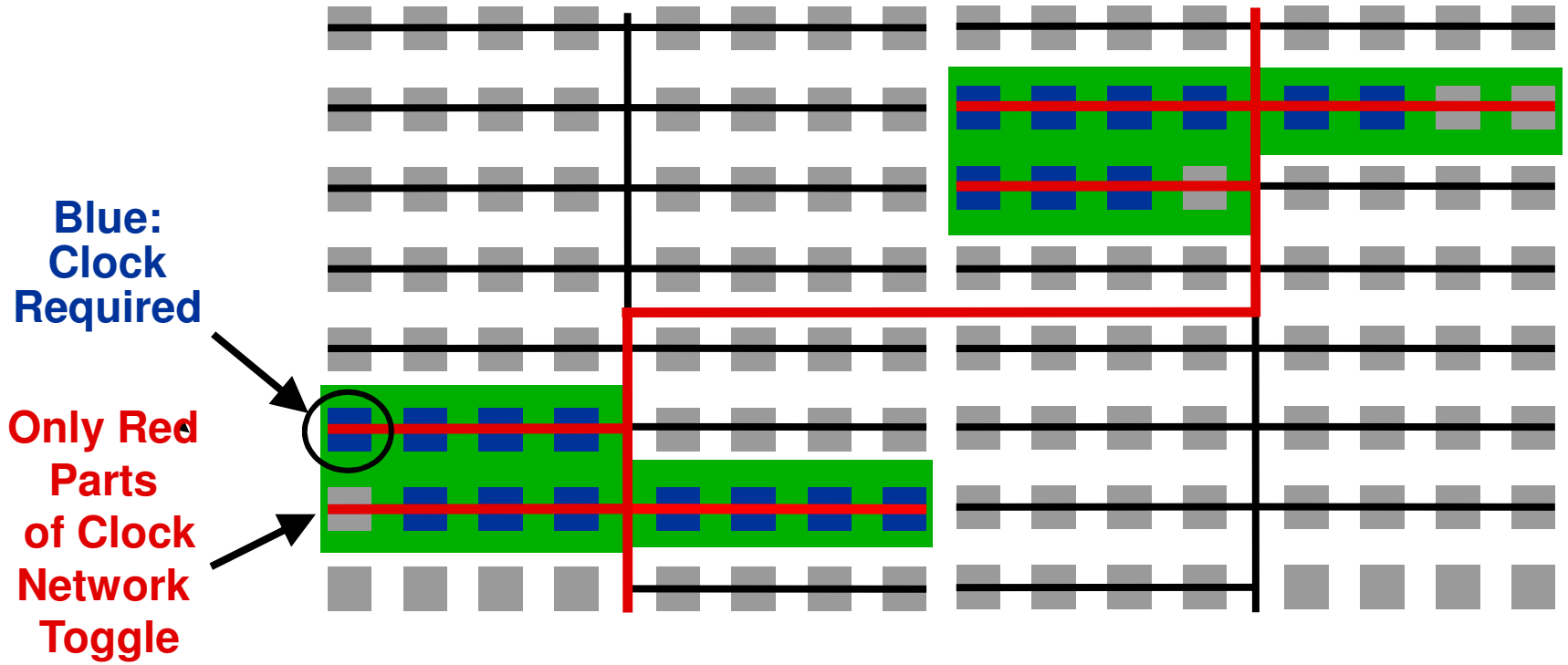
Minimizing Dynamic Power: Clocking

- Stratix II FPGA Shuts Down Unused Parts of Clock Networks
  - With Fine Control Granularity (Nearly 800 Regions!)
  - Automatically Implemented for Each Design by Quartus® II Software



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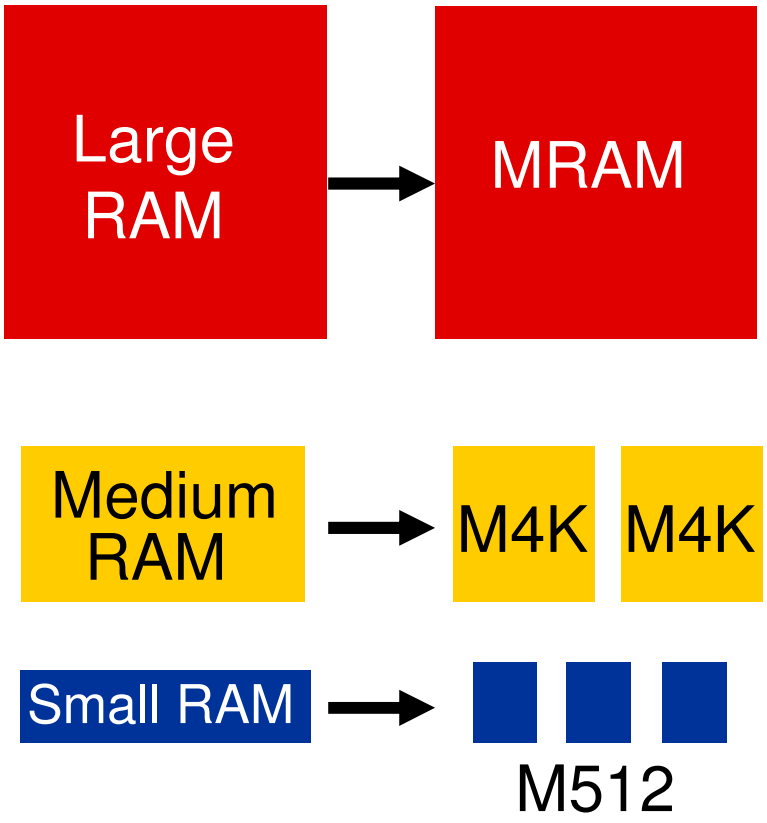
Minimizing Dynamic Power: RAM

- Tri-Matrix Memory
  - Power Inefficient to Use a Large Physical RAM for a Small Memory or Vice Versa
  - Stratix II FPGA: 3 RAM Sizes
  - Quartus II Software Automatically Picks Good Physical RAM
- Shut Down RAM Core When Clk Enable Low
  - Near 0 Dynamic Power on Cycles Where RAM Not Accessed
  - Quartus II Release 5.0 Automates When Possible



Basic Blocks: Power Estimators

- Compare Component Power for Stratix II & Virtex-4 FPGAs
- Using Latest Power Estimators
  - Altera Early Power Estimator Version 2.1
  - Xilinx Power WebTool Version 4.1
- Measure All Power Sources
  - Stratix II FPGA
    - V_{CCINT}: Internal Core Power
    - V_{CCIO}: I/O Power
    - V_{CCPD}: Pre-Drive Power for I/O
  - Virtex-4 FPGA
    - V_{CCINT}: Internal Core Power (Most Internal Circuitry)
    - V_{CCO}: I/O Power
    - V_{CCAUX}: Powers Some Internal Circuitry

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Dynamic Power: Logic & Routing

- Power = # LUTs x Power per (LUT + Routing)

200 MHz, 30% Toggle	Stratix II (mW)	Virtex-4 (mW)	% Diff
1 LUT/ALUT + FF + Typical Routing	0.147	0.157	-6%
Stratix II: 18% Fewer ALUTs per Circuit	0.121 (eq. logic)	0.157	-23%

Stratix II Family Has Lower Power in Logic & Routing

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Dynamic Power: Memory

- 200 MHz Dual-Port (1 Read, 1 Write) Synchronous RAM

Size (bits)	Width x Depth	Stratix II (mW)	Virtex-4 (mW)	% Diff
512	16 x 32	4.1	9.9	-58%
4K	8 x 512	6.9	11.3	-39%
16K	16 x 1024	15.6	12.3	+27%
	128 x 128	33.8	62.4	-46%
512K	64 x 8192	218	339	-36%

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Dynamic Power: DSP & PLL

Block @ 200 Mhz	Stratix II (mW)	Virtex-4 (mW)	% Diff
18x18 Multiplier	8.0	10.0	-20%
9x9 Multiplier	3.5	<10.0	-65%
36x36 Multiplier	20.5	45.6	-55%
400 MHz PLL/DCM	23	119	-81%
100 MHz PLL/DCM	17	38	-55%

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Basic Blocks: Measured Power

- Lab Measurements of Power Consumed per Basic Block
  1. Measure Power With Only Test Circuitry
  2. Measure Power With Test Circuitry & Basic Block of Interest
  3. Subtract to Obtain Power for Basic Block
- Nominal Voltage
- Ambient Temperature = 25°C
  - Recall: Very Little Impact on Dynamic Power

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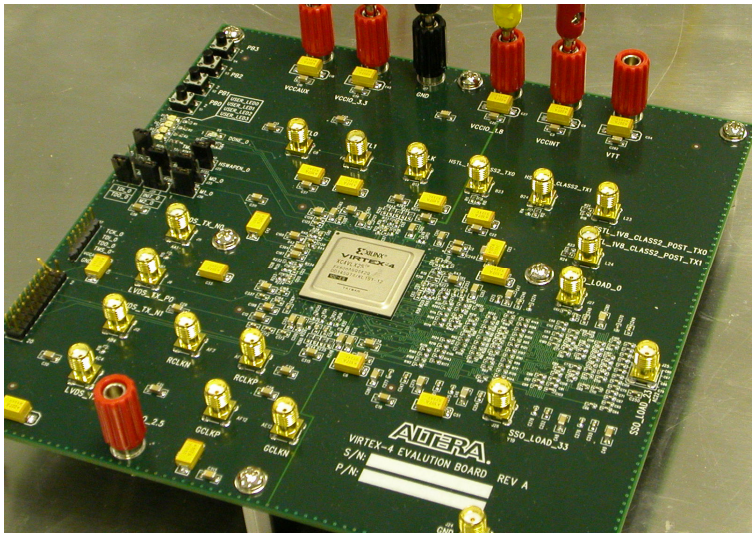
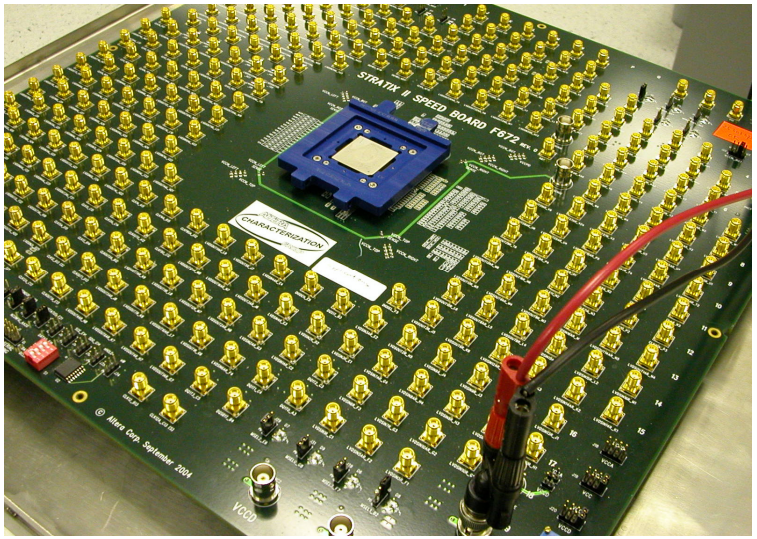
Devices & Boards Used





Family	Device	Equiv. LEs
Stratix II	EP2S15	15,600
Virtex-4	4VLX25	21,504
Stratix II	EP2S30	33,880
Stratix	EP1S25	25,660

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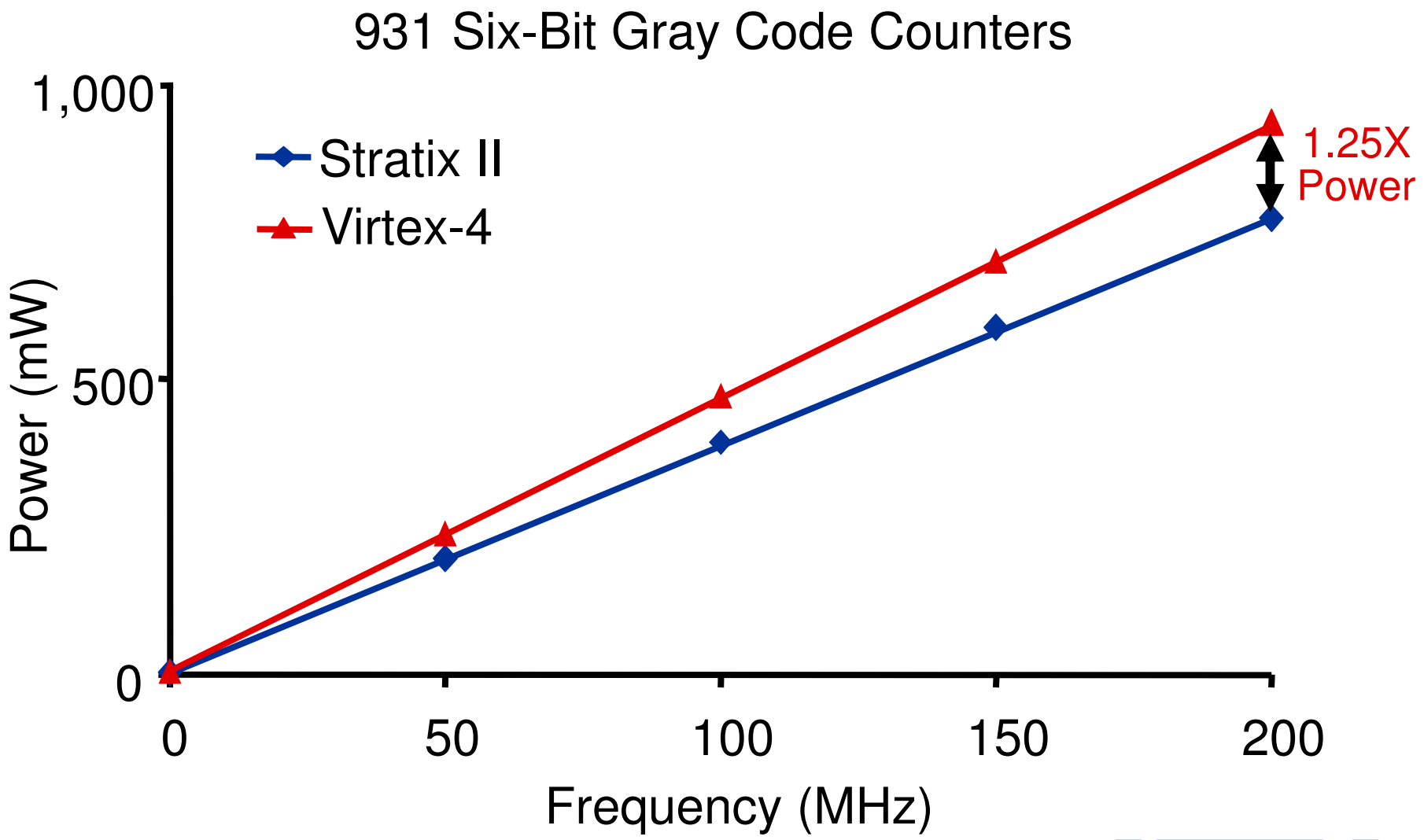
Dynamic Power: Logic



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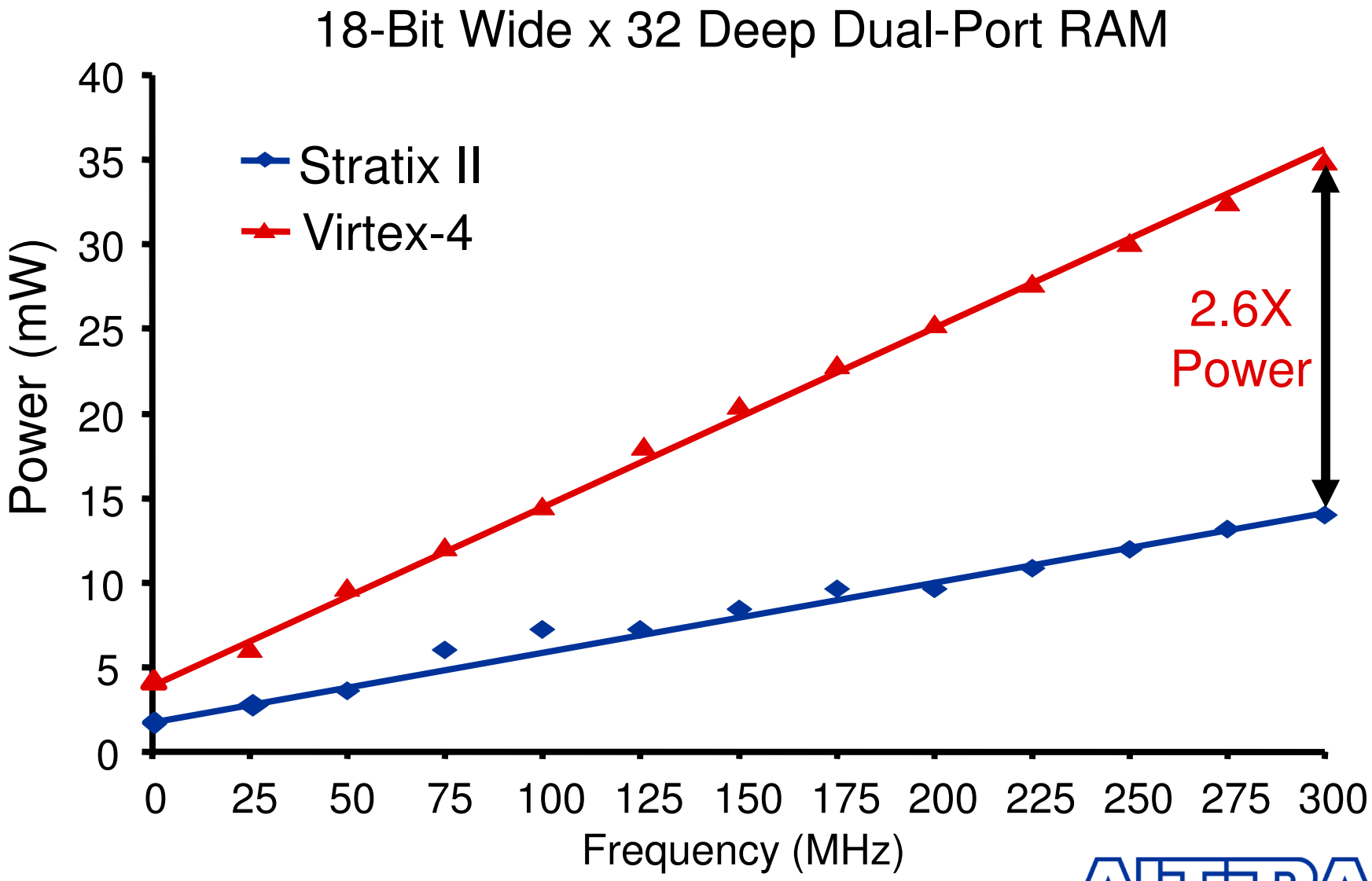
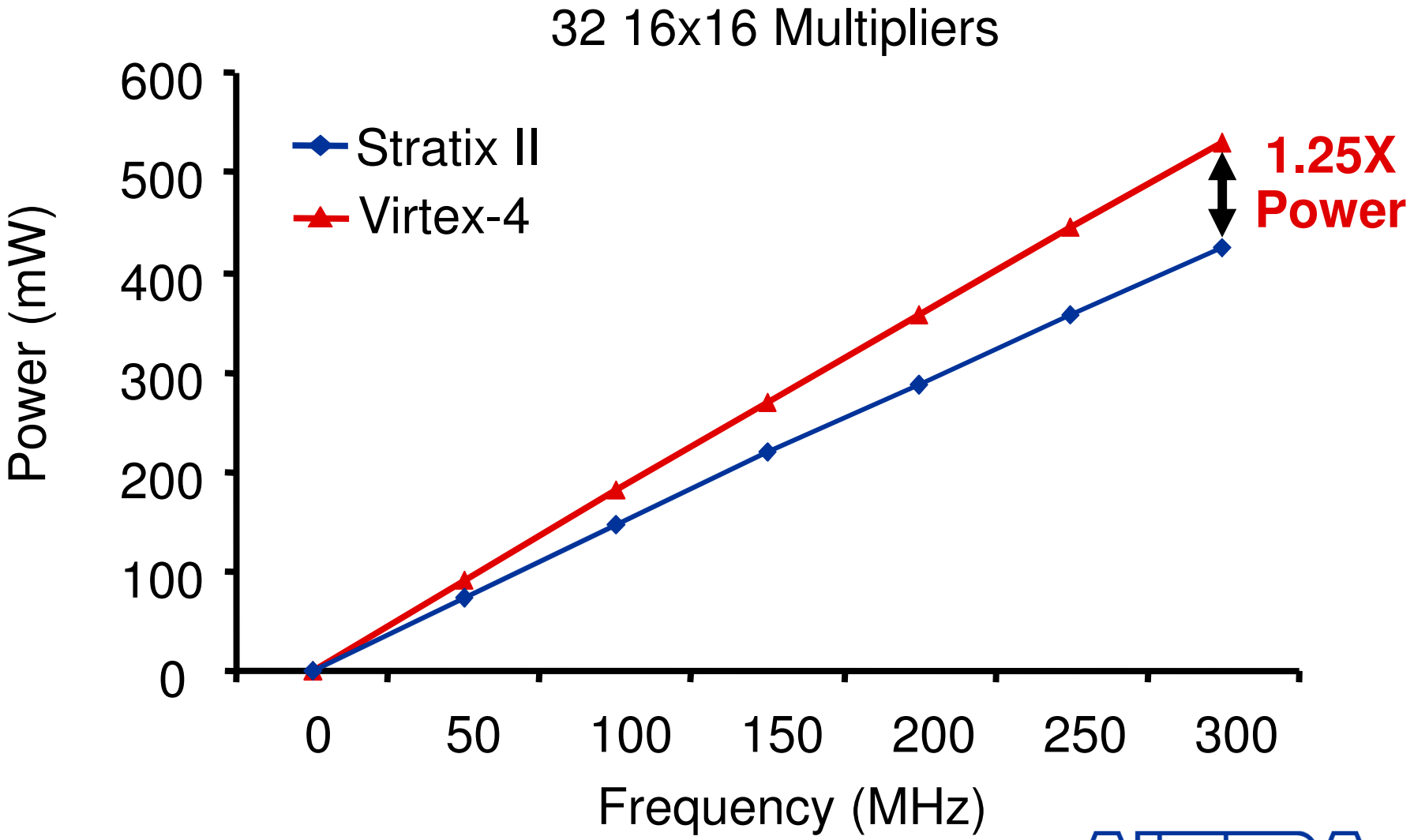
Dynamic Power: RAM



Dynamic Power: DSP



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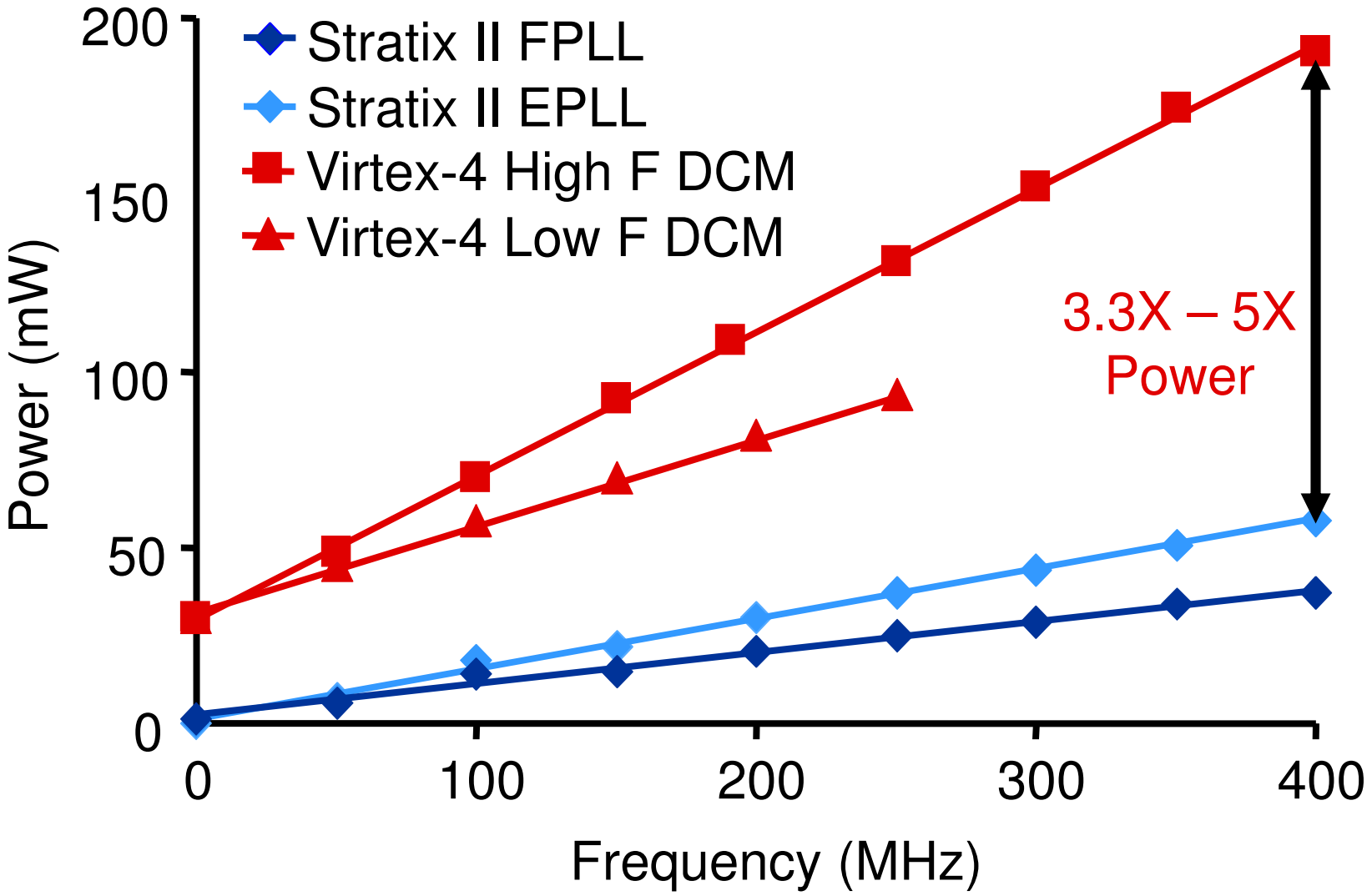
DCM/PLL Power



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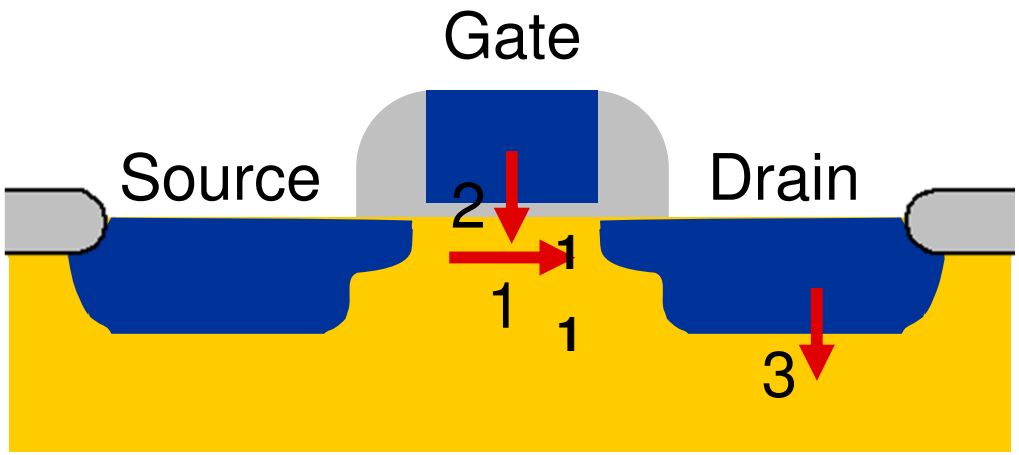
2. Static Power

Static Power

1. Subthreshold Leakage from Source to Drain of Off Transistors
   - Main Leakage Component at 90 nm
   - Increases Rapidly with Temperature
   - Highly Dependent on Process Variation
2. Gate Leakage (Smaller)
3. Reverse-Biased Junction Leakage (Very Small)



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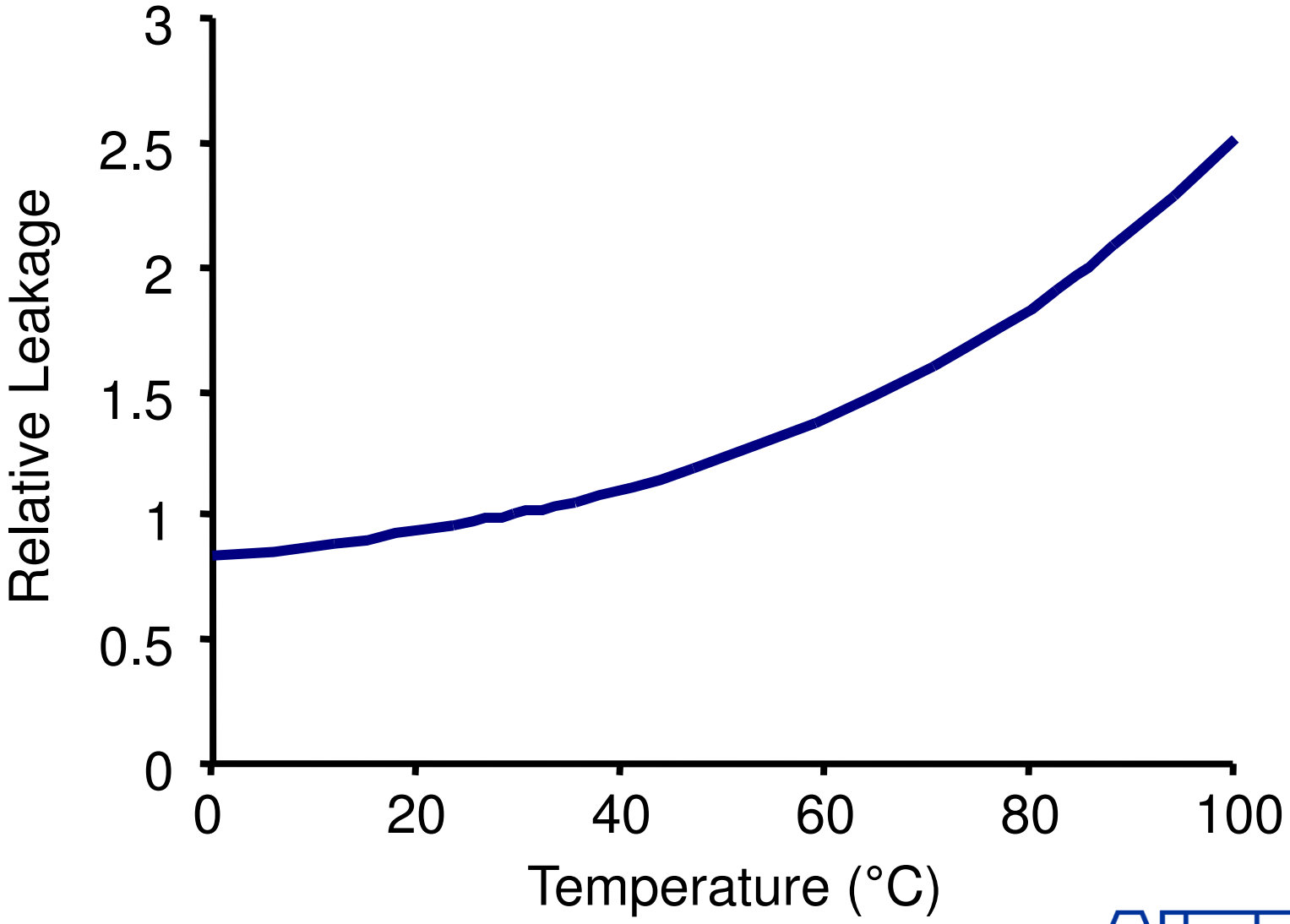
Leakage Power: Temperature Effect



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Stratix II Leakage Power Reduction

- High-Vt Transistors Where Not Speed-Critical
  - Especially Configuration SRAM
  - 10X Leakage Reduction
- Longer Channels for Most Transistors
  - Significant Leakage Reduction
  - Reduces Leakage Variability Across Process
    - Helps **Worst-Case Leakage** Most!

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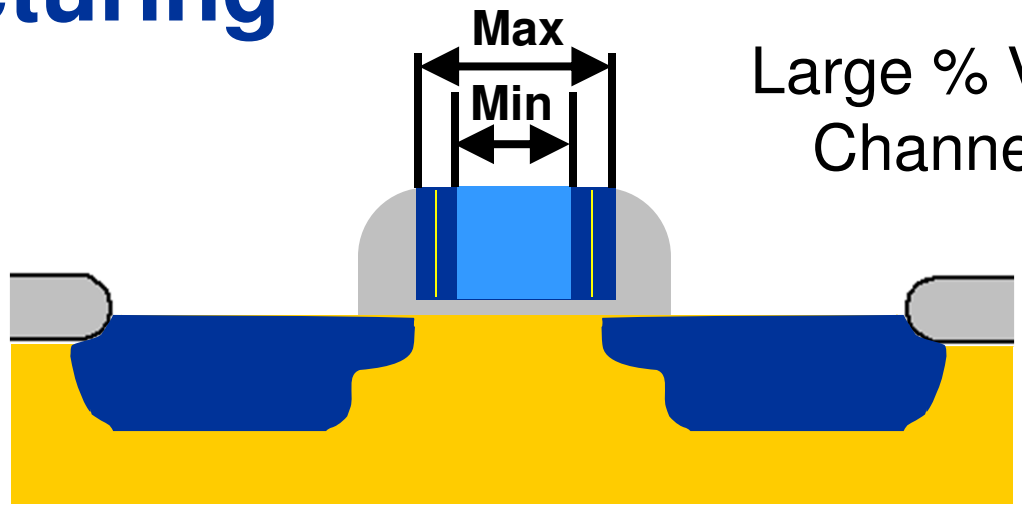
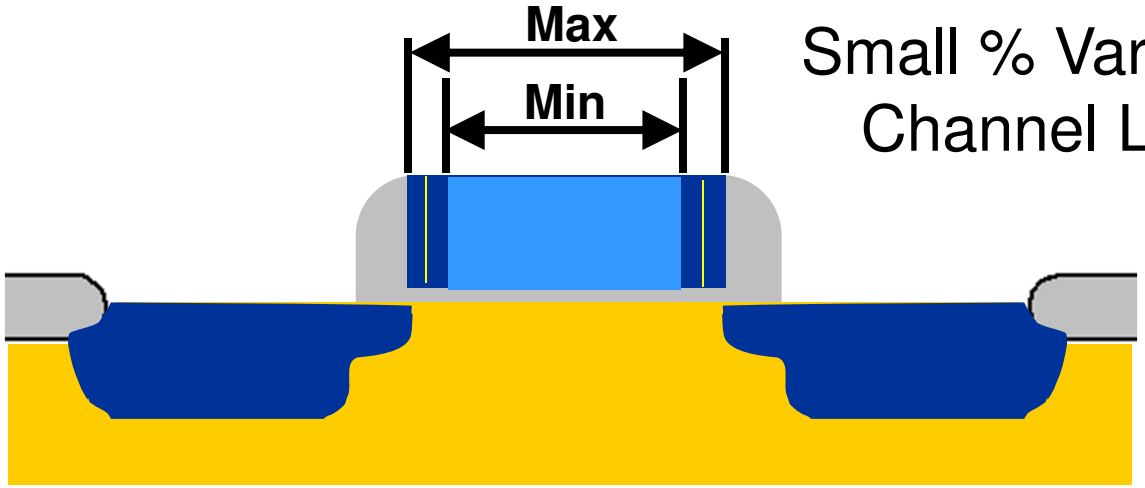
Channel Length Variation Due To Manufacturing

Short Gate



Large % Variation of Channel Length

Long Gate



Small % Variation of Channel Length

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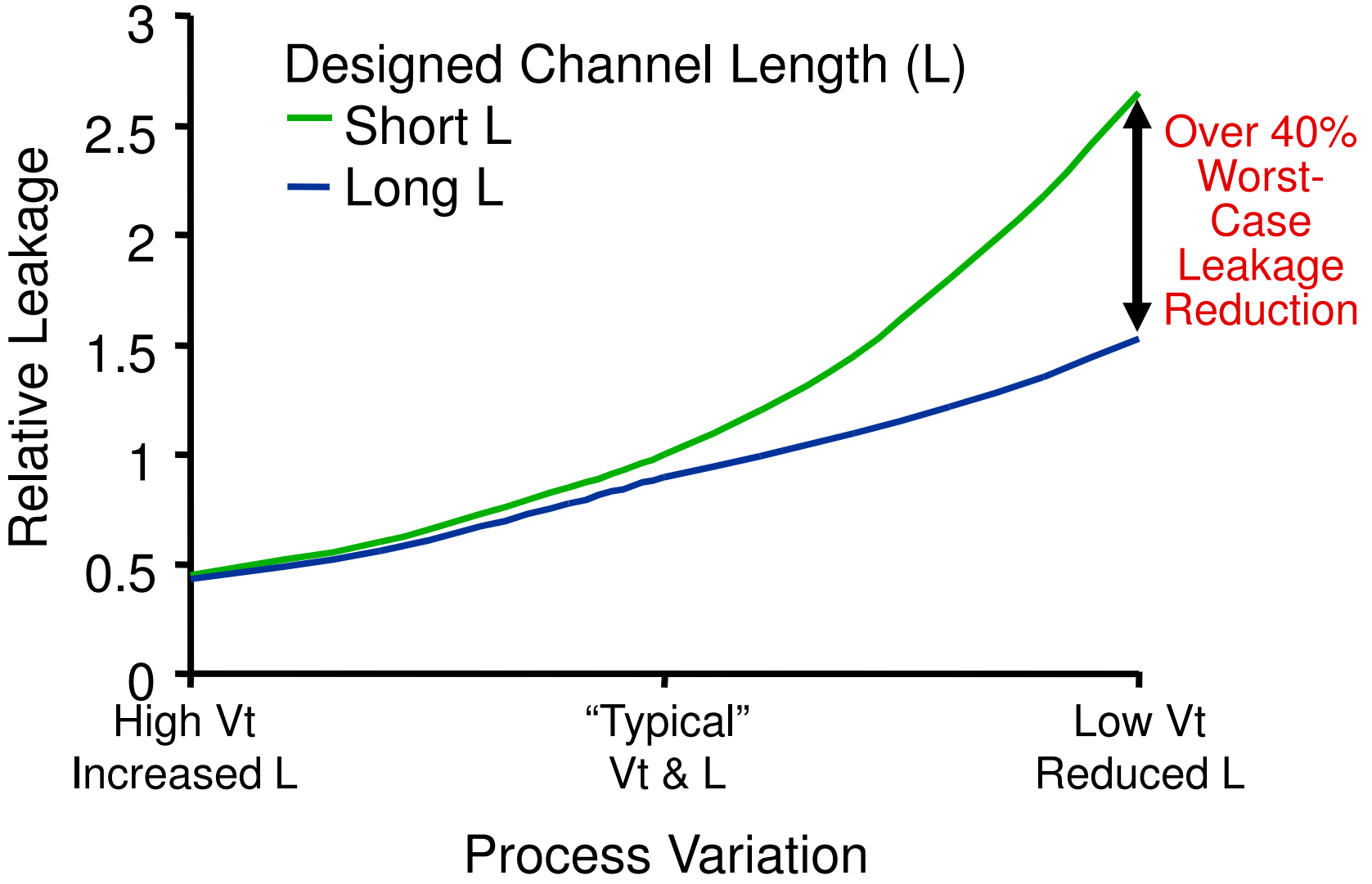
Process Variation Impact On Leakage



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Static Power Comparison

- Using Latest Altera & Xilinx Power Estimators
  - Sum Static Power From All Relevant Supplies
    - Vccint & Vccpd for Stratix II FPGA
    - Vccint & Vccaux for Virtex-4 FPGA
- Most Important Comparison: Worst-Case Device Leakage Values
    - Using Typical Values Means **50%** of Devices You Receive Will Have Power Greater Than You Model!
    - Stratix II Early Power Estimator Includes Worst-Case Models
    - Virtex-4 Power Tool: Multiply Typical Static Power by 2.5X (Xilinx Guidance to Customers)

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Static Power Comparison

Altera Stratix II (85°C Worst Case)				Xilinx Virtex-4 (85°C Worst Case)			
Part	Power V_{CCINT}	Power V_{CCPD}	Total Static Power	Part	Power V_{CCINT}	Power V_{CCAUX}	Total Static Power
EP2S15	792mW	33mW	**825mW**	LX15	345mW	230mW	**575mW**
				LX25	568mW	262mW	**830mW**
EP2S30	1.13W	66mW	**1.19W**	LX40	892mW	305mW	**1.20W**
EP2S60	2.16W	76mW	**2.24W**	LX60	1.22W	530mW	**1.74W**
				LX80	1.60W	585mW	**2.18W**
EP2S90	3.16W	82mW	**3.24W**	LX100	2.12W	660mW	**2.78W**
EP2S130	4.32W	99mW	**4.42W**	LX160	2.79W	935mW	**3.73W**
EP2S180	5.34W	116mW	**5.46W**	LX200	3.96W	1.04W	**5.00W**

Virtex-4: 21% to 40% of Leakage Power from Vccaux Supply

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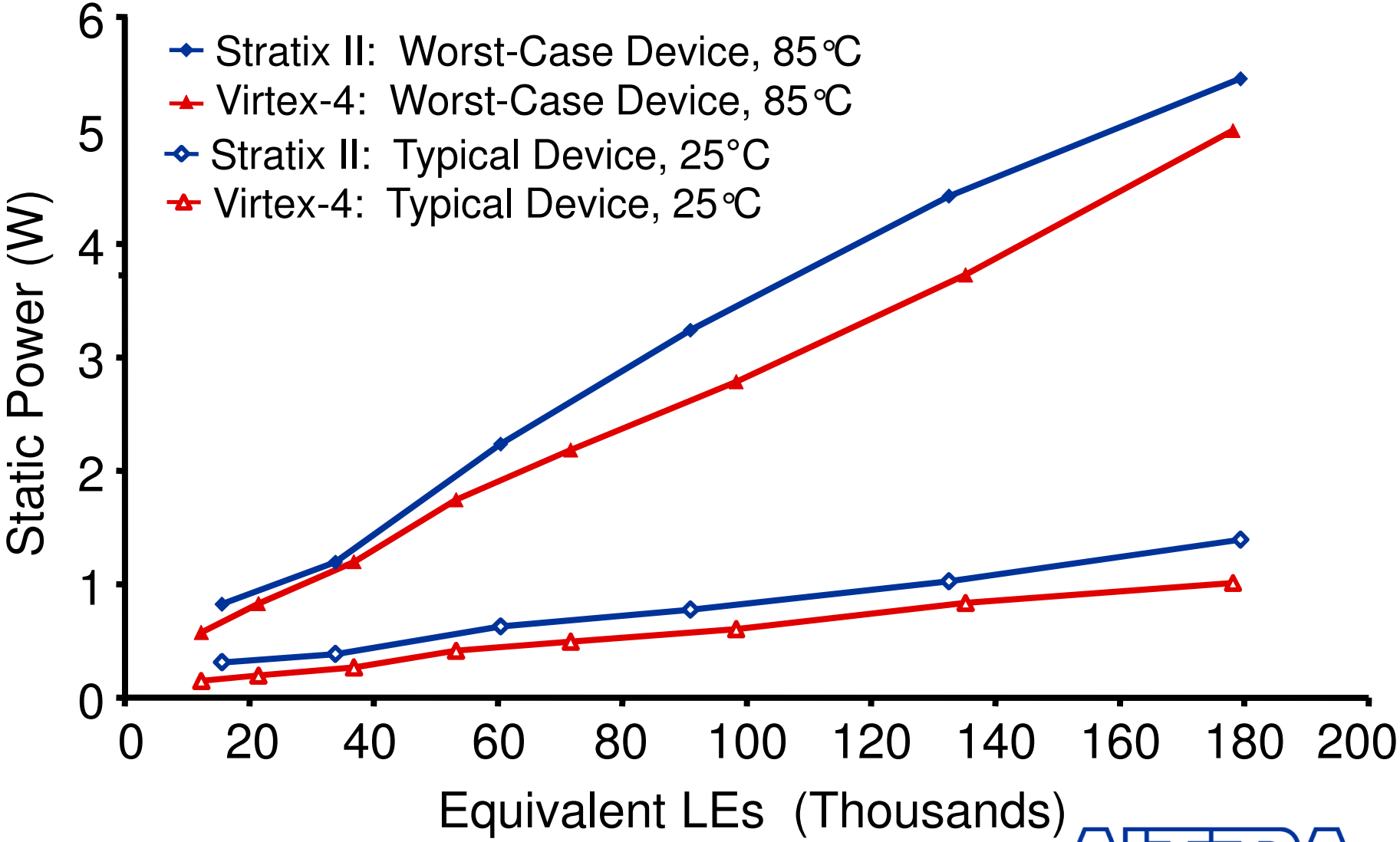
Static Power Comparison



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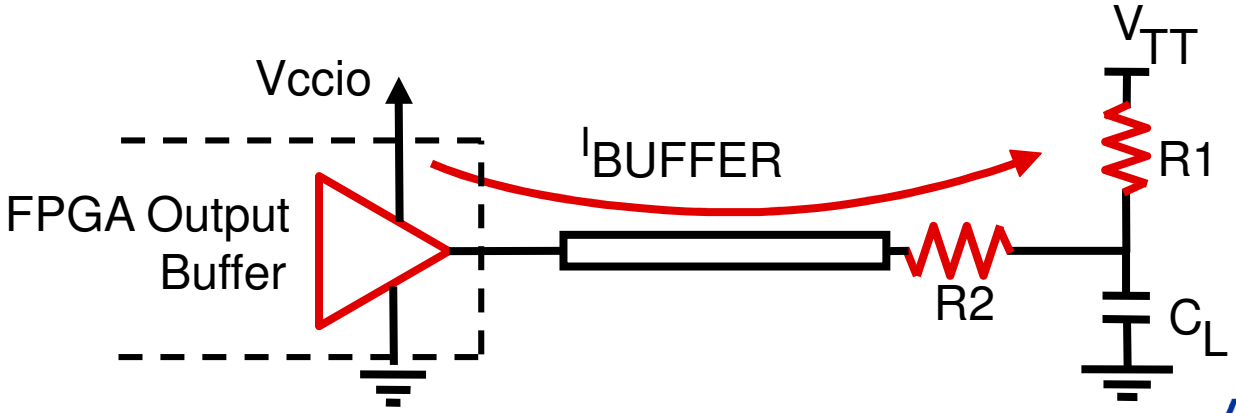
3. I/O Power

I/O Power

- Dynamic Power to Charge Capacitance
- Also Static Power for Resistively Terminated Standards
  - e.g., SSTL
- Terminated I/O Standards: Some Power Dissipated as Heat in Off-Chip Resistors
  - Power Models Need to Report
    1. Power Dissipated as Heat on FPGA
    2. Power Drawn From Supply (Larger)
  - Stratix II Power Models Give Both Values
    - Competition: Only One Power Number



Stratix II: Low I/O Power

- I/O Pins Are Large & Drive Large Capacitance
  →Large Power
- Stratix II I/O Pins: Less than ½ the Pin Capacitance of Competing FPGAs
  - Cuts Stratix II Output I/O Power
  - **Also Saves Power on Chips Driving Stratix II Inputs**

I/O Type	Stratix II (Measured)	Virtex-4 (Measured)
Left/Right	5.0 pF	12.5 pF
Top/Bottom	6.1 pF	12.5 pF

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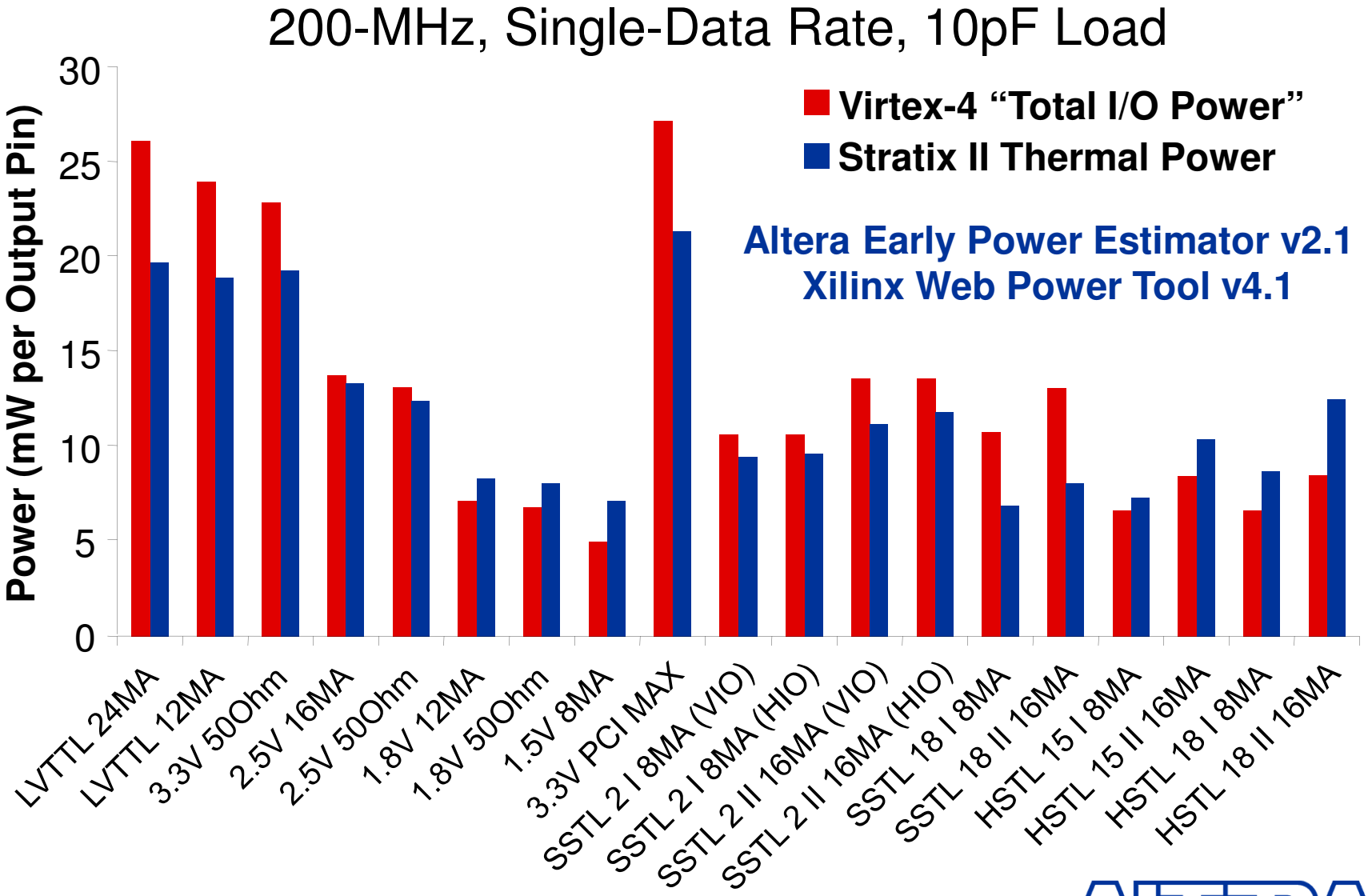
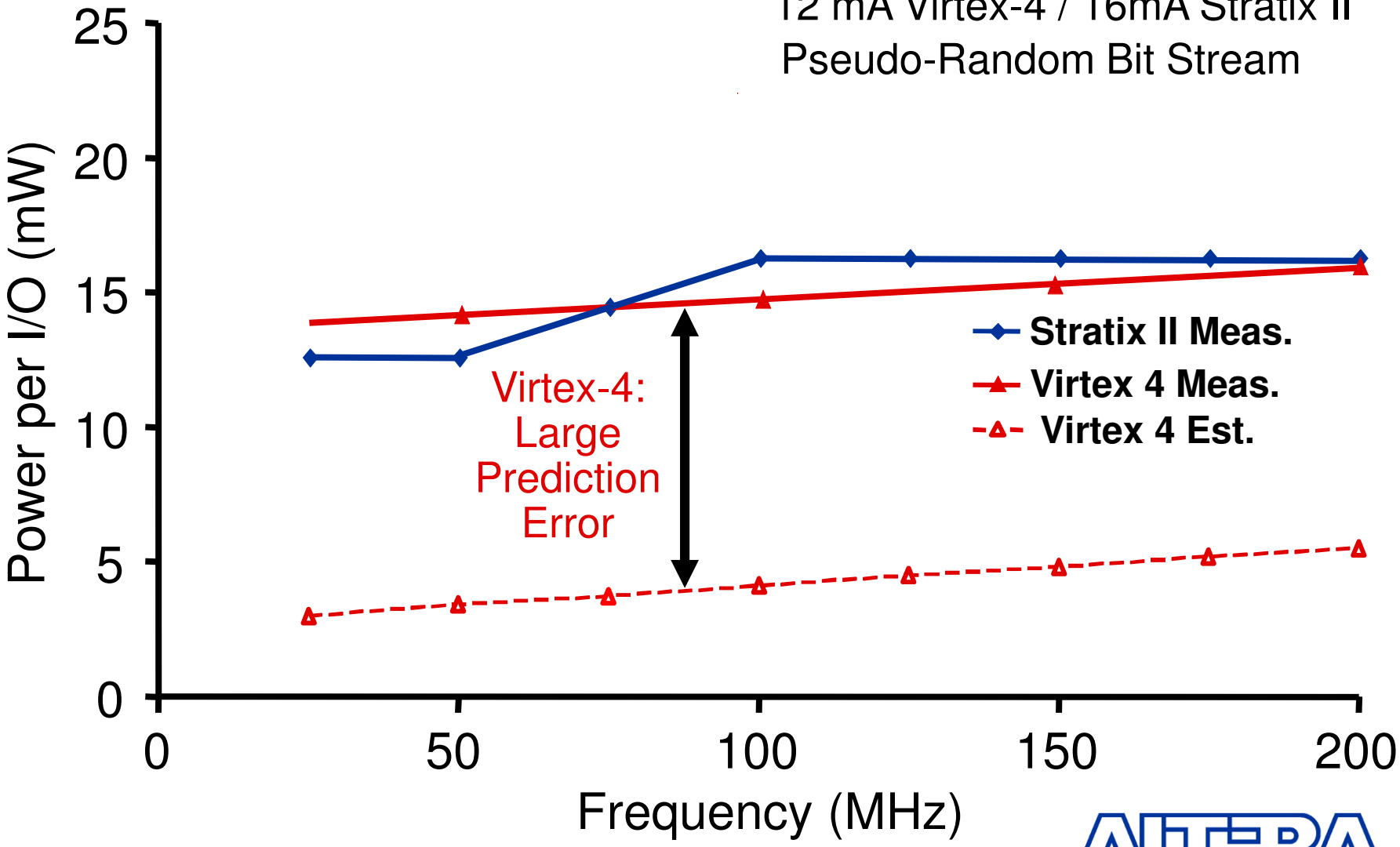
I/O Power – Stratix II vs. Virtex 4



I/O Power: HSTL

Single-Ended HSTL 1.8V Class II
12 mA Virtex-4 / 16mA Stratix II
Pseudo-Random Bit Stream



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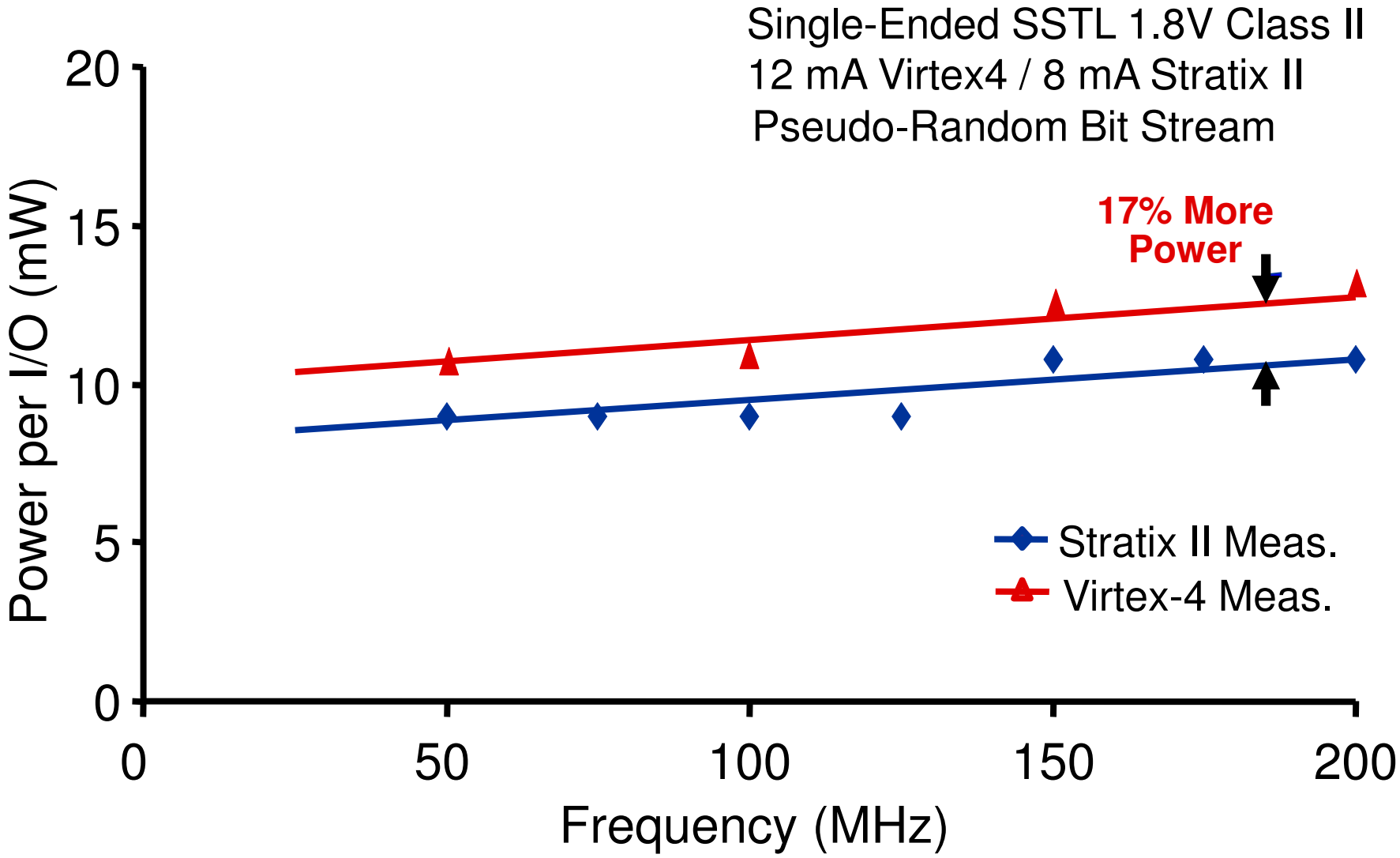
I/O Power: SSTL



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Total Device Power Comparison

Stratix II & Virtex-4 Total Power Comparison

- Operating Frequency & Activity
  - 200 MHz Clock, 12.5% Logic Toggle Rate
- Design Resource Utilization – Apples-to-Apples
  - Logic: 75% of Stratix II
    - Virtex-4: Same LE Count
  - RAM: 50% of Stratix II
    - Virtex-4: Same Bit Count
  - DSP: 25% of Stratix II
    - Virtex-4: Same 18x18 Multiplier Count
  - I/O: 30% of Stratix II Max I/O
    - Virtex-4: Same I/O Count
- Operating Conditions
  1. 25°C Ambient Temperature, Typical Device
  2. 85°C Junction Temperature, Worst-Case Device
- Latest Power Estimators

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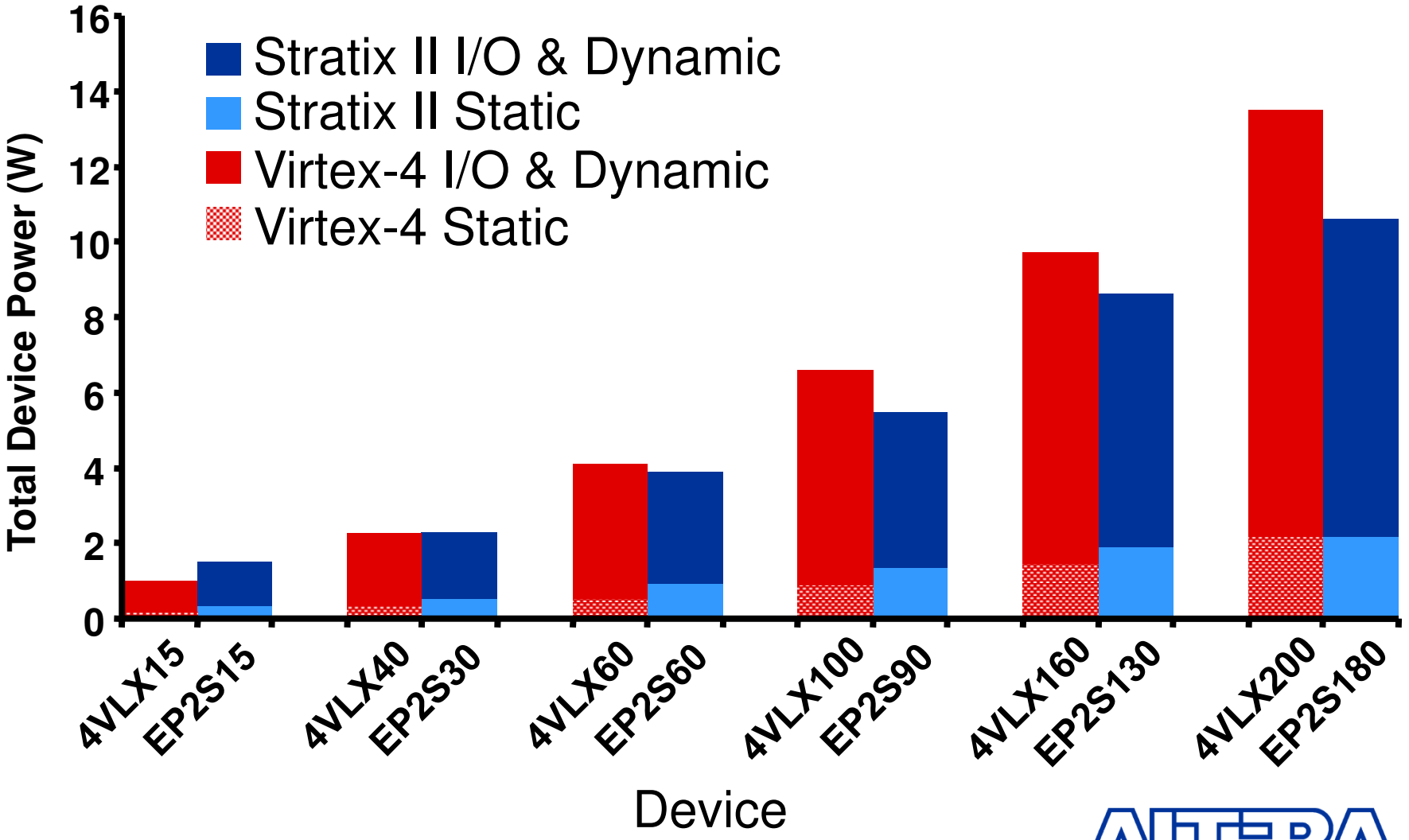
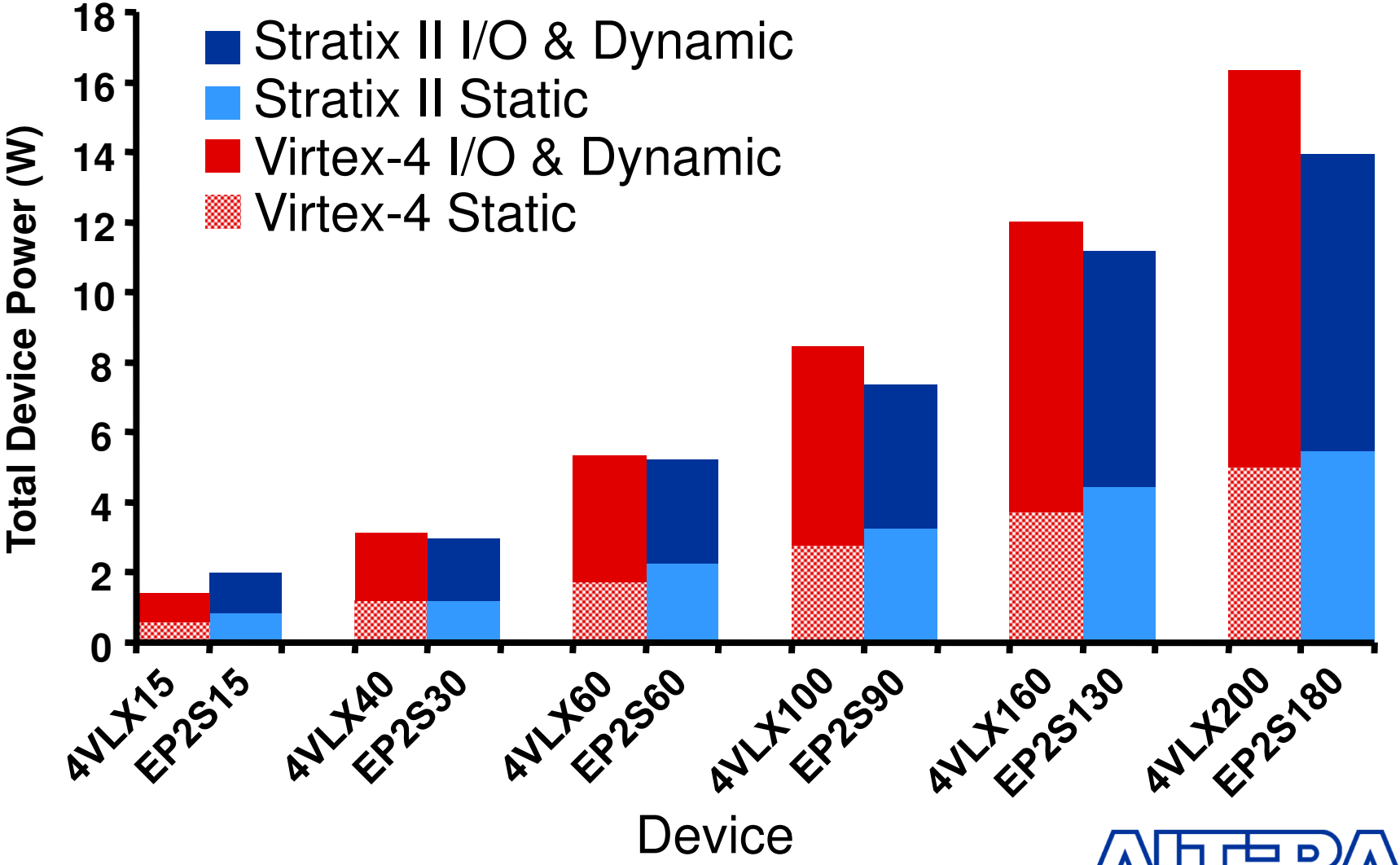
Total Device Power Comparison

200-MHz System, Typical Leakage Conditions



Total Device Power Comparison

200 MHz System, Worst-Case Leakage Conditions



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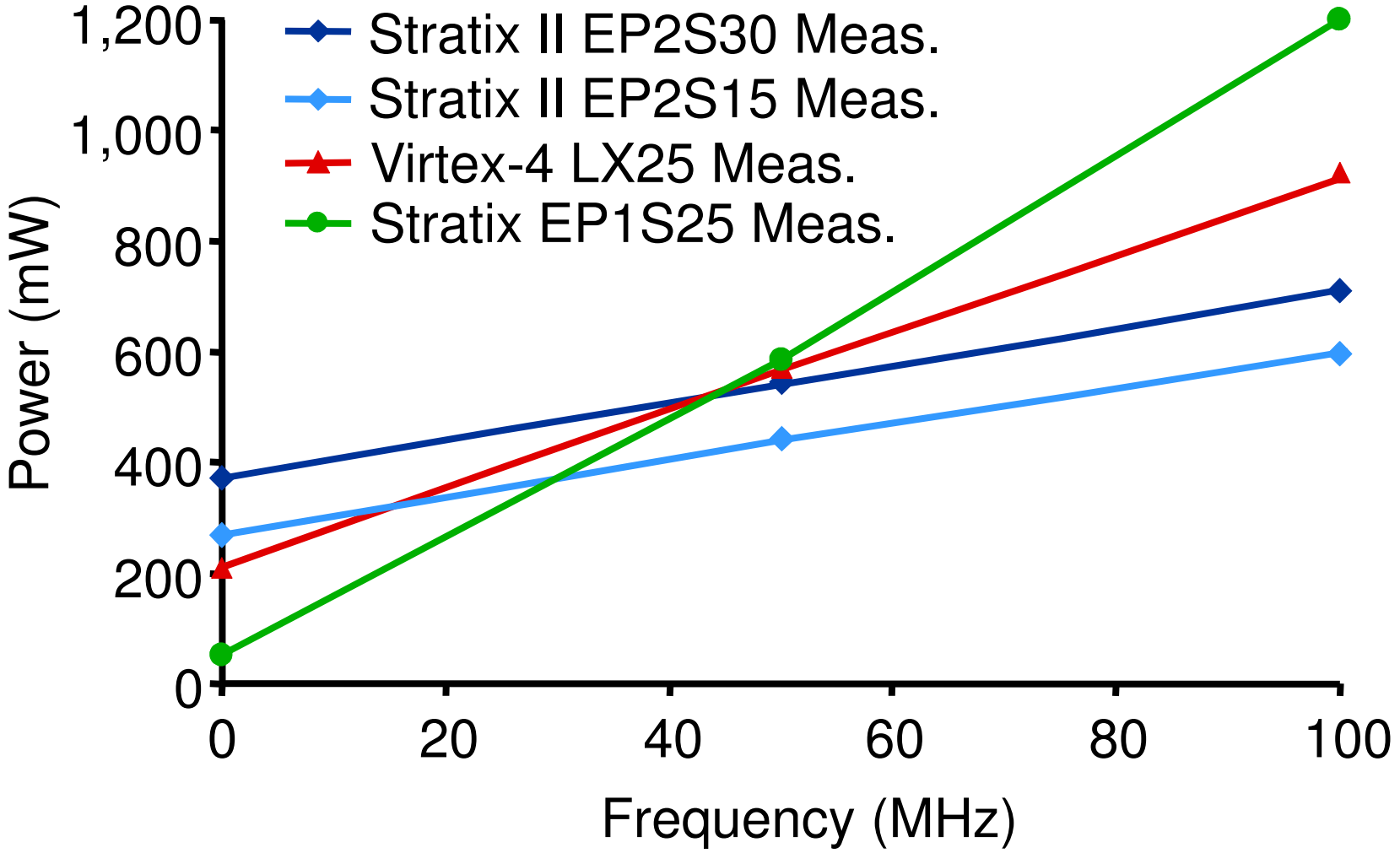
Measured Complete Design (DES)



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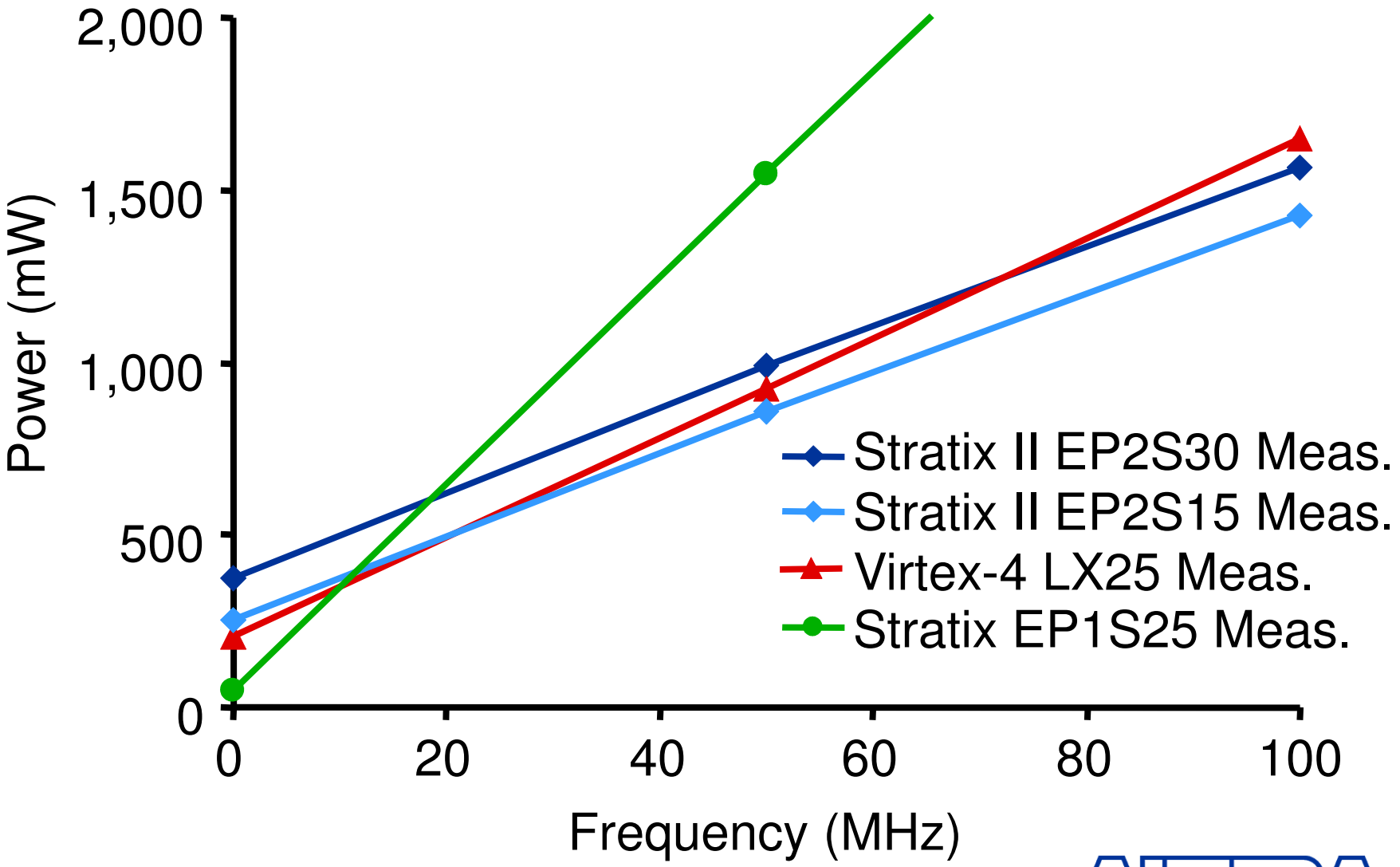
Measured Complete Design (Rijndael)



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Any Power-On Surge Current?

Start-Up / In Rush Current

- No Current Spike on Power-Up
  - Many Older FPGAs Had High Power-Up Current Requirements
  - Due to Contention in Configuration SRAM
  - Stratix II Production Devices: **Power-Up Is Contention-Free**
    - Some EP2S60 Engineering Samples Had Small Surge; Fixed in Production Silicon

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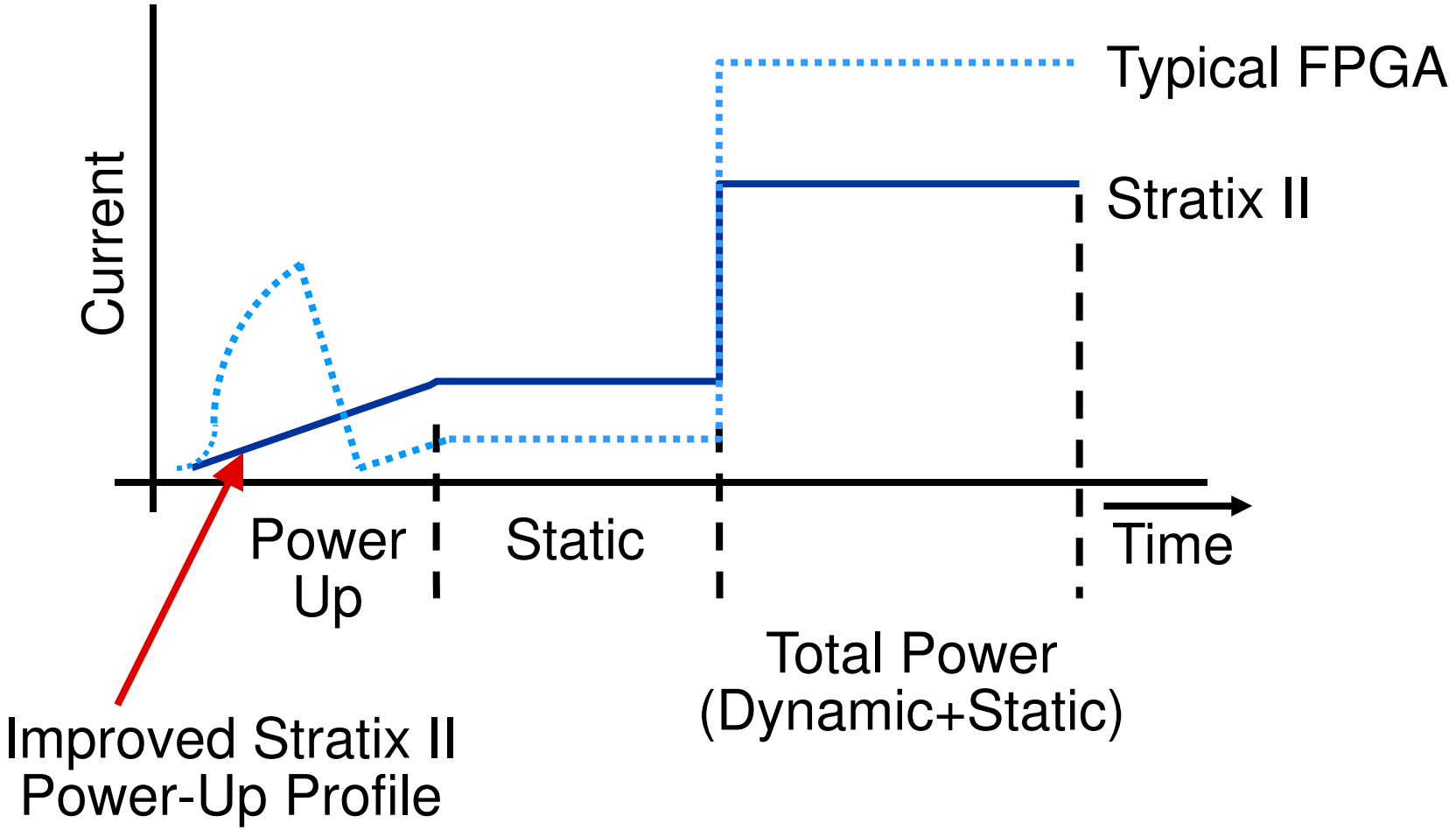
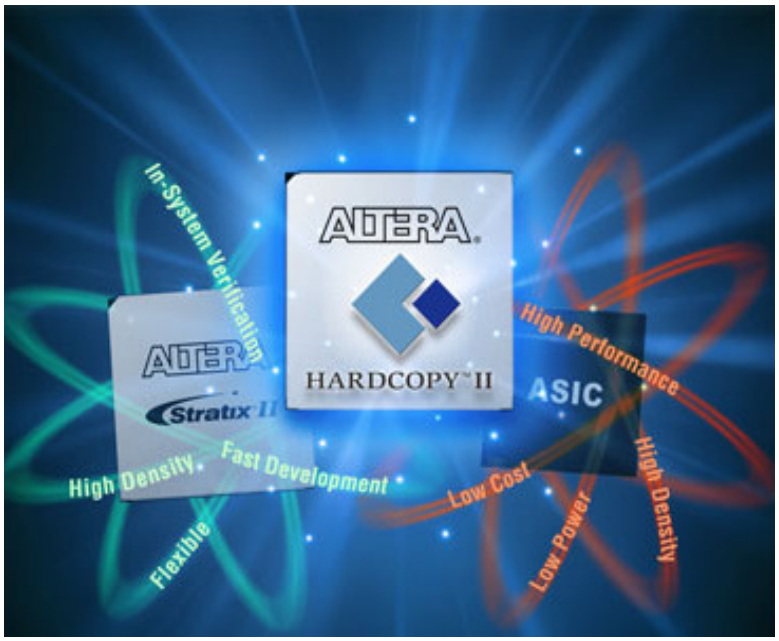
Power Up: No Surge!



HardCopy II Structured ASICs Migrate to the Lowest Power

HardCopy II Overview

- Lowest-Risk Structured ASIC
- Seamless Migration Path From Stratix II Design to HardCopy II
  - Same Design Software: Quartus II
  - Same IP Available
  - Functional Equivalence Guaranteed



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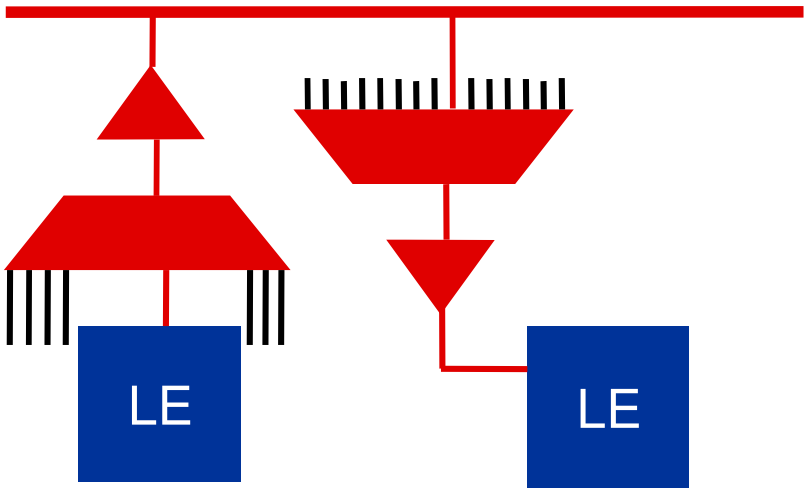
HardCopy II Routing Power

- FPGA Programmable Routing
  - Long Pre-Fabricated Wires
  - Pre-Fabricated Muxes & Buffers
  - → High Capacitance!
- HardCopy II: Custom Metal Routing
  - No Muxes
  - Only Exact Wires & Buffers Needed
- Logic Density Higher
  - Shorter Routes
- **20X Less Routing Capacitance!**



FPGA:
Programmable Routing

HardCopy II:
Custom Metal Routing

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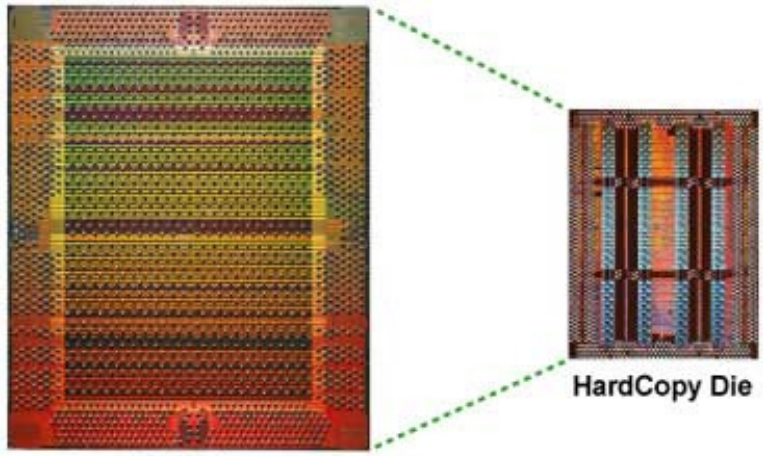
HardCopy II Leakage & Logic Power

- Far Fewer Transistors than an FPGA
  - → Lower Leakage



- FPGA Logic Cells
  - Internal Multiplexers Select Mode & Logic Function
- HardCopy II HCell Architecture
  - Simpler Gates; Use Metal Connections to Configure
  - 5 to 10X Less Logic Dynamic Power

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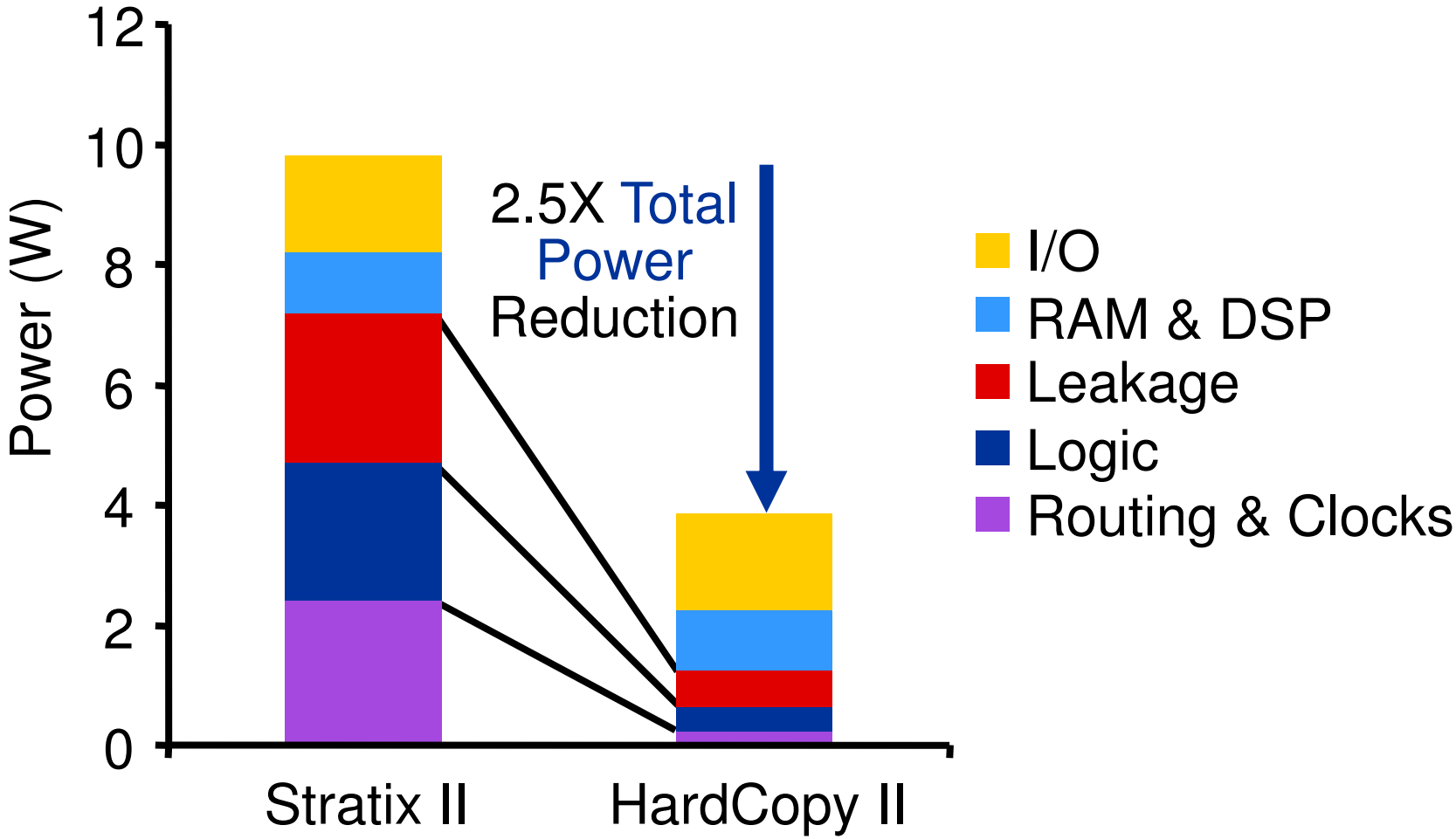
HardCopy II Power Advantage

- Example: High-Speed, High-Density Stratix II Design



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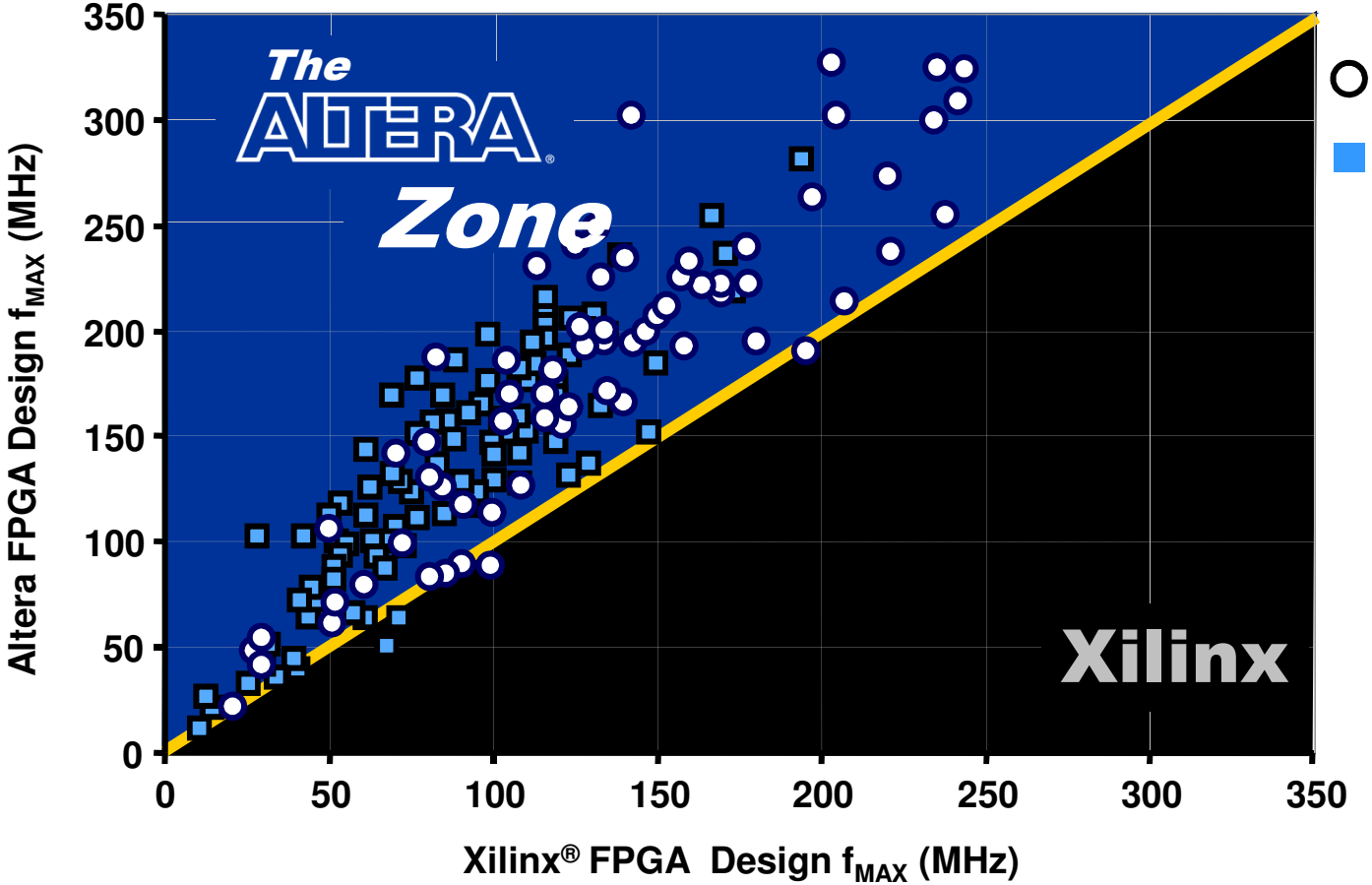
Performance & Summary

Great Performance While Managing Power

187 Designs Conclusively Validate Altera's Performance Advantage



- Stratix II vs. Virtex-4
- Cyclone/Cyclone II vs. Spartan-3

77 Designs Target Stratix II & Virtex-4; 110 Designs Target Cyclone/Cyclone II & Spartan-3 For details on methodology, see Altera's FPGA Performance Benchmarking Methodology White Paper

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Summary

- Total Device Power Is What Matters
  - 90-nm FPGAs Have Best Total Device Power
- Accurate Power Estimation
  - Requires Good Power Models
  - Sum Power of All Voltage Rails
  - Consider Worst-Case Silicon
- Stratix II
  - Best Performance at 90 nm
  - Total Device Power Better than Competition for High Speed Designs
- HardCopy II Reduces Power Even Further
  - Achieves Power Efficiency Beyond Any FPGA

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Resources & More Information

- Power Management Resource Center:
  http://www.altera.com/support/devices/power/pow-power.html
  - Stratix II Early Power Estimator v2.1 (Spreadsheet)
  - Power Basics
  - Certified Power Partner Solutions
  - AN 378: Stratix II Low Power Design Techniques (PDF)
  - AN 355: Stratix II Device Power Considerations (PDF)
  - AN 358: Thermal Management for 90nm FPGAs (PDF)
  - User Guide: PowerPlay Early Power Estimator (Coming Mid-05)
- Quartus II Handbook – PowerPlay Sections
  - Early Power Estimator (Vol. 3 Chapter 7)
  - Power Analyzer (Vol. 3 Chapter 8)
- Stratix II 90-nm Silicon Power Optimization
  http://www.altera.com/products/devices/stratix2/features/st2-power.html

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