Reduce FPGA Power With Automatic Optimization & Power-Efficient Design

Vaughn Betz & Sanjay Rajput
Previous Power Net Seminar…

Silicon vs. Software Comparison

Quartus® II PowerPlay: The Most Accurate Power Estimation Tool

(1) The Xilinx ISE XPower Tool Crashes

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Accurate Models Lead to Intelligent Decisions

- Intelligent decisions on power & thermal management
  - Accurate power models are critical

- For FPGA software to make intelligent power optimization decisions
  - Accurate power models are critical
Questions We’ll Answer Today

- How do I estimate my design’s power?
- How does power optimization work?
- How effective is Quartus II PowerPlay in reducing power?
- What are design techniques for reducing power?
- How can I ensure I’m using the best CAD settings for power?
Power Analysis
Overview

Getting the Best Accuracy
Accurate power estimates & analysis allow
- Time to optimize system
- FPGA CAD software to optimize design power
- Design decisions that reduce power
Early Power Estimator Accuracy

- Dynamic power accuracy limited by
  - Lack of place & route data
  - User entry: Resources, toggle rates, enable rates

+/-20% Error vs. Power Analyzer With Perfect User Data Entry

Stratix® II design

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Quartus II Power Analyzer

- More accurate than Early Power Estimator
  - Has precise resource counts
  - Has power models for each RAM/ALM/DSP mode
  - Considers exact routing used

- Best accuracy: Simulate for toggle rates

- Reduced accuracy: Vectorless analysis for toggle rates
Example: Power vs. RAM Mode

8700+ Designs Covering All FPGA Elements
Quartus II Automatic Power Optimization

Settings, Algorithms and Results
Power Optimization Overview

Timing-Driven Compiler

- **Timing Critical?**
  - Yes → **Min Delay**
  - No → **Min Area**

Power-Driven Compiler

- **Timing Critical?**
  - Yes → **Min Delay**
  - No → **Power Critical?**
    - Yes → **Min Power**
    - No → **Min Area**
PowerPlay Power Optimization

- Power-driven synthesis & fitting

- Normal effort (default)
  - Does not increase compile time
  - No reduction in design performance
  - No need for toggle rate data from simulation

- Extra effort
  - Larger power reduction
  - May increase compile time
  - All timing optimization enabled, but performance loss possible
  - Best with toggle rate data from simulation
PowerPlay Power Optimization

- Automatic, but less accurate
- Requires testbench, more accurate
  - Vectorless Estimation
  - RTL Simulation

Power-Driven Synthesis
- Normal or Extra effort

Power-Driven Fit

Evaluate Power
- Gate-Level Simulation + Power Analyzer
- Hardware Measurement

Power Report

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Three Components of Power

- Core Dynamic: 67%
- Core Static: 22%
- I/O: 11%

99 Customer Designs, Stratix II Devices

Dynamic Power Dominant
Focus of Power Optimization
Core Dynamic Power

99 Customer Designs, Stratix II Devices

Routing 38%

RAM Blocks 14%

ALM Combinational 19%

ALM Registers 18%

DSP Blocks 2%*

Clock Networks 9%

*Digital Signal Processing (DSP) Block power: 5% of Dynamic power for designs that use DSP blocks

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Power-Optimal RAM Mapping

- Power inefficient to use large physical RAM for small memory or vice versa
- Tri-matrix memory gives 3 physical RAM sizes
- Quartus II automatically picks best physical RAM
RAM Enable Optimization

- Shut RAM down when unused → less power
  - Convert read/write enable to clock enable
Power-Optimized RAM Mapping

Default Option

1K X 16 RAM

Power Efficient Option

2:4 Decoder

4 1Kx4 M4K RAMs

4 256x16 M4K RAMs
RAM Power Reduction (Stratix II)

- Normal effort: 6% average savings
- Extra effort: 21% average savings

Design

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Power-Driven Place & Route

- Minimize capacitance of high-toggling signals
- Without violating timing constraints

20 Million Toggle/s 100 Million Toggle/s

Power Optimize
Clock Shut Down Hardware

- Stratix II: Can shut down clock at 3 levels of tree
  - Top-level: Shut down 1/8 of clock tree
  - Next-level: 1/500 of clock tree
  - Bottom-level: 1/5000 of clock tree
Placement to Reduce Clock Power

Clocking Legal, Timing Optimized

Power Optimize

Group Clocks for Maximum Shutdown

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Experimental Flow

Source HDL

33 Designs:
Customer & Internal Altera

Quartus II 5.1
Synthesis & Fitting
with PowerPlay

Quartus II 5.0 SP1
Synthesis & Fitting

Compare Dynamic Power
I don't see any results. Is it slide 25 and 26?

Amy Lee, 02/12/2005
Stratix II Results: Normal Effort

Dynamic Power Reduction vs. Quartus 5.0

- Logic Intensive
- DSP Intensive
- RAM Intensive
- Balanced
Stratix II Results: Extra Effort

Dynamic Power Reduction vs. Quartus 5.0

- Logic Intensive
- DSP Intensive
- RAM Intensive
- Balanced
## Stratix II Results Summary

<table>
<thead>
<tr>
<th>Power Optimization Flow</th>
<th>Dynamic Power vs. QII 5.0</th>
<th>$F_{\text{max}}$ Change</th>
<th>Compile Time Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Effort: Normal</td>
<td>-15%</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Effort: Extra</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Toggle rates: Simulation</td>
<td>-21%</td>
<td>-2%</td>
<td>+9%</td>
</tr>
<tr>
<td>Effort: Extra</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Toggle rates: Vectorless</td>
<td>-18%</td>
<td>-2%</td>
<td>+9%</td>
</tr>
<tr>
<td>Effort: Extra</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Toggle rates: Simulation</td>
<td>-25%</td>
<td>--</td>
<td>+100%</td>
</tr>
<tr>
<td>Easy timing constraint</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Designing for Lower Power

Six Tips for Reducing Core Power
1. Use Hard IP Blocks

- Synthesis tool inferring all the hard blocks it should?
  - Check with floor-plan editor or HDL viewer

- DSP Blocks
  - Less power than logic elements except for small multiplies (e.g. 5x5)
  - Use all the DSP logic (not just multipliers):
    - Multiplier-accumulator, complex-multiplier, finite impulse response sample chaining, etc.
  - Use altmultAccum MegaFunction if synthesis not inferring
1. Use Hard IP Blocks (Cont.)

- RAM blocks
  - Usually inferred by synthesis
  - Use `altsyncram` MegaFunction if necessary

- Shift registers
  - Many toggling signals: Power inefficient
  - Medium to large shift registers: Implement in FIFOs
  - Use `altshift_taps` MegaFunction if necessary
2. Synthesize for Area

- Less logic usually means less power
  - Fewer signals to toggle
  - If sufficient timing margin, tell synthesis tool to optimize for area
3. Help Shut Down RAM Blocks

- Specify read-enable & write-enable signals on your RAMs whenever possible
  - PowerPlay will convert to clock enables
  - Completely shuts down RAM on many cycles

- Leave RAM Block Type = Auto
  - Power optimizer will choose best RAM block
4. Use Clock Enables on Logic

- When clock enable is low
  1. Register + downstream logic don’t toggle
  2. Clock inside a logic array block (LAB) is shut off

- Even when clock enable is not needed for functionality, it can save power
5. Minimize Glitching

- Some logic produces many transitions/cycle
  - For example, CRC/parity, combinational multipliers
  - Find “Glitchy” logic via power analyzer report
  - Register inputs & outputs of “Glitchy” logic
  - Insert pipeline registers if possible
6. Shut Down Idle Clocks

- Entire clock domain unused in some cycles
  - Use the `altclkctrl` MegaFunction to safely gate the clock
  - Shuts down entire clock tree → lower power than a clock enable on all registers
Power Optimization Advisor & Design Space Explorer

“Youre FAEs in Quartus”
Power Optimization Advisor

- Explains power analysis best practices
- Power optimization suggestions
  - In priority order
- Highlights recommended settings not enabled on your design
- Button to correct settings
- Located in Tools Menu
### Power Optimization Advisor

#### Power-Driven Synthesis

<table>
<thead>
<tr>
<th>Recommendation</th>
<th>Set PowerPlay Power Optimization during synthesis to Extra Effort.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>Extra effort power-driven synthesis will choose logic and RAM implementations which minimize design dynamic power.</td>
</tr>
<tr>
<td>Summary</td>
<td>The following areas will be affected by the recommended changes:</td>
</tr>
<tr>
<td></td>
<td>- Delay may increase (fmax may decrease)</td>
</tr>
<tr>
<td></td>
<td>- Logic element usage may increase</td>
</tr>
<tr>
<td></td>
<td>= Compilation time is unaffected</td>
</tr>
<tr>
<td>Action</td>
<td>Set PowerPlay Power Optimization during synthesis to Extra Effort</td>
</tr>
<tr>
<td></td>
<td>Current Global Settings:</td>
</tr>
<tr>
<td></td>
<td>PowerPlay Power Optimization = NORMAL</td>
</tr>
<tr>
<td></td>
<td>Compilation (Recommended: EXTRA EFFORT)</td>
</tr>
</tbody>
</table>

**Correct the Settings**

Open Settings dialog box - Analysis & Synthesis
Design Space Explorer

- Searches Quartus options to find best implementation
  - “Search for Lowest Power”
  - Finds settings that minimize power & meet timing
  - `quartus_sh --dse`
  or Tools Menu
Summary & Wrap Up
Altera’s PowerPlay Suite

- Most accurate power analysis tools
- Automatic power optimization
  - Industry first
  - Highly effective
  - 20% to 25% dynamic power reduction on average
- Power Optimization Advisor guides you to lower power

Better Tools:
Lower Power & No Surprises
Stratix II vs. Virtex-4 Power

Dynamic Power: Stratix II vs. Virtex-4

Logic intensive
DSP intensive
RAM intensive
Balanced

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Power & Altera Hardware

- **Stratix II**
  - Lowest dynamic power & lowest total power for 90nm high-density FPGAs

- **Cyclone™ II**
  - Lowest power of any FPGA

- **HardCopy® II**
  - Smooth migration to lower power
  - Typical: 2X to 3X reduction vs. FPGA
Resources & More Information

- Quartus II Handbook Volume 2, Chapter 9. - Power Optimization
  www.altera.com/quartus2

- Stratix II power page
  www.altera.com/stratix2power

- Cyclone II power page
  www.altera.com/cyclone2power

- Power management resource center
  www.altera.com/power
Thank You

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