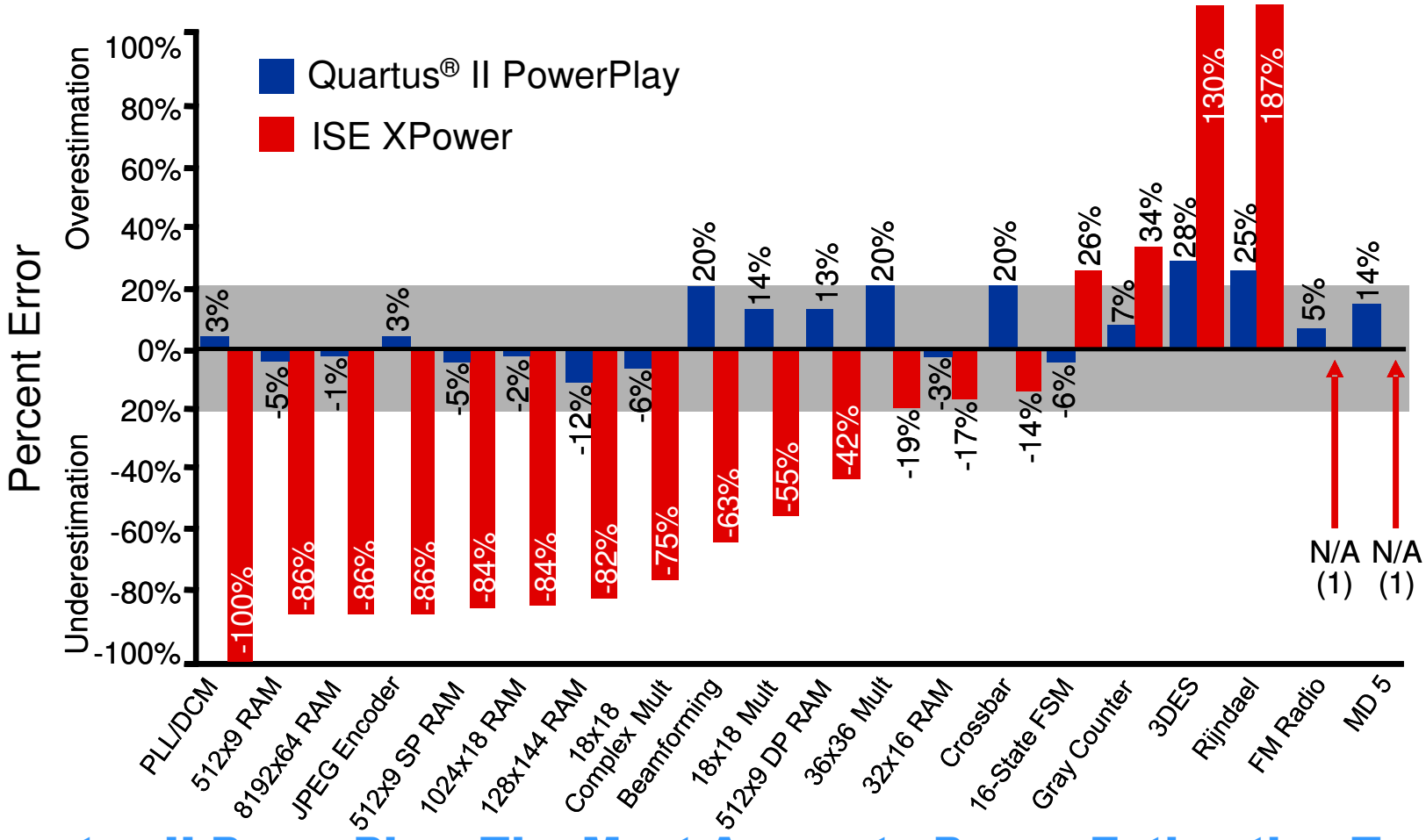
Reduce FPGA Power With Automatic Optimization & Power-Efficient Design

Vaughn Betz & Sanjay Rajput

Previous Power Net Seminar…

Silicon vs. Software Comparison



Quartus II PowerPlay: The Most Accurate Power Estimation Tool

(1) The Xilinx ISE XPower Tool Crashes

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Accurate Models Lead to Intelligent Decisions

- Intelligent decisions on power & thermal management
  - Accurate power models are critical
- For FPGA software to make intelligent power optimization decisions
  - Accurate power models are critical

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Questions We'll Answer Today

- How do I estimate my design's power?
- How does power optimization work?
- How effective is Quartus II PowerPlay in reducing power?
- What are design techniques for reducing power?
- How can I ensure I'm using the best CAD settings for power?

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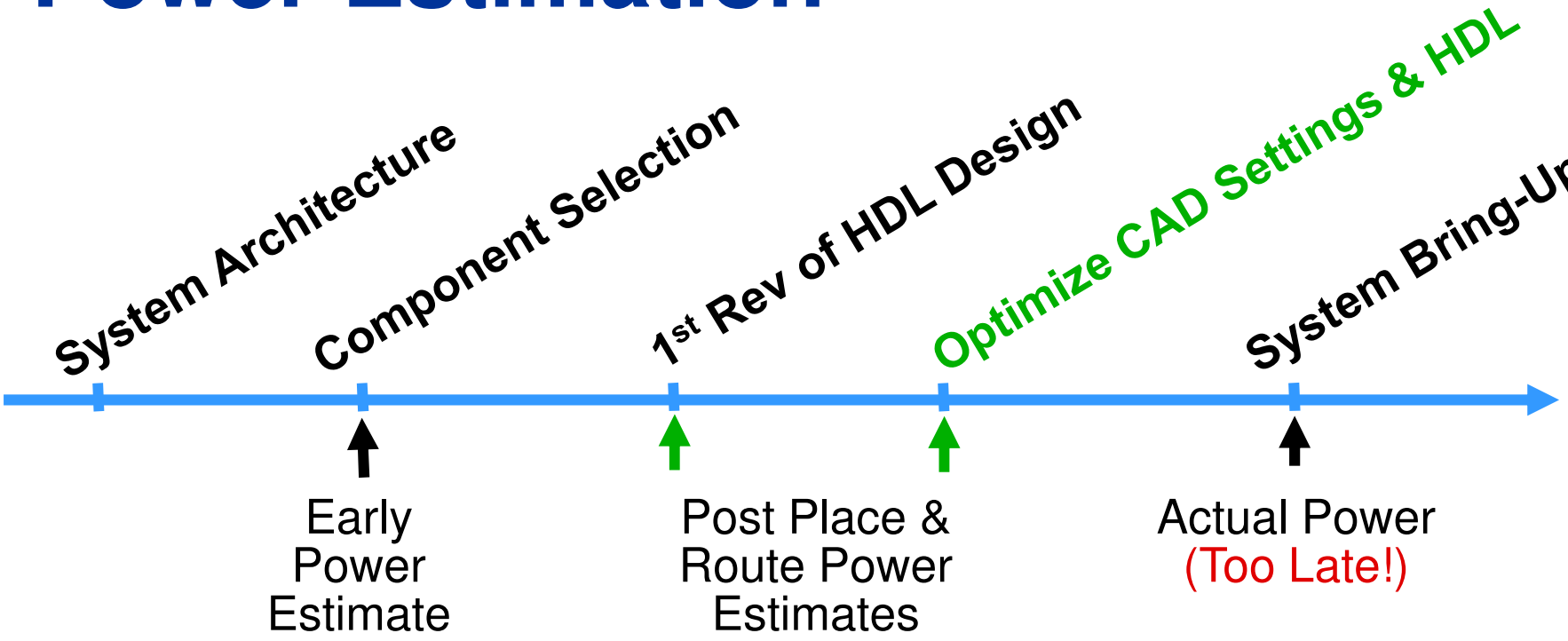
Power Analysis Overview

Getting the Best Accuracy

Power Estimation



- Accurate power estimates & analysis allow
  - Time to optimize system
  - FPGA CAD software to optimize design power
  - Design decisions that reduce power

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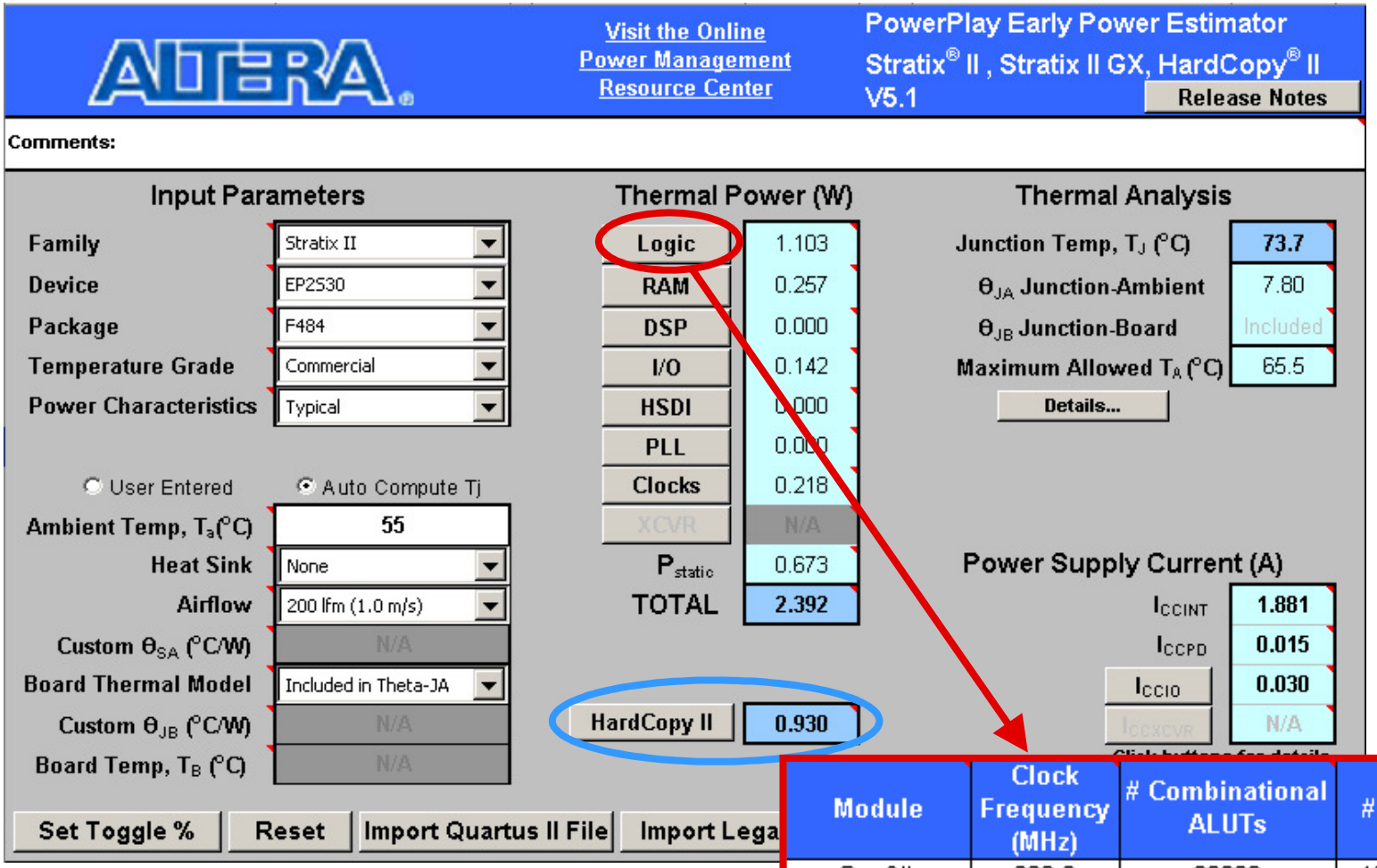
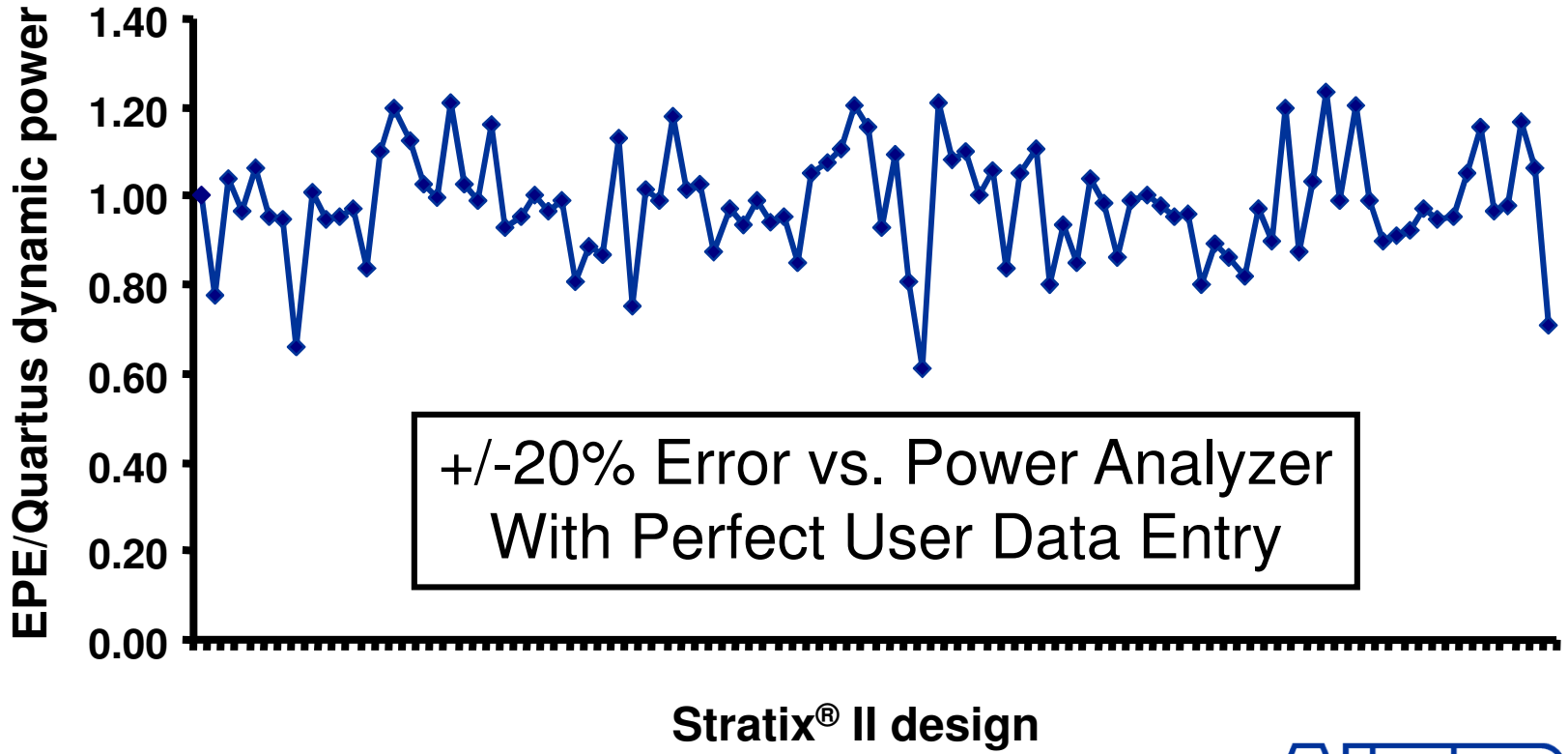
Early Power Estimator



Module	Clock Frequency (MHz)	# Combinational ALUTs	# FFs	Toggle %
SysClk	200.0	20000	12000	12.5%
IngressClk	400.0	300	400	25.0%
EgressClk	200.0	400	200	25.0%

Early Power Estimator Accuracy

- Dynamic power accuracy limited by
  - Lack of place & route data
  - User entry: Resources, toggle rates, enable rates



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Quartus II Power Analyzer

- More accurate than Early Power Estimator
  - Has precise resource counts
  - Has power models for each RAM/ALM/DSP mode
  - Considers exact routing used
- Best accuracy: Simulate for toggle rates
- Reduced accuracy: Vectorless analysis for toggle rates

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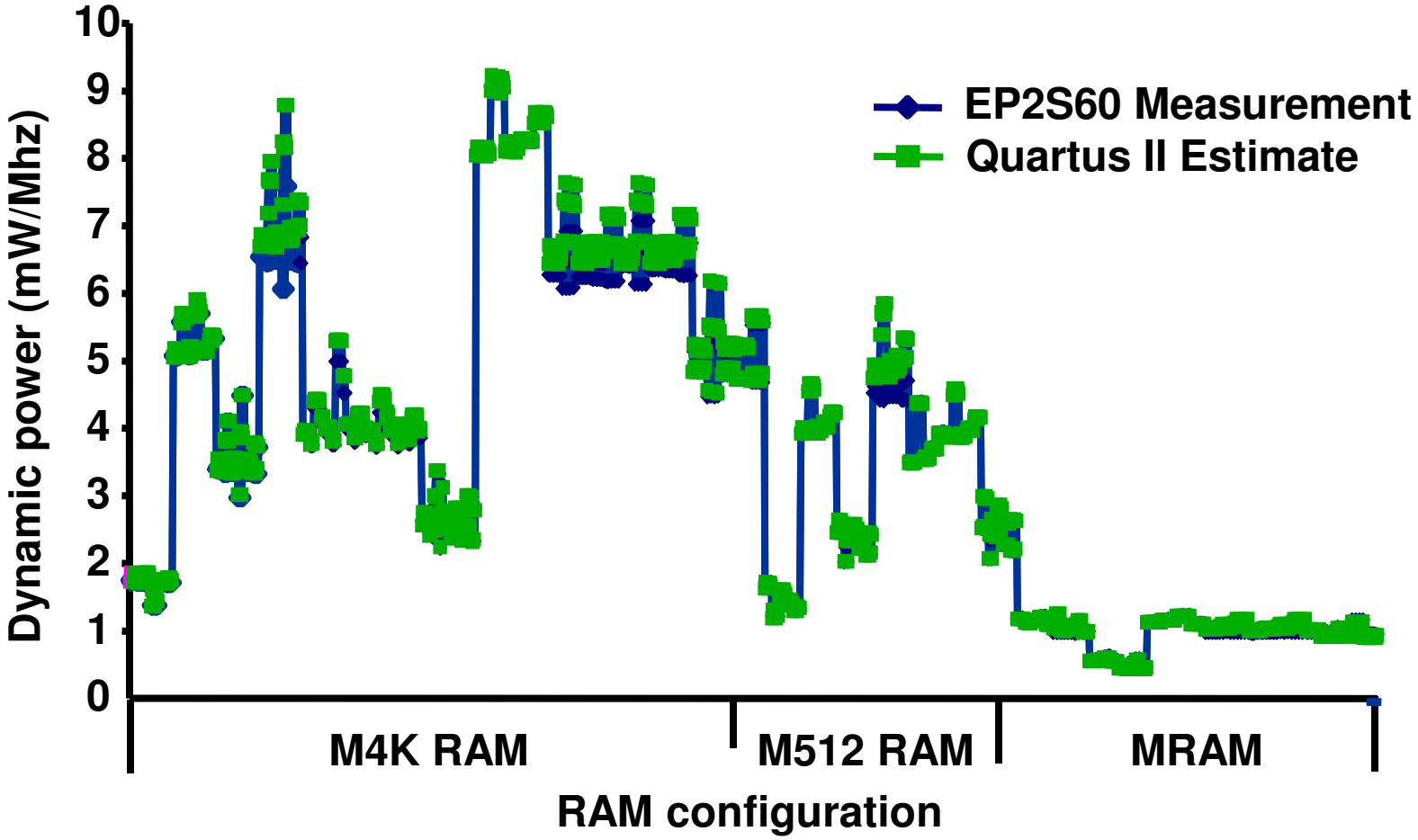
Example: Power vs. RAM Mode



8700+ Designs Covering All FPGA Elements

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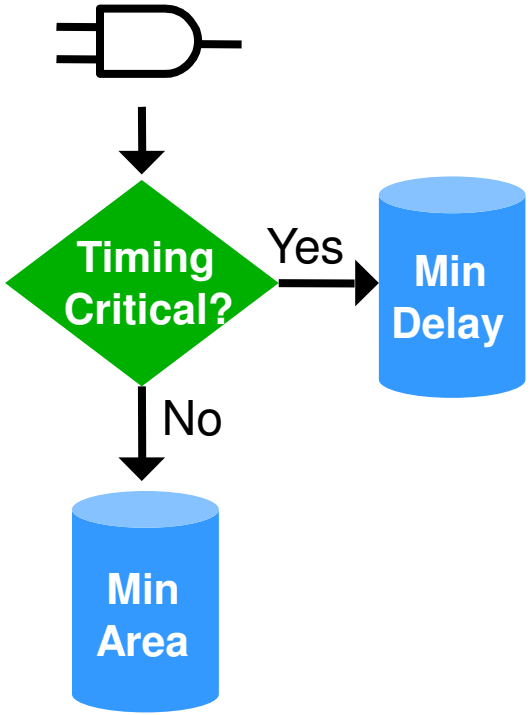
Quartus II Automatic Power Optimization

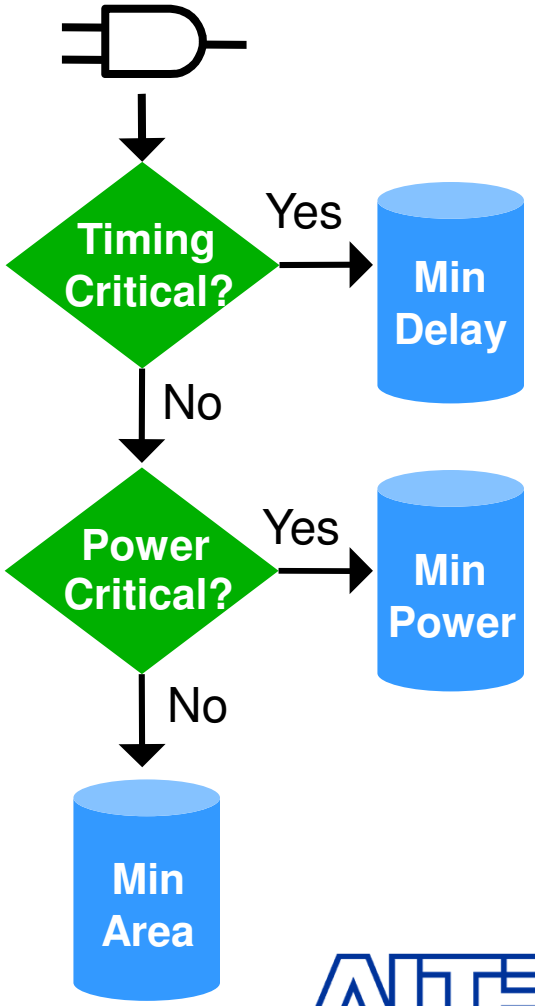
Settings, Algorithms and Results

Power Optimization Overview

Timing-Driven Compiler



Power-Driven Compiler



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PowerPlay Power Optimization

- Power-driven synthesis & fitting
- Normal effort (default)
  - Does not increase compile time
  - No reduction in design performance
  - No need for toggle rate data from simulation
- Extra effort
  - Larger power reduction
  - May increase compile time
  - All timing optimization enabled, but performance loss possible
  - Best with toggle rate data from simulation

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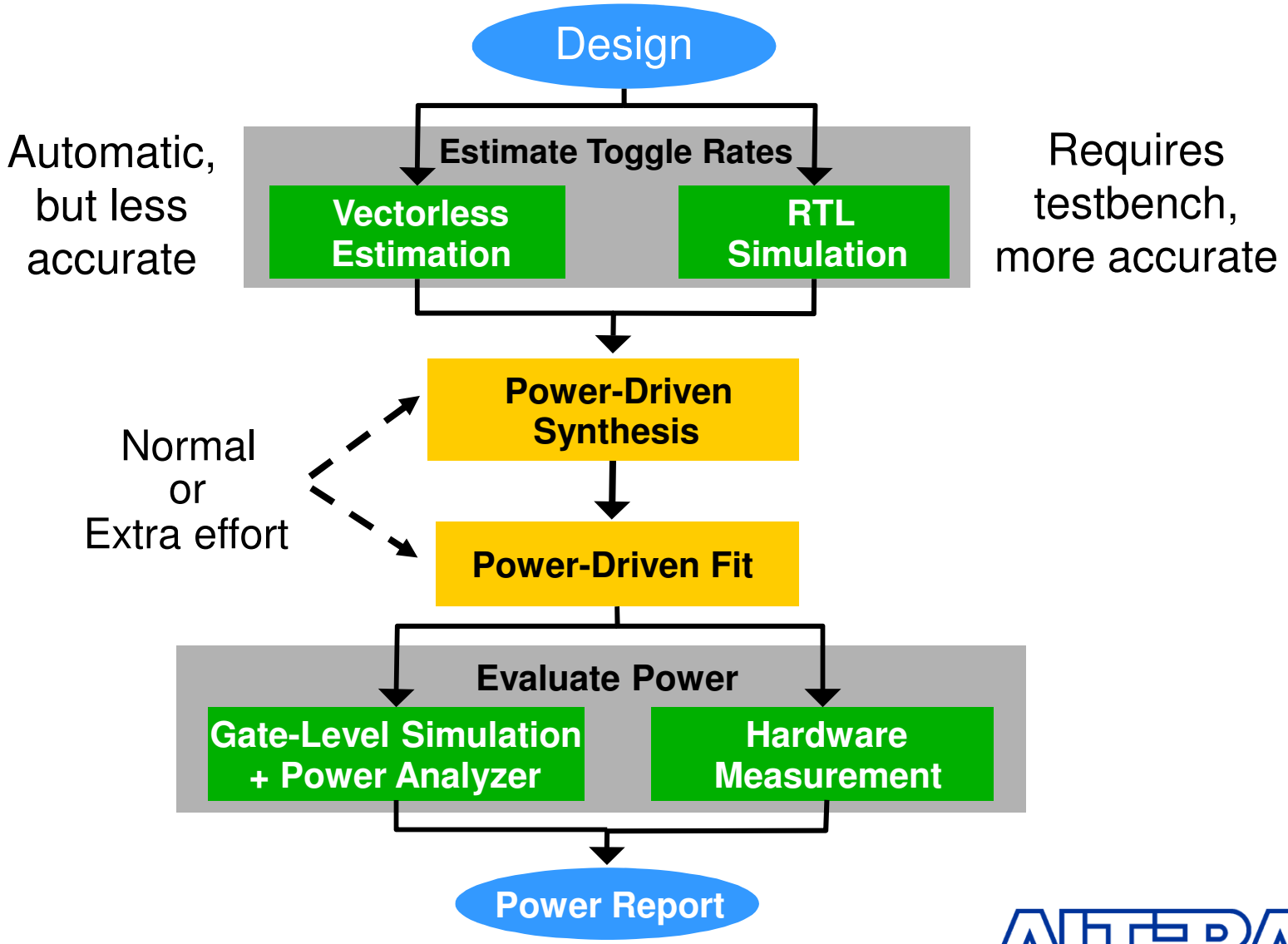
PowerPlay Power Optimization



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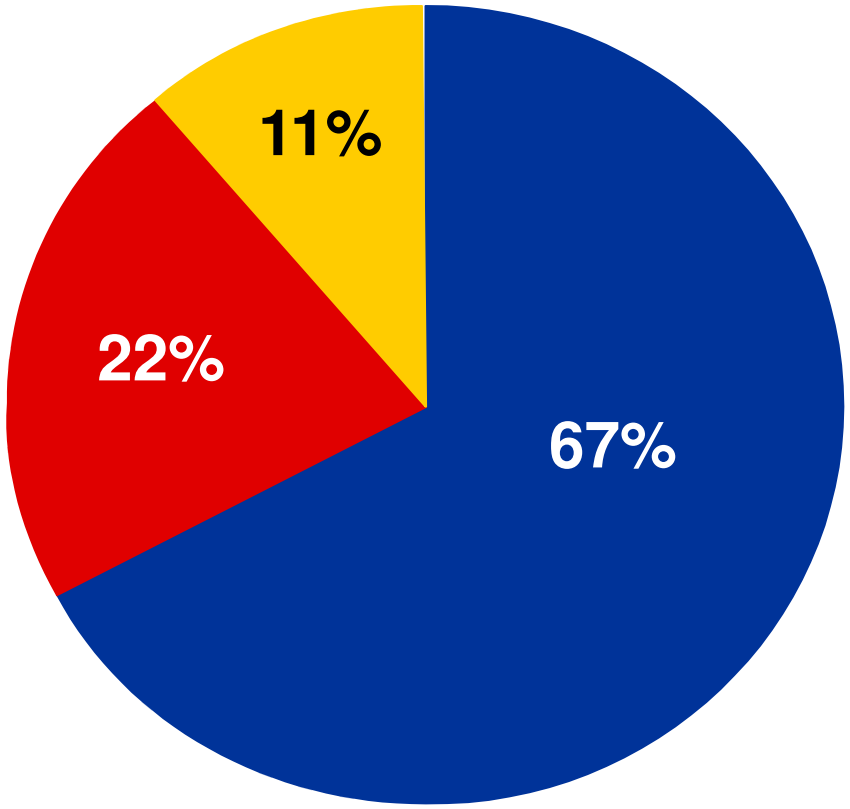
Three Components of Power



99 Customer Designs, Stratix II Devices

- Core Dynamic
- Core Static
- I/O

Dynamic Power Dominant Focus of Power Optimization

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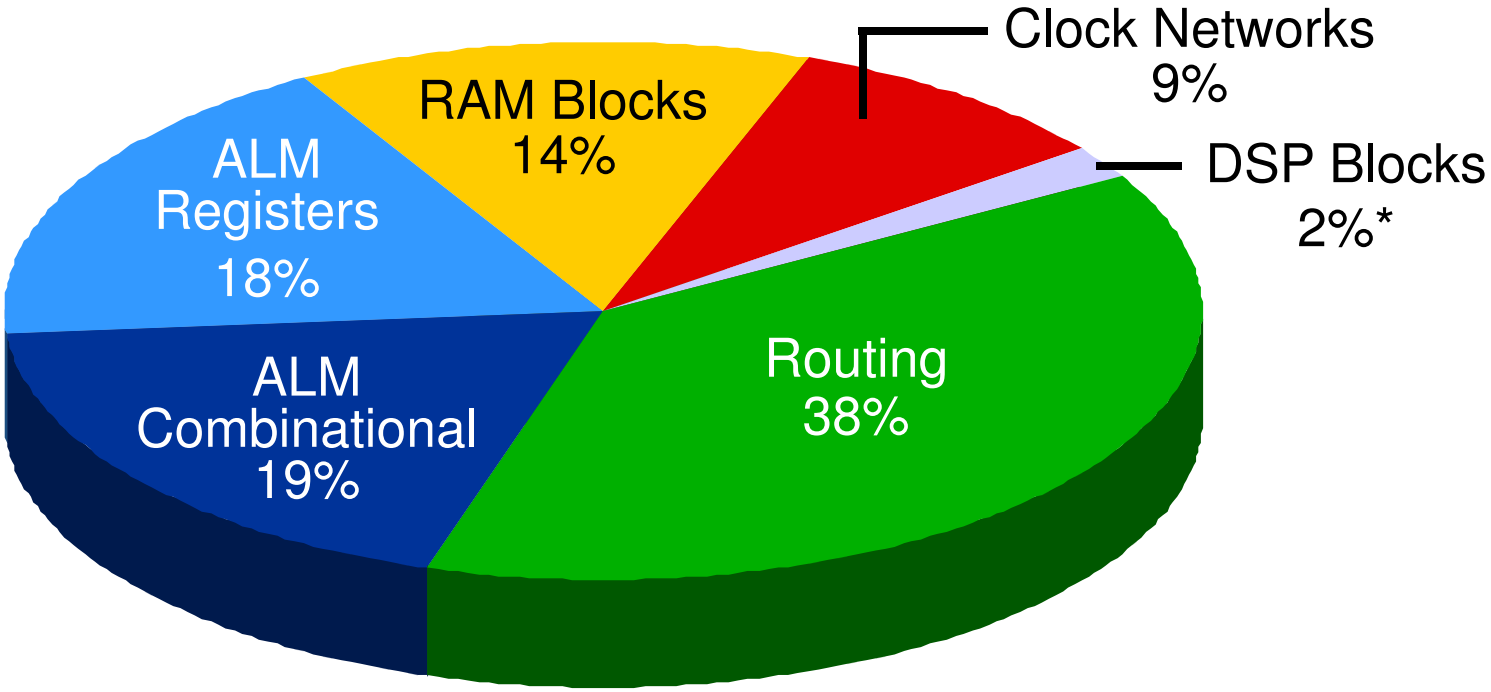
Core Dynamic Power

99 Customer Designs, Stratix II Devices



***Digital Signal Processing (DSP) Block power:**
5% of Dynamic power for designs that use DSP blocks

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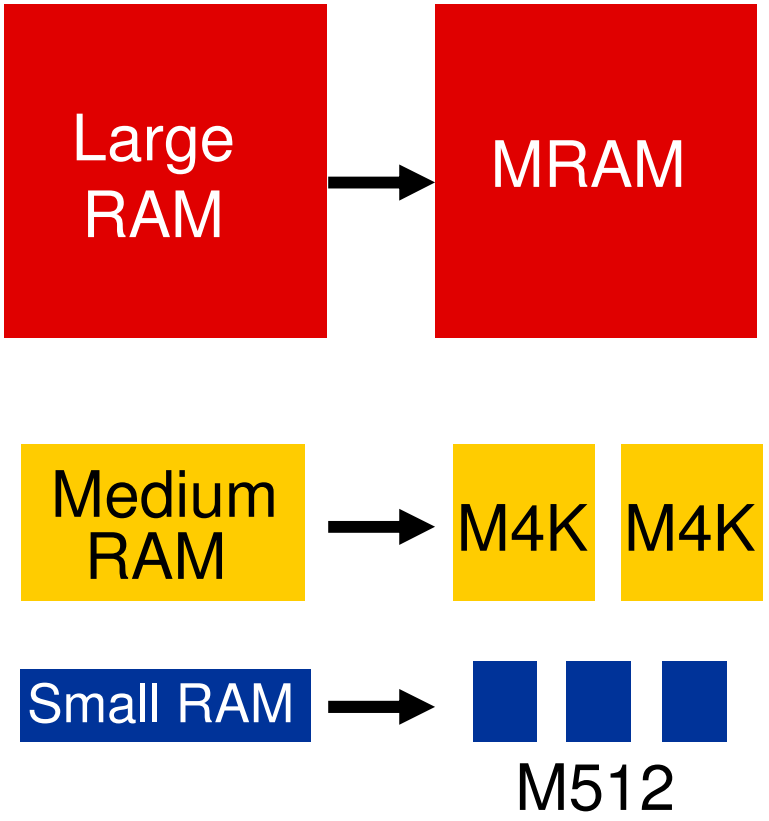
Power-Optimal RAM Mapping

- Power inefficient to use large physical RAM for small memory or vice versa
- Tri-matrix memory gives 3 physical RAM sizes
- Quartus II automatically picks best physical RAM



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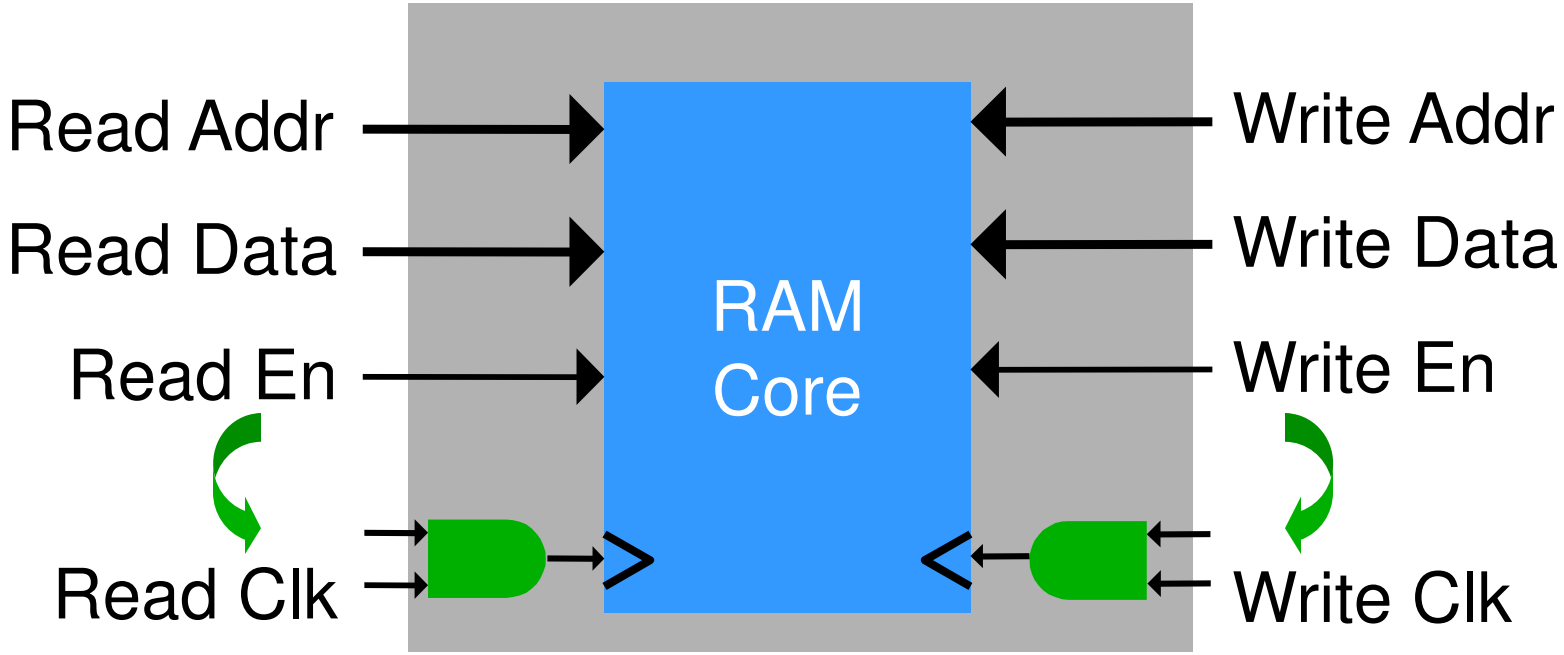
RAM Enable Optimization

- Shut RAM down when unused → less power
  - Convert read/write enable to clock enable



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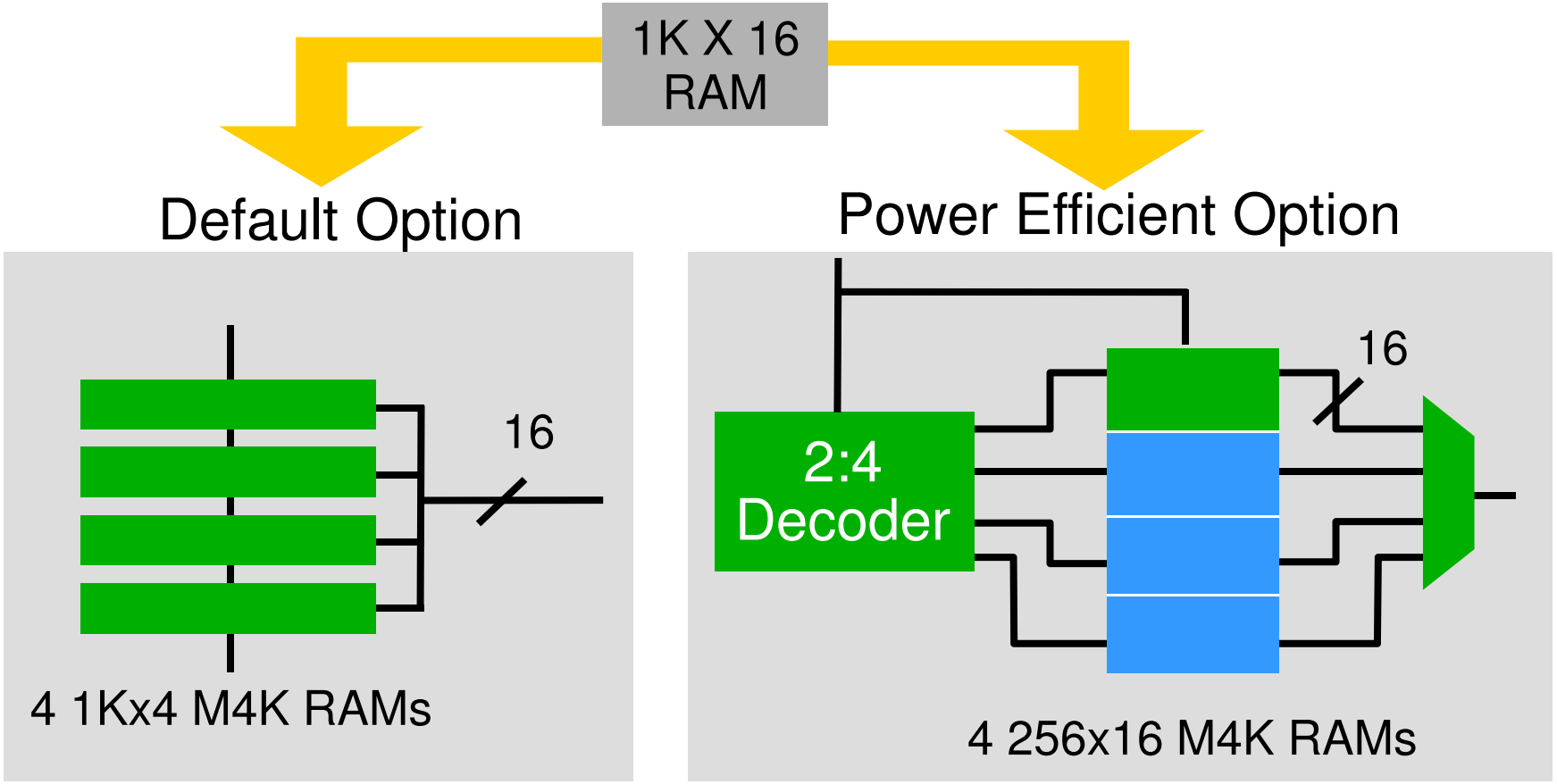
Power-Optimized RAM Mapping



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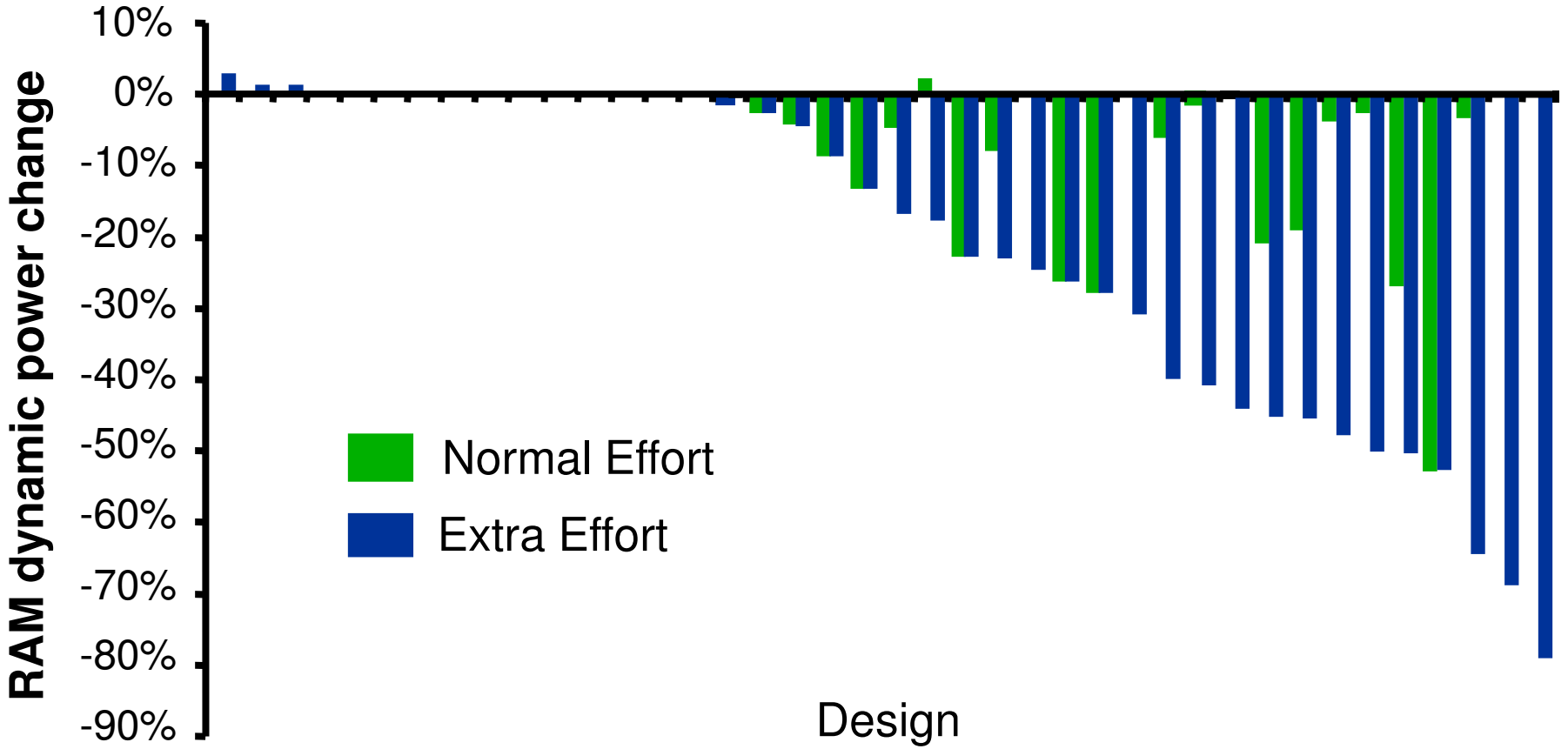
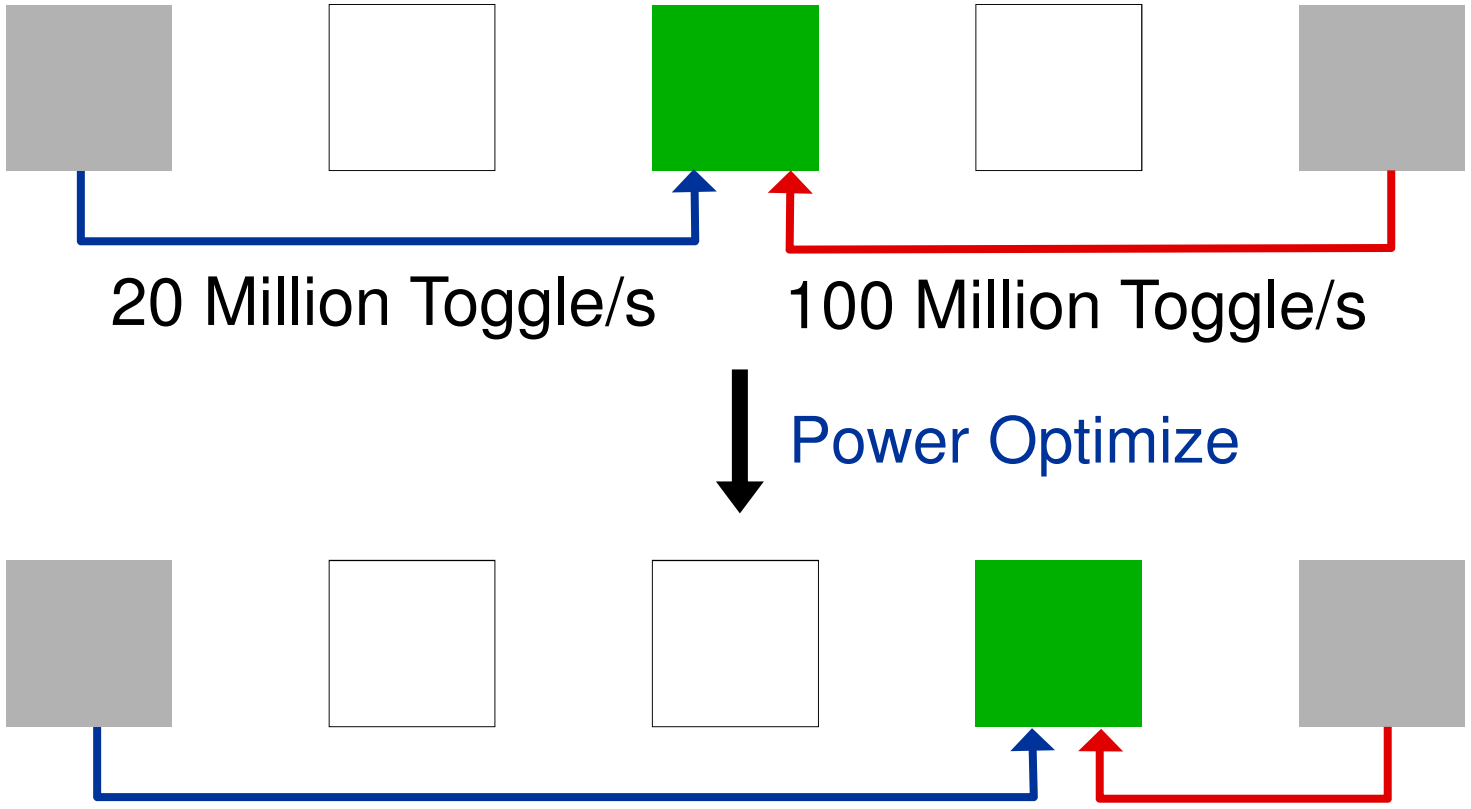
RAM Power Reduction (Stratix II)

- Normal effort: 6% average savings
- Extra effort: 21% average savings



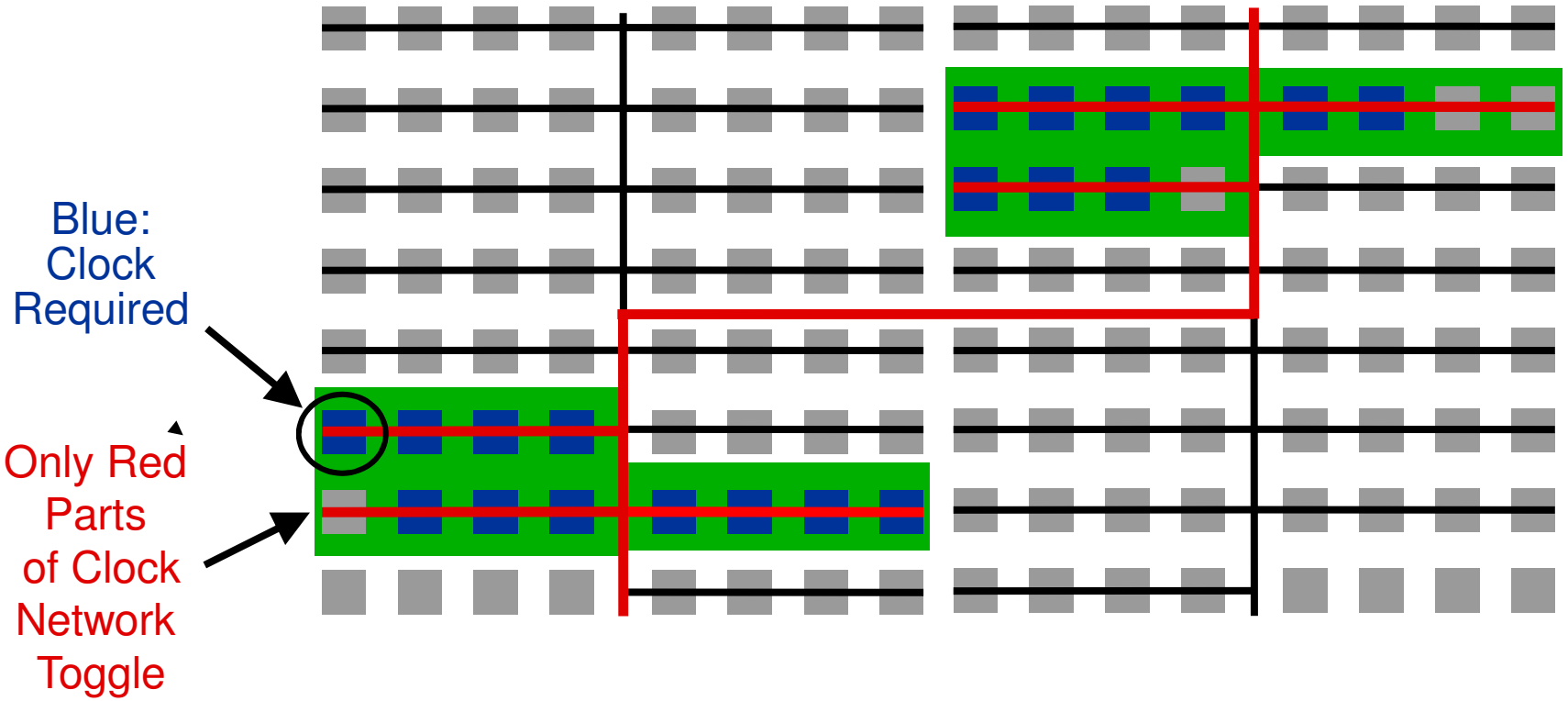
Power-Driven Place & Route

- Minimize capacitance of high-toggling signals
- Without violating timing constraints



Clock Shut Down Hardware

- Stratix II: Can shut down clock at 3 levels of tree
  - Top-level: Shut down 1/8 of clock tree
  - Next-level: 1/500 of clock tree
  - Bottom-level: 1/5000 of clock tree



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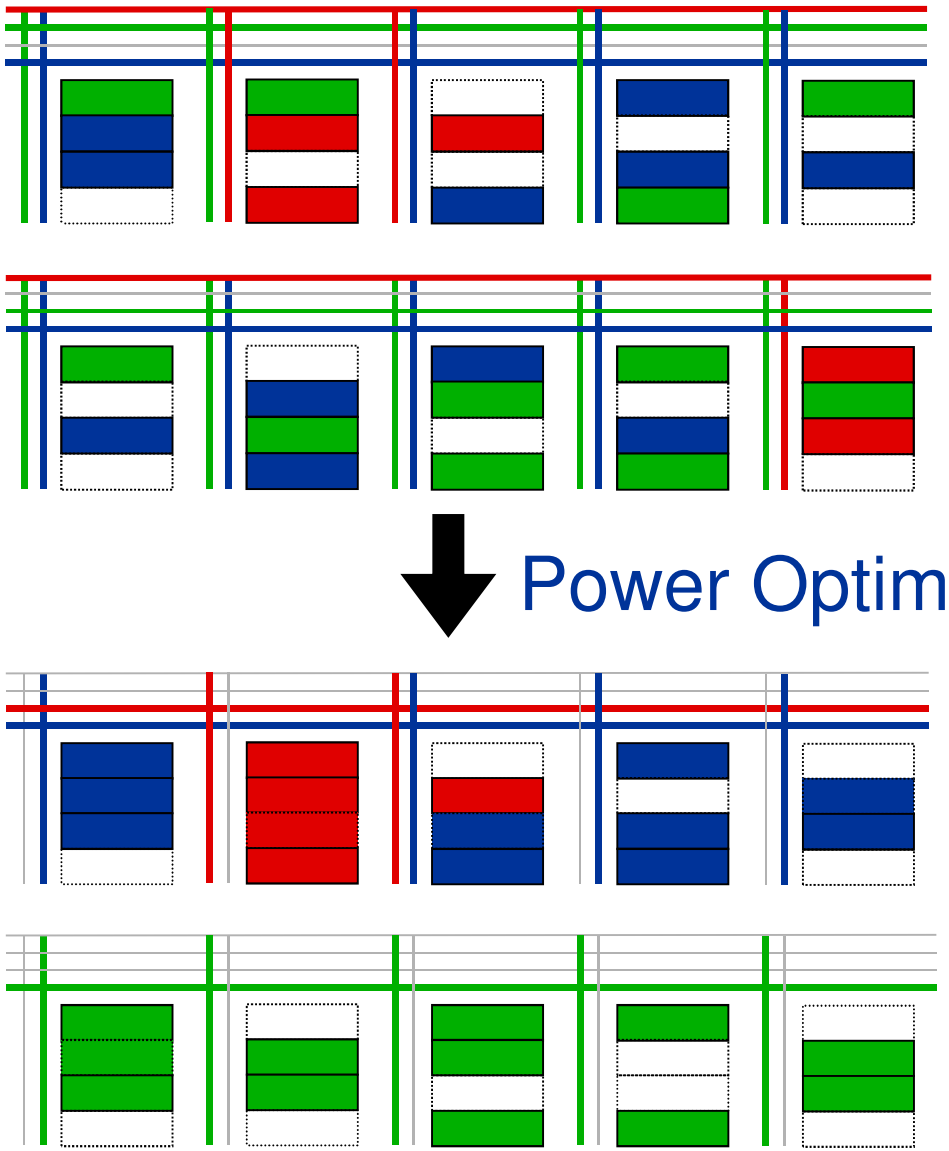
Placement to Reduce Clock Power



Clocking Legal,
Timing Optimized

Group Clocks for
Maximum Shutdown

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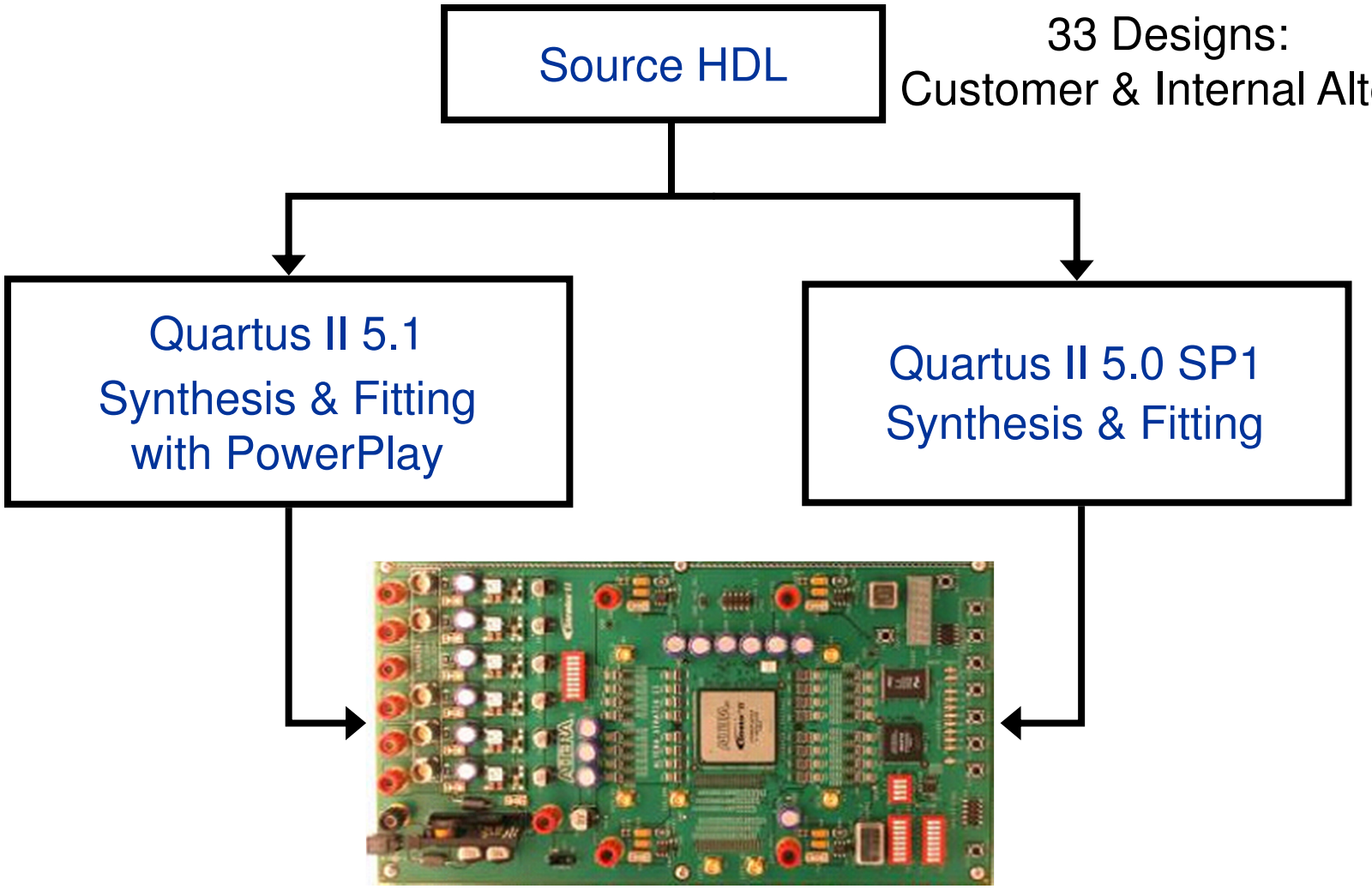
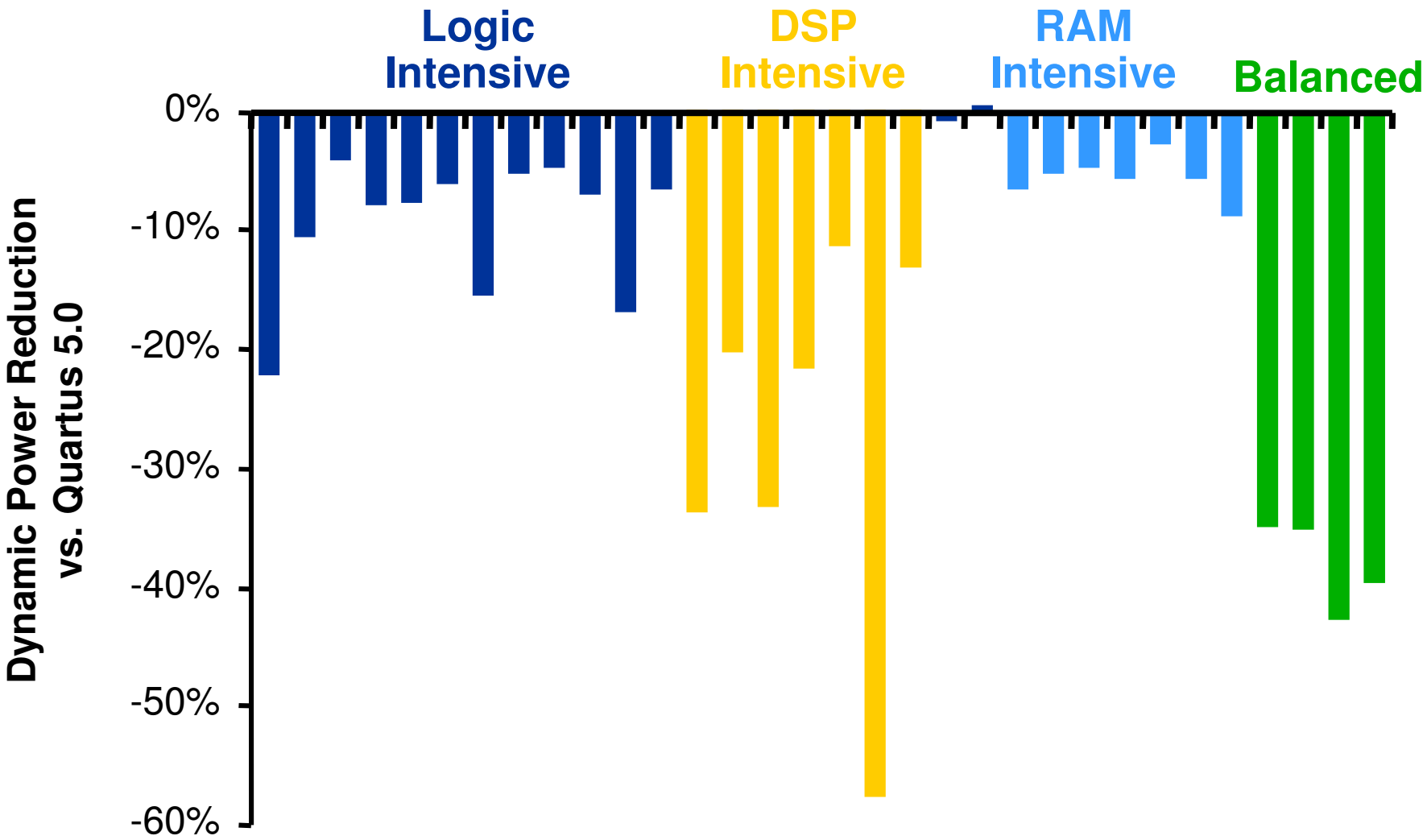
Experimental Flow



Slide 24

AL14 I don't see any results. Is it slide 25 and 26?
Amy Lee, 02/12/2005

Stratix II Results: Normal Effort



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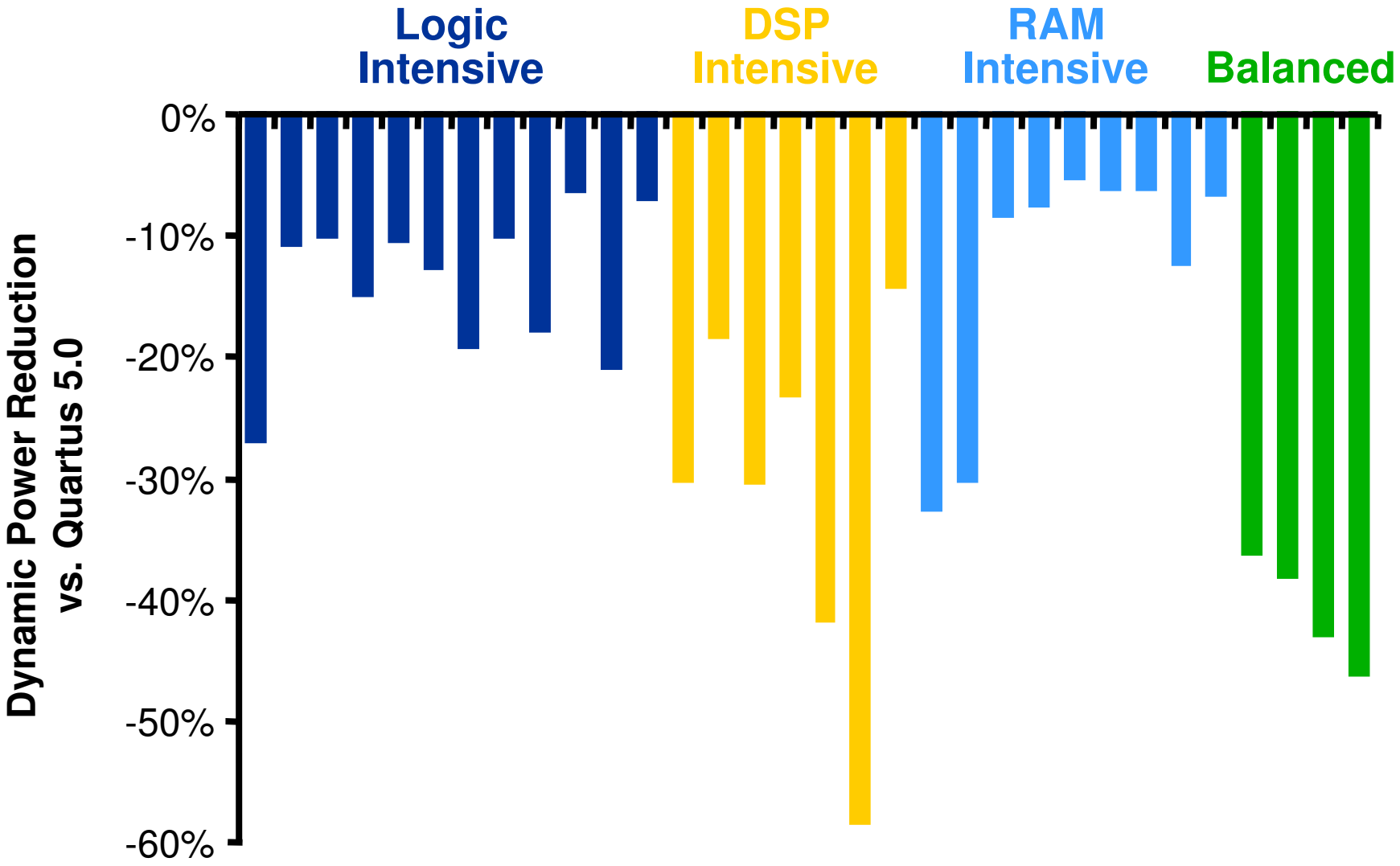
Stratix II Results: Extra Effort



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Stratix II Results Summary

Power Optimization Flow	Dynamic Power vs. QII 5.0	F_{max} Change	Compile Time Change
Effort: Normal	-15%	--	--
Effort: Extra Toggle rates: Simulation	-21%	-2%	+9%
Effort: Extra Toggle rates: Vectorless	-18%	-2%	+9%
Effort: Extra Toggle rates: Simulation Easy timing constraint	-25%	--	+100%

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Designing for Lower Power

Six Tips for Reducing Core Power

1. Use Hard IP Blocks

- Synthesis tool inferring all the hard blocks it should?
  - Check with floor-plan editor or HDL viewer

- DSP Blocks
  - Less power than logic elements except for small multiplies (e.g. 5x5)
  - Use all the DSP logic (not just multipliers):
    - Multiplier-accumulator, complex-multiplier, finite impulse response sample chaining, etc.
  - Use **altmult_accum** MegaFunction if synthesis not inferring

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1. Use Hard IP Blocks (Cont.)

- RAM blocks
  - Usually inferred by synthesis
  - Use **altsyncram** MegaFunction if necessary
- Shift registers
  - Many toggling signals: Power inefficient
  - Medium to large shift registers: Implement in FIFOs
  - Use **altshift_taps** MegaFunction if necessary

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2. Synthesize for Area

- Less logic usually means less power
  - Fewer signals to toggle
  - If sufficient timing margin, tell synthesis tool to optimize for area

3. Help Shut Down RAM Blocks

- Specify read-enable & write-enable signals on your RAMs whenever possible
  - PowerPlay will convert to clock enables
  - Completely shuts down RAM on many cycles
- Leave RAM Block Type = Auto
  - Power optimizer will choose best RAM block

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4. Use Clock Enables on Logic

- When clock enable is low
  1. Register + downstream logic don't toggle
  2. Clock inside a logic array block (LAB) is shut off
- Even when clock enable is not needed for functionality, it can save power

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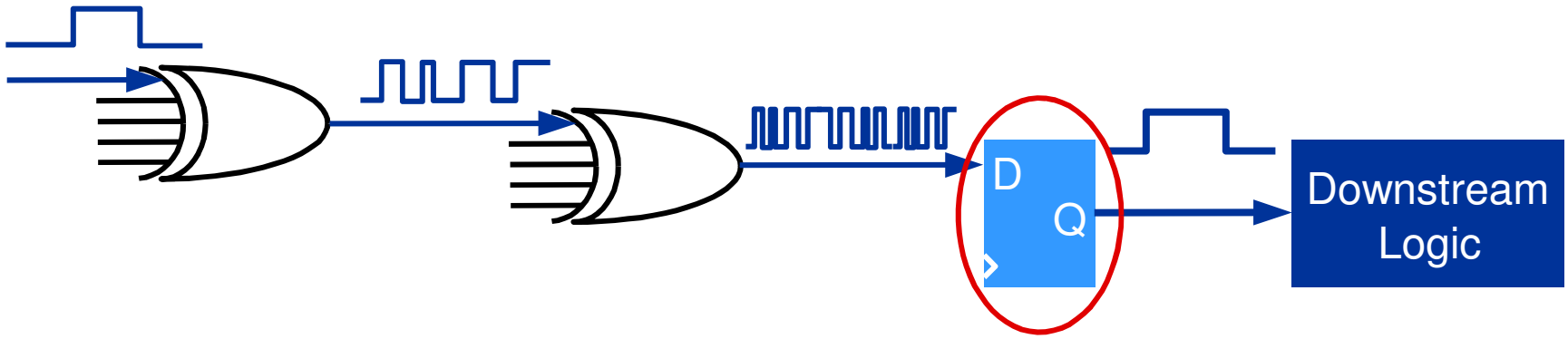
5. Minimize Glitching

- Some logic produces many transitions/cycle
  - For example, CRC/parity, combinational multipliers
  - Find “Glitchy” logic via power analyzer report
  - Register inputs & outputs of “Glitchy” logic
  - Insert pipeline registers if possible



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6. Shut Down Idle Clocks

- Entire clock domain unused in some cycles
  - Use the **altclkctrl** MegaFunction to safely gate the clock
  - Shuts down entire clock tree → lower power than a clock enable on all registers

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Power Optimization Advisor & Design Space Explorer

"Your FAEs in Quartus"

Power Optimization Advisor

- Explains power analysis best practices
- Power optimization suggestions
  - In priority order
- Highlights recommended settings not enabled on your design
- Button to correct settings
- Located in Tools Menu

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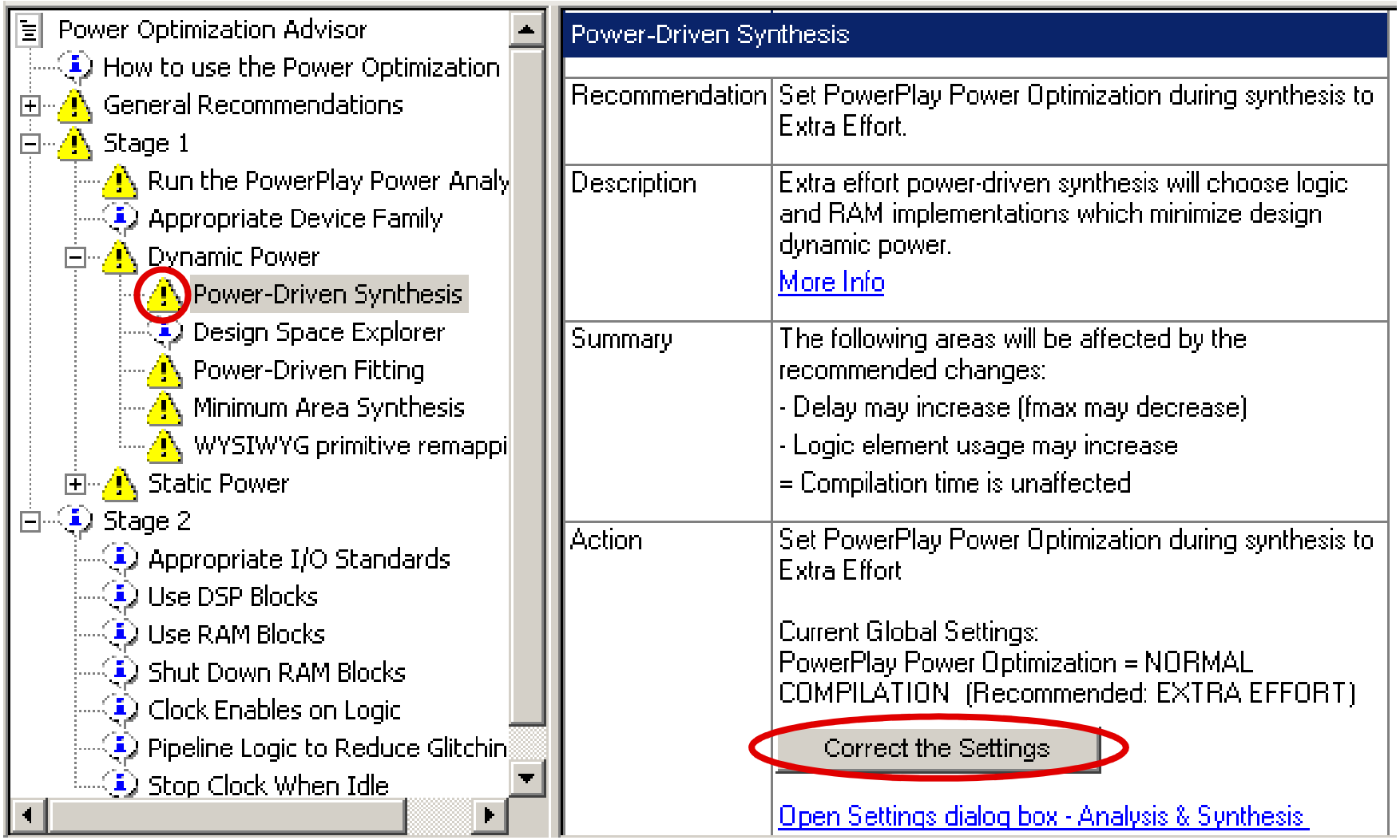
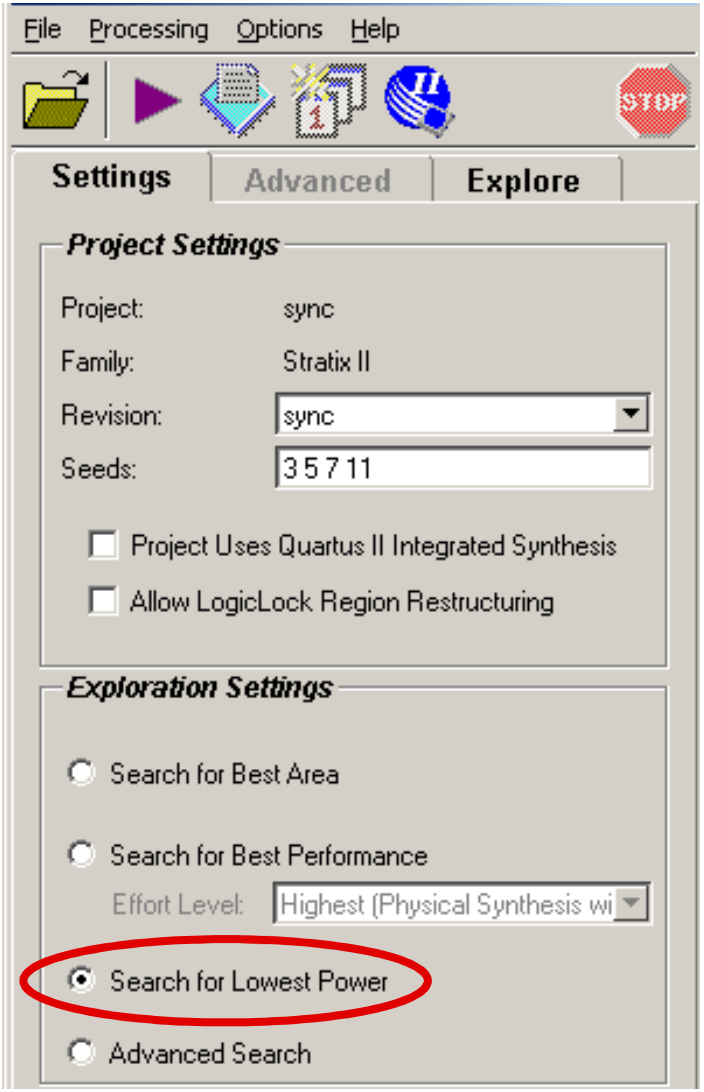
Power Optimization Advisor



Design Space Explorer

- Searches Quartus options to find best implementation
  - "Search for Lowest Power"
  - Finds settings that minimize power & meet timing
  - quartus_sh --dse
    or Tools Menu



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Summary & Wrap Up

Altera's PowerPlay Suite

- Most accurate power analysis tools
- Automatic power optimization
  - Industry first
  - Highly effective
  - 20% to 25% dynamic power reduction on average
- Power Optimization Advisor guides you to lower power

Better Tools: Lower Power & No Surprises

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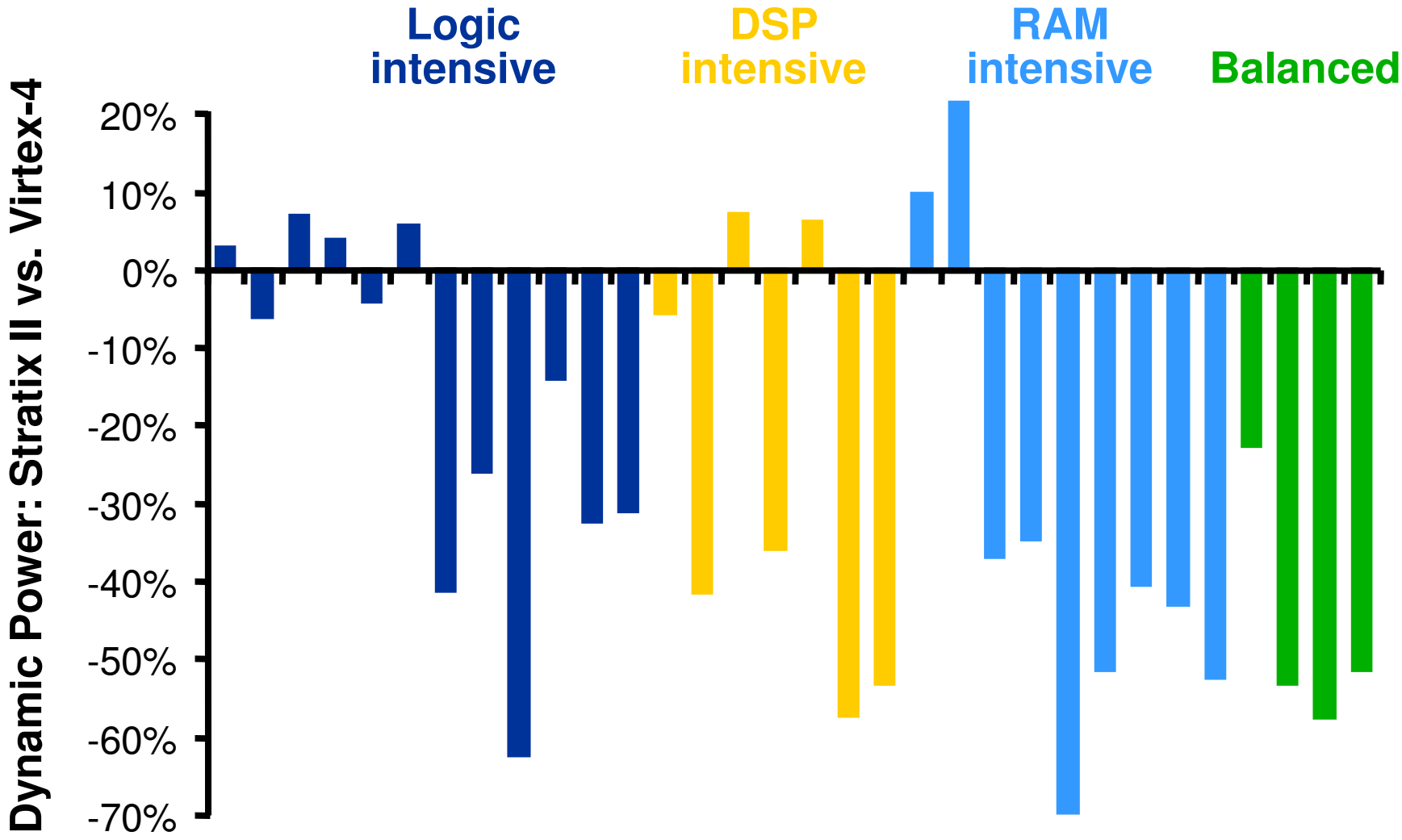
Stratix II vs. Virtex-4 Power



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Power & Altera Hardware

- Stratix II
  - Lowest dynamic power & lowest total power for 90nm high-density FPGAs
- Cyclone™ II
  - Lowest power of any FPGA
- HardCopy® II
  - Smooth migration to lower power
  - Typical: **2X to 3X reduction** vs. FPGA

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Resources & More Information

- Quartus II Handbook Volume 2, Chapter 9. - Power Optimization
  www.altera.com/quartus2
- Stratix II power page
  www.altera.com/stratix2power
- Cyclone II power page
  www.altera.com/cyclone2power
- Power management resource center
  www.altera.com/power

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Thank You

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