Learn to Design with Stratix III FPGAs’ Programmable Power Technology and Selectable Core Voltage

Vaughn Betz and Sanjay Rajput
Agenda

- The power challenge
- Stratix® III power innovations
  - Programmable power
  - Selectable core voltage
  - Quartus® II power optimization
  - IO power: On-chip dynamic termination and DDR3
- Device selection and competitive overview
- Wrap up
Altera’s End Customers

**Consumer Broadcast Automotive**
- Entertainment
  - Broadband
  - Audio/video
  - Video display
- Broadcast
  - Studio
  - Satellite
  - Broadcasting
- Automotive
  - Navigation
  - Entertainment

**Test, Measurement and Medical**
- Instrumentation
  - Medical
  - Test equipment
  - Manufacturing

**Communications**
- Wireless
  - Cellular
  - Base stations
  - Wireless LAN
- Networking
  - Switches
  - Routers
- Wireline
  - Optical
  - Metro
  - Access

**Military and Industrial**
- Military
  - Secure comm.
  - Radar
  - Guidance and control
- Security and Energy Management
  - Card readers
  - Control systems
  - ATM

**Computer and Storage**
- Computers
  - Servers
  - Mainframe
- Storage
  - RAID
  - SAN
- Office Automation
  - Copiers
  - Printers
  - MFP
The Challenge: System Design Trend

High-End System Version 1.0 → Next Generation Design → High-End System Version 2.0

<table>
<thead>
<tr>
<th>New System Requirements</th>
<th>Stratix III FPGAs</th>
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<tr>
<td>Same or Lower Power Budget</td>
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Meeting the Power Challenge

- Increased Performance
- 65 nm (Increased Leakage)
- Increased Density

Power vs. Density

- Stratix II
- 1.5M Gates
- 3.0M Gates
Meeting the Power Challenge

Stratix III FPGAs cut power by 50% vs. 90 nm
Benefits of Lower Power

- Stay within a fixed power budget
  - Chassis limits (heat, space, current)
  - Outside power budget \( \rightarrow \) not an option

- Reduce system cost
  - Fewer/smaller heat sinks and fans
  - Smaller power supplies

- Increase reliability
  - No fans \( \rightarrow \) no moving parts
  - Lower system temperature

- Reduce design time and effort to meet power and thermal constraints
Stratix III FPGAs: Lower Power, Higher Performance
## Industry-Leading Low-Power Technology

<table>
<thead>
<tr>
<th>Stratix III FPGA Power Reduction Technique</th>
<th>Lower Static Power</th>
<th>Lower Dynamic Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Process Optimizations</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Programmable Power Technology</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Selectable Core Voltage (0.9 V or 1.1 V)</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Power Optimized DDR Memory Interface</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Quartus II Software PowerPlay Power Analysis and Optimization</td>
<td>✓</td>
<td>✓</td>
</tr>
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</table>
Leading Edge Process Technology
Increased Performance, Reduced Power

- Advanced 65-nm process
  - 15% capacitance reduction → reduces dynamic power 15%
  - Lower voltage → reduces dynamic power another 16%

- Multiple-gate oxide thicknesses (triple oxide)
  - Trade-off static power vs. speed per transistor

- Multiple-threshold voltages
  - Trade-off static power vs. speed per transistor

- Low-k inter-metal dielectric
  - Reduces dynamic power, increases performance

- Strained silicon
  - Increased performance

- Copper interconnect
  - Increased performance, reduced IR drop
Programmable Power
Design-Specific Power Optimization

- Only a small fraction of logic is performance critical

Slack Histogram

- Not Performance Critical
- Performance Critical

Number of Connections

Slack %

- 90-100%
- 80-90%
- 70-80%
- 60-70%
- 50-60%
- 40-50%
- 30-40%
- 20-30%
- 10-20%
- 0-10%
Programmable Power Technology

Logic Array

Timing Critical Path

High-Speed Logic
Programmable Power Technology

Logic Array

Timing Critical Path

High-Speed Logic

Low-Power Logic
Programmable Power Technology

* Power mapping fully automated by Quartus II based on timing constraints

High-speed Logic
Low-power Logic
Unused Low-power Logic

High performance where you need it, lowest power everywhere else
High Speed/Low Power

- Low-power mode for a tile results in
  - 60% reduction in static power
  - 5% reduction in dynamic power
  - ~20% increase in delay
    - Quartus II CAD system doesn’t use on critical paths
    - No impact on system speed

- Tiles can be
  - Pair of Logic Array Blocks (LABs)
  - RAM block
  - DSP block
High-Resolution Power Control

Stratix III FPGA (EP3SL340) has **8,050 Tiles** for very high resolution power/performance optimization.

Only a small percentage of high-speed tiles required to maintain design performance.

**Speed of the fastest LABs**
**power of the slowest**
Most Tiles Are Low Power

All Clocks At Maximum Speed (Worst Case)

Average: 19% High Speed

Complete Customer Design
Static Power Tamed (85°C)

- Stratix II
- Stratix III

Typical High-Performance Design (1.1V)

All Low-Power Tiles (1.1V)
Real Customer Designs

Stratix II Advantage

Stratix III Advantage

Low Power
Without
Sacrificing
Performance

Average: 25%
Increase

F_{MAX} Ratio: Stratix III vs. Stratix II

Designs

Real Customer Designs

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Using Programmable Power

- Circuit board requirements: none!
  - Stratix III FPGAs create low-power tiles using on-chip circuitry
  - No extra power supplies, no extra board components

- Design changes: none!
  - Quartus II software automatically uses high-speed tiles where needed for timing
  - All unused tiles set to low power
  - All tiles with timing margin set to low power
  - Failed timing constraints: all tiles not on critical paths set to low power
Programmable Power Controls

- High-speed tile usage always optimized
- Extra effort lowers high-speed usage (by a few %)
  - Also reduces dynamic power (average 15% vs. off)
  - At ~20% compile time cost
- Advanced options under Fitter | More Settings
Selectable Core Voltage

- Customer selects the FPGA core voltage
  - 1.1 V for maximum performance
  - 0.9 V for minimum power

- I/O and PLL voltages unaffected
  - Still get maximum I/O interface speed
  - Crucial, since I/O bandwidth limits many systems

<table>
<thead>
<tr>
<th>Nominal Voltage</th>
<th>Min. Regulator $V_{OUT}$</th>
<th>Max. Regulator $V_{OUT}$</th>
<th>Slow Timing Model</th>
<th>Fast Timing Model</th>
<th>Power Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1 V</td>
<td>1.05 V</td>
<td>1.15 V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>0.9 V</td>
<td>0.86 V</td>
<td>0.94 V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
Selectable Core Voltage

Variable Voltage Region

- ALMs
- M9K Blocks
- M144K Blocks
- DSP Blocks
- I/Os and Interface Circuitry
- Phase-Locked Loops (PLLs)
- Delay-Locked Loops (DLLs)
Power and Timing Impact

<table>
<thead>
<tr>
<th>Core Voltage</th>
<th>Dynamic Power Reduction From Stratix II FPGAs</th>
<th>Static Power Reduction From Stratix II FPGAs</th>
<th>Performance Gain Over Stratix II FPGAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1 V</td>
<td>33%</td>
<td>52%</td>
<td>25%</td>
</tr>
<tr>
<td>0.9 V</td>
<td>55%</td>
<td>64%</td>
<td>0%</td>
</tr>
</tbody>
</table>

More choice to meet your power and performance budgets
Even Lower Static Power (85°C)

- Stratix II
- Stratix III

- Typical high-performance design (1.1V)
- All low-power tiles (1.1 V)
- All low-power tiles (0.9 V)

Core Static Power (W) vs. Number of LEs
Using Selectable Core Voltage

- Provide 0.9 V and 1.1 V supplies to FPGA
  - Risk mitigation: provide two supplies on board if concerned about power budget
  - Set voltage regulator output to 0.9 V if power budget exceeded at 1.1 V

- Quartus II software:
  - Select -4L speed grade
  - Select 0.9 V operation
Power Optimized DDR Memory Interface
Stratix III On-Chip Termination (OCT)

- Both parallel (Rt=50Ω) and series (Rs=50Ω) termination

(*) DDR 1/2/3, RLDRAMII, QDR II/II+ support
Stratix III FPGA Dynamic OCT

- **Write**: Rs on, Rt off → Matching line impedance
- **Read**: Rs off, Rt on → Terminating far end

**Write**
- Stratix III FPGA (TX)
- Memory Chip

**Read**
- Stratix III FPGA (RX)
- Memory Chip
Benefits of Dynamic OCT

1. Power significantly reduced vs. traditional parallel OCT
   - Saves 1.6 W of DC power on 72-bit DDR2 bus

2. Proper line termination and impedance matching on bidirectional busses
   - Enhanced signal integrity

3. No need for on-board termination resistors
Stratix III FPGAs Support DDR3

- Stratix III: The only FPGA that supports DDR3
- DDR3 is **30% lower power** than DDR2
  - DDR2: 1.8V
  - DDR3: 1.5V

- Example system:
  - 72-pin 200MHz memory interface, with on-chip termination
    - Conventional FPGA DDR2 power: 3.9 W
    - Stratix III (dynamic OCT) DDR2 power: 2.3W
    - Stratix III (dynamic OCT) DDR3 power: 1.6W
  - **Total savings of 2.3 W**
PowerPlay: Automatic Optimization

Set compiler settings to focus on reducing power

Design Entry] Constraints

Synthesis
Optimize Power ✓

Place and Route
Optimize Power ✓

PowerPlay Power Analyzer

Power-Optimized Design ✓
Automatic Programmable Power

1. Synthesis
2. Place and Route
3. Unused Tiles → Low Power
4. Timing Analyze
5. Tiles with Timing Slack → Low Power
6. Done?
   - No
   - Yes

- All High-Speed Tiles
- Mostly Low-Power Tiles
Power-Optimized RAM Mapping

**Default Option**

- Four 2Kx8 M9K RAMs

**Power Efficient Option**

- 2:4 Decoder
- Four 512x32 M9K RAMs
Power-Driven Place and Route

- Minimize capacitance of high-toggling signals
- Without violating timing constraints

20 Million Toggle/s 100 Million Toggle/s

Power Optimize
Clock Shut Down Hardware

- Stratix III FPGAs: Can shut down clock at 3 levels of tree
  - Top-level: Shut down 1/16 of clock tree
  - Next-level: 1/500 of clock tree
  - Bottom-level: 1/10,000 of clock tree
Placement to Reduce Clock Power

Clocking Legal, Timing Optimized

Power Optimize

Group Clocks for Maximum Shutdown

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PowerPlay Power Optimization

Automatic, but less accurate
Requires testbench, more accurate

Design

Estimate Toggle Rates

Vectorless Estimation
RTL Simulation

Power-Driven Synthesis

Normal or Extra Effort

Power-Driven Fit

Power Analyzer

Power Report
Dynamic Power Optimization

Dynamic Power Reduction vs. Minimum Effort

Extra Effort

Normal Effort

Design
Device Selection for Power

Use Altera’s Early Power Estimator

- Accurate
- Allows what-if analysis of different voltages
- Best option if no code has been written
- After implementation, Quartus II PowerPlay Power Analyzer provides the best estimate
  - Knows exact design utilization, block configurations, routing, signal behavior, etc.
Buyer Beware

- Not all power estimators are accurate
  - Especially for dynamic power

- Xilinx XPE – XPower estimator
  - Register power greatly underestimated
  - IO power greatly underestimated
    - Example: estimating memory interface power
  - Does not report any clock power – not modeled
  - LUT fan-out unrealistically low (2)
How Good Are the Estimates?

- Compare estimates to silicon measurements
  - Import design info from FPGA CAD tool to estimator
  - Obtain dynamic power estimate with correct toggle rates
  - Compare to silicon measurement of dynamic power

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<tr>
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<th>Stratix II EPE Ver. 6.1 % Error</th>
<th>Virtex-5 XPE Ver. 9.1 % Error</th>
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<tbody>
<tr>
<td>counter_16x1024</td>
<td>9%</td>
<td>-40%</td>
</tr>
<tr>
<td>grey6</td>
<td>22%</td>
<td>-56%</td>
</tr>
<tr>
<td>des3_6</td>
<td>-3%</td>
<td>-81%</td>
</tr>
<tr>
<td>rijndael_iter</td>
<td>-20%</td>
<td>-31%</td>
</tr>
<tr>
<td>tessierbeamform_12beams</td>
<td>28%</td>
<td>-36%</td>
</tr>
<tr>
<td>mult_18x18_32copies</td>
<td>14%</td>
<td>-60%</td>
</tr>
<tr>
<td>ram_8192dx64wx1</td>
<td>13%</td>
<td>-32%</td>
</tr>
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Negative number = Underestimation (Bad)
Positive number = Overestimation (Safe)
40% Power Advantage for Stratix III

Total Power For Typical Design

* Total power (Dynamic + Static + IO), 85°C junction temp., equivalent density devices, average customer usage of logic, memory, multipliers, and IO.
Performance Benchmarking

- Fastest speed grades are compared
- Full timing constraints for each design
  - Tight $f_{\text{MAX}}$ constraint for each clock domain
  - I/O constraint on all pins
- Best effort (true FPGA performance)
  - Multiple compilations to get best result
- See “How Fast is the Fastest FPGA” net seminar for more details
Relative Core Performance Comparison

Stratix III (fast) vs. Virtex-5 (fast)

Stratix III FPGAs Average One Speed Grade Faster than Virtex-5

Alterna Advantage

Customer Designs
Summary

- **Stratix III FPGAs**
  - Meet the power challenge of next generation designs
  - With the highest performance AND lowest power

- **Power reduction**
  - Excellent process technology and engineering
  - Programmable power
  - Selectable core voltage
  - Power-efficient DDR interface
  - Quartus II software power optimization

- Lower power and higher performance than any competitive FPGA
More Resources

- **Stratix III website** - [www.altera.com/stratix3](http://www.altera.com/stratix3)
  - Click on “Programmable Power Technology” to learn more about this and other Stratix III power related features

- **Programmable Power White Paper**

- **Stratix III EPE – power estimation spreadsheet**
  - User guide available on this page

- **Download Quartus II software and start designing with Stratix III FPGAs today**
  - [www.altera.com/download](http://www.altera.com/download)
Quartus II v6.1 Supports Stratix III FPGAs
Quartus II v6.1 Supports Stratix III FPGAs

- Quartus II web edition v6.1

- Quartus II subscription edition v6.1
  - Supports all Stratix III devices
Additional Stratix III Net Seminars

- Overview of Altera’s 65-nm Stratix III FPGAs (10 minutes)
- Using Stratix III FPGAs to Achieve Higher Performance Systems with Lower Power (60 minutes)
- How Fast is the Fastest FPGA? Stratix III Performance Capabilities (60 minutes)
- Upcoming Stratix III Net Seminar (June 2006): How to Maximize Performance with Stratix III FPGAs Using Quartus II Software (60 minutes)