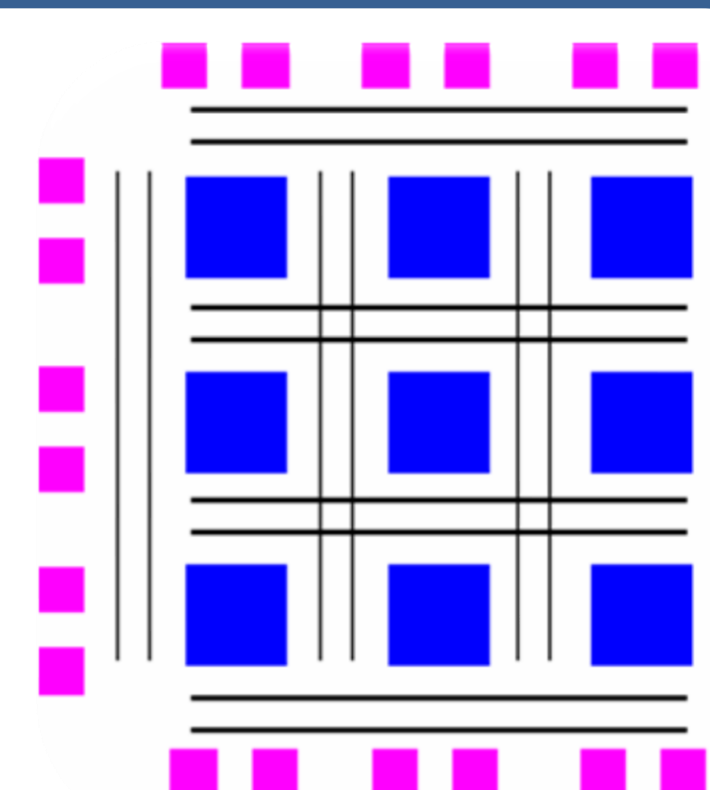


# Enabling Realistic Benchmark Testing in Academic FPGA Design

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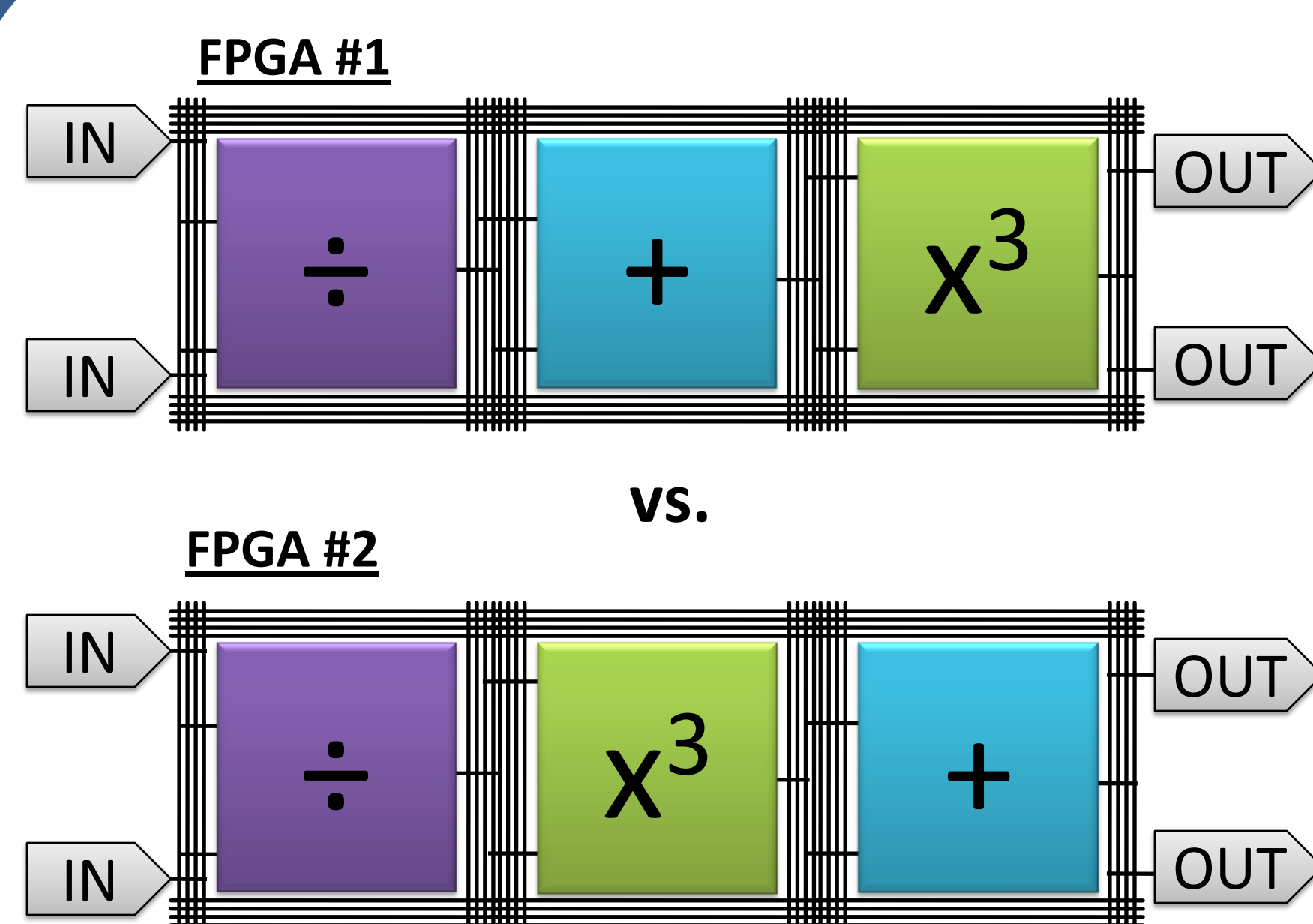
## What is an FPGA?

A **Field-Programmable Gate Array (FPGA)** is a software-configurable digital hardware chip. An FPGA Designer creates a digital circuit which is translated by software and then sent to the chip. The chip then configures its logic appropriately and connects it as required by the Designer.



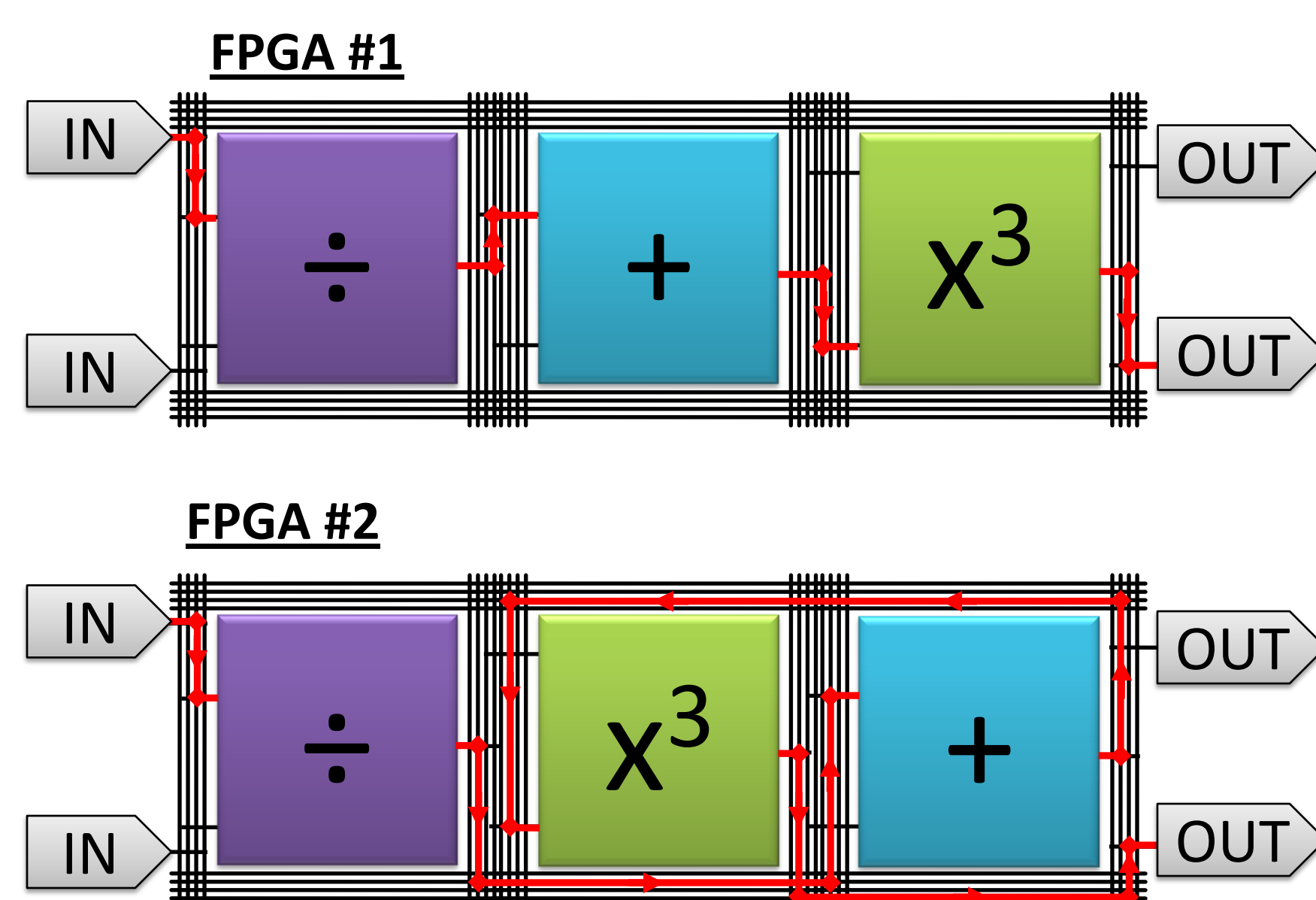
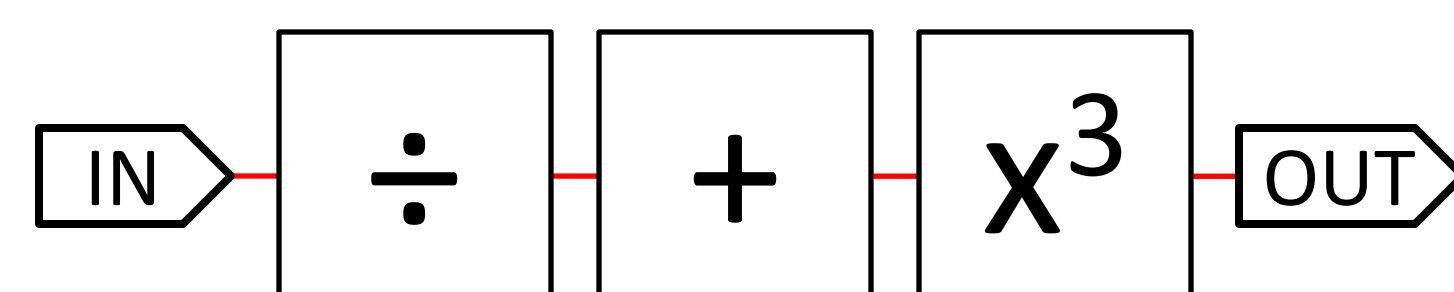
These chips have many modern applications including internet routers, medical imaging technology, and fish range finders.

## Creating FPGAs



Creating an FPGA architecture is a very complex task. Simply given two different hypothetical FPGAs, it is often difficult to determine which is better. The best way to compare two architectures is to implement standardized **benchmark circuits** on each and then compare the results.

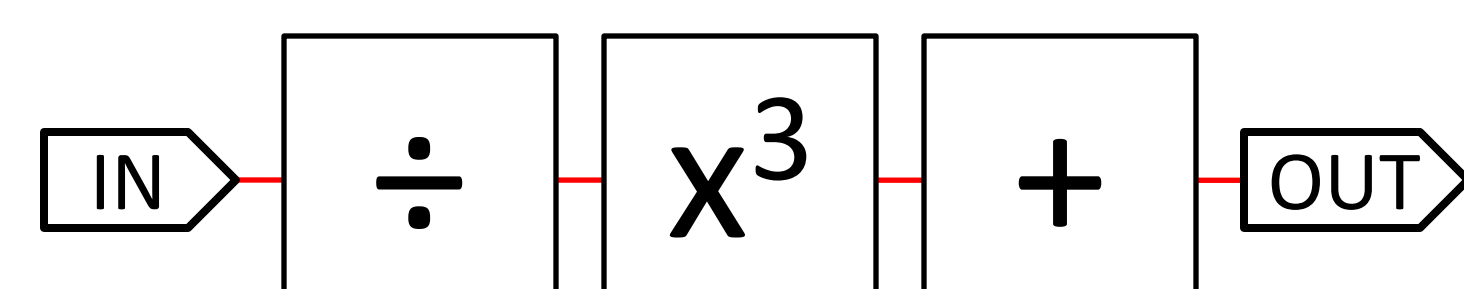
Benchmark Circuit #1



When this benchmark is implemented on FPGA #1, it requires much fewer **routing resources** than when it is implemented on FPGA #2. This means FPGA #1 will use less power and run faster than FPGA #2.

So clearly #1 is the better FPGA architecture. Right?

Benchmark Circuit #2

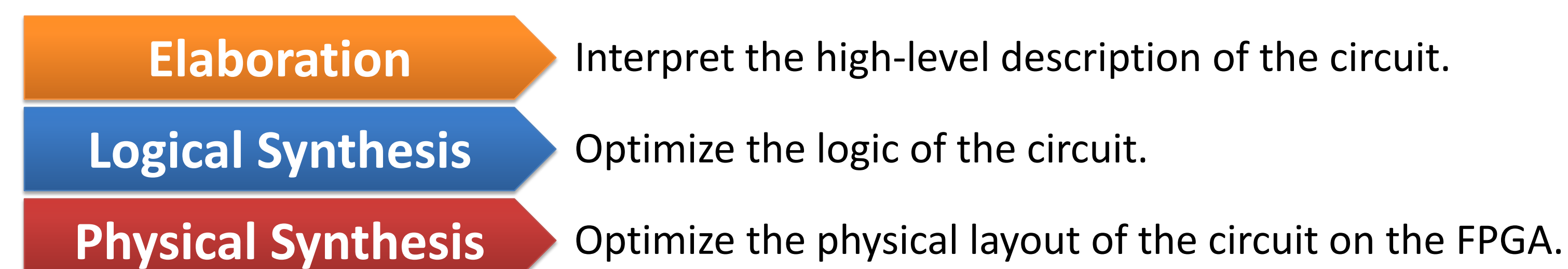


It depends on the benchmark!

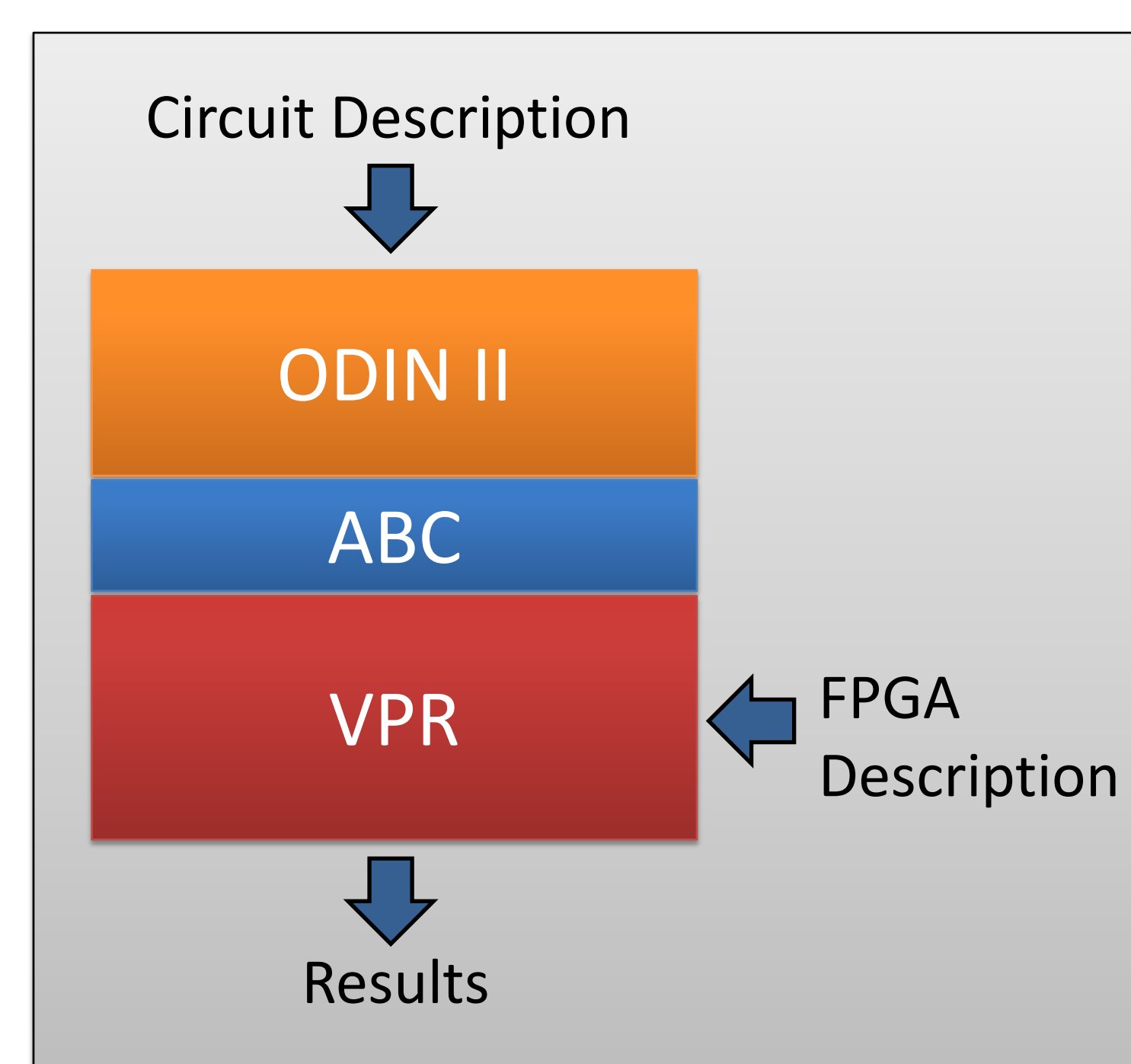
When creating an FPGA, benchmark circuits are critical in evaluating different design decisions. However, **which** benchmarks you use is just as important. Modern FPGA users have incredibly large and complex requests, so it is very important to test with large and complex benchmarks. Otherwise, the results may not accurately reflect the FPGA's real-world applicability.

## A New FPGA Software Flow

The process of testing a circuit on an FPGA is generally comprised of several individual software tools that create a **flow**. There are three key phases to these flows:



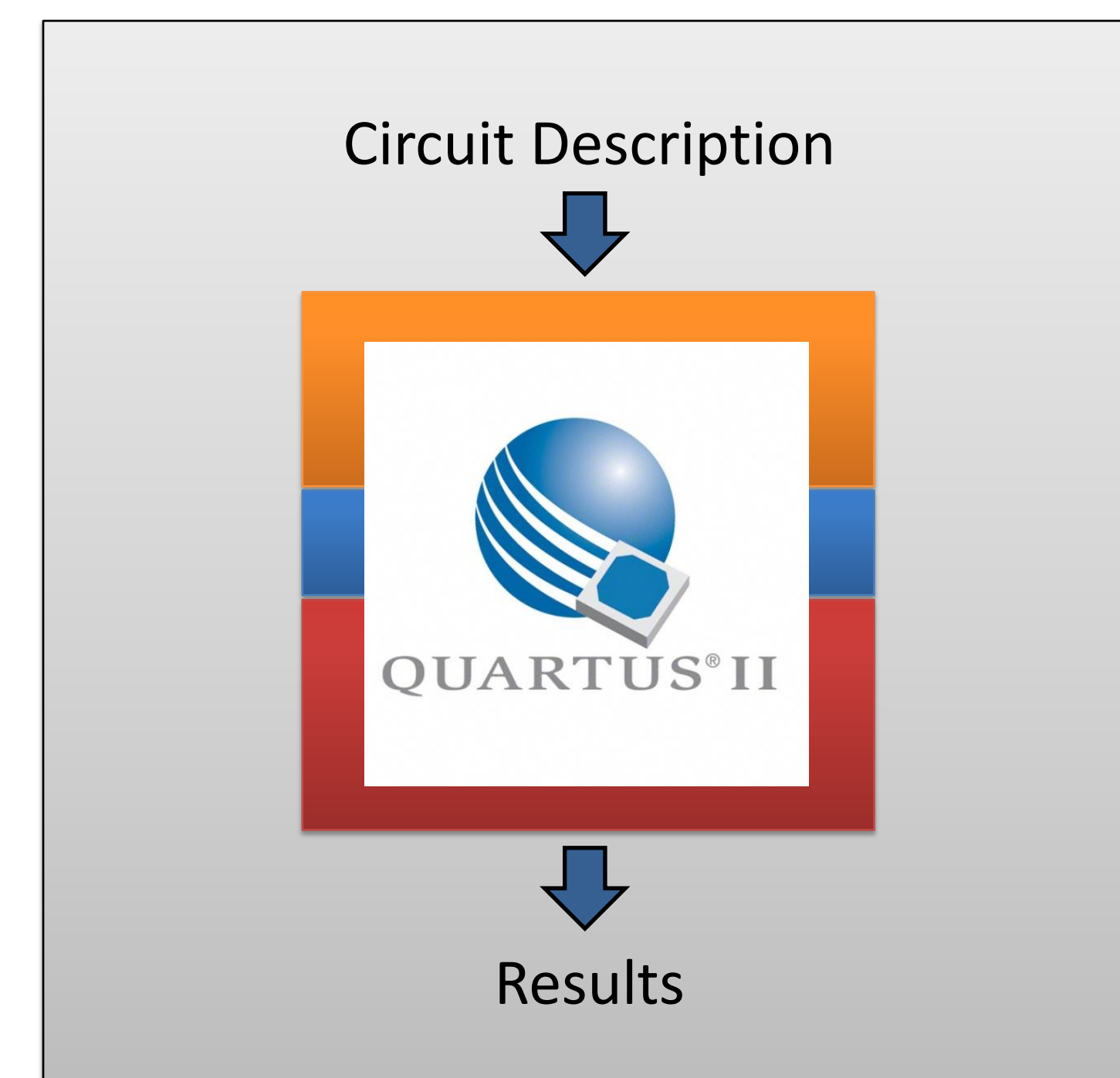
### Academic Flow 1,2,3



**Pro:** The software takes a hypothetical FPGA as input, allowing the user to test their own architectures against each other.

**Con:** ODIN II does not support the full IEEE Standard 1364-1995 Verilog Hardware Description Language or its later versions. This means it cannot interpret the vast majority of large developed circuits, and it is difficult and very time consuming to convert them.

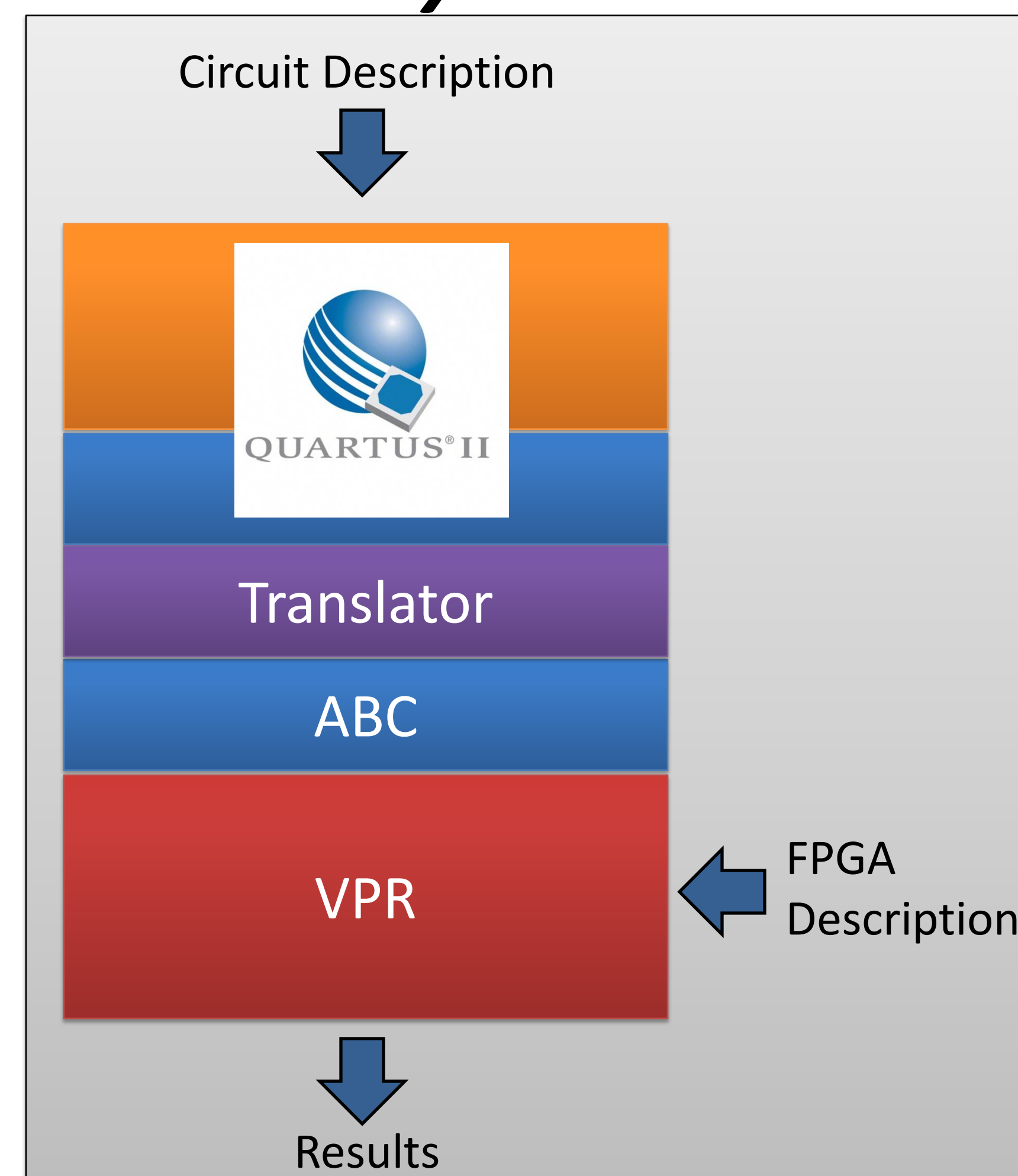
### Industrial Flow



**Pro:** Many modern developers and researchers use Altera's Quartus® II to make their circuits, which means it can handle realistic benchmarks.

**Con:** The commercially available software can only implement circuits on a predefined set of FPGAs, which disallows users from testing their own architectures.

### Hybrid Flow



By using the powerful interpretation capability of Quartus II and the data-driven nature of the academic tools, a new flow was created that can implement large, realistic benchmarks on a hypothetical FPGA architecture.

To make this new flow possible, Quartus II is interrupted and it outputs an intermediate file describing the circuit. A translator tool then converts that file into a format compatible with ABC and VPR.

## Results

	Logic Elements	Memory Bits	Multipliers
diffeq1*	222	0	12
diffeq2*	223	0	12
fir_filter	759	0	0
LU8PEEng	9781	2700	32
LU64PEEng	60752	18407	256
ch_dfsin	20681	217	72
mcml	11763	600	72
or1200*	3359	242	4
blob_merge*	5330	0	0
reed_solomon*	3184	120	0
sha*	772	0	0
spree	765	128	4

This new benchmark suite has been successfully passed through the **Hybrid Flow**, allowing future exploration of new FPGA architectures using such realistic circuits.

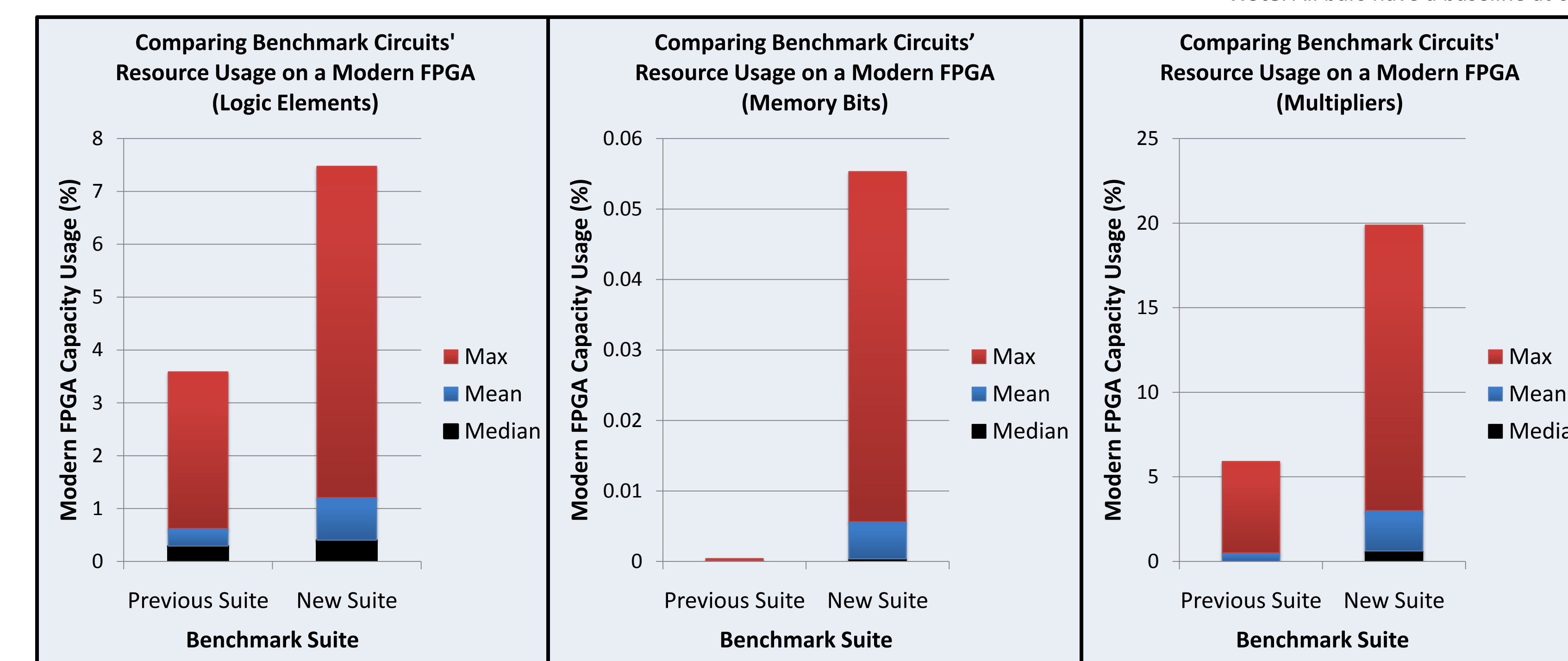
A previous benchmark suite was released in March 2011 with the **Academic Flow**. Their sizes are compared to the new suite below, relative to the percentage of an Altera Stratix IV® FPGA they consume.

\* - Member of the previous benchmark Suite, released March 2011

For reference, the Stratix IV E Family of Devices has a maximum of: <sup>4</sup>

**813,050** Logic Elements  
**33,294,000** Memory Bits  
**1,288** 18x18 Multipliers

Note: All bars have a baseline at 0.



Although the new suite shows a marked improvement from previous benchmarks, there is still need for more realistic benchmarks. Future work includes gathering even larger, more complex circuits to add to the suite.

## References

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