FPGA 2014
Program

Wednesday February 26

2:00pm **Workshop: FPGAs in the Datacenter (Marriott Hotel San Carlos 3/4)**

Chair: Derek Chiou, University of Texas at Austin

This workshop will explore the promise, opportunities, and challenges of using FPGAs in the data center. We will hear from potential data center users of FPGAs, such as Microsoft and Google, system vendors such as IBM, and semiconductor manufacturers such as Intel.

7:00pm **Conference Reception (Marriott Hotel Ferrantes Room)**

Thursday February 27

8:00am **Continental Breakfast & Registration (Steinbeck Lobby)**

8:50am **Opening Remarks (Steinbeck Forum)**

George A. Constantinides and Vaughn Betz

9:10am **Session 1: Physical Design (Steinbeck Forum)**

Chair: Jonathan Rose, University of Toronto, Canada

Fast and Effective Placement and Routing Directed High-Level Synthesis for FPGAs
Hongbin Zheng, Swathi Gurumani, Kyle Rupnow and Deming Chen

Optimizing Effective Interconnect Capacitance for FPGA Power Reduction
Safeen Huda, Jason Anderson and Hirotaka Tamura

Towards Interconnect-Adaptive Packing for FPGAs
Jason Luu, Jonathan Rose and Jason Anderson

Rent's Rule Based FPGA Packing for Routability Optimization (short)
Wenyi Feng, Jonathan Greene, Kris Vorwerk, Val Pevzner and Arun Kundu

10:15am **Poster Session 1 (Colton Room)**

11:15am **Session 2: Architecture (Steinbeck Forum)**

Chair: Mike Hutton, Altera, USA

Modular Multi-ported SRAM-based Memories
Ameer M.S. Abdelhadi and Guy G.F. Lemieux

Revisiting And-Inverter Cones
Grace Zgheib, Liqun Yang, Zhihong Huang, David Novo, Hadi Parandeh-Afshar, Haigang Yang and Paolo Ienne

Scalable Multi-Access Flash Store for Big Data Analytics
Sang-Woo Jun, Ming Liu, Kermin Fleming and Arvind

12:15pm **Lunch**

2:00pm **Session 3: Tools and Methods (Steinbeck Forum)**

Chair: Jason Anderson, University of Toronto, Canada

Dynamic Voltage & Frequency Scaling with Online Slack Measurement
Joshua M. Levine, Edward A. Stott and Peter Y.K. Cheung

CAD and Routing Architecture for Interposer-Based Multi-FPGA Systems
Andre Hahn Pereira and Vaughn Betz

Memory Block Based Scan-BIST Architecture for Application-Dependent FPGA Testing (short)
Keita Ito, Tomokazu Yoneda, Yuta Yamato, Kazumi Hatayama and Michiko Inoue

2:45pm **Poster Session 2 (Colton Room)**

3:45pm **Session 4: Applications 1 (Steinbeck Forum)**

Chair: Patrick Lysaght, Xilinx, USA

FPGA-based Biophysically-Meaningful Modeling of Olivocerebellar Neurons
Georgios Smaragdos, Sebastian Isaza, Martijn Van Eijk, Ioannis Sourdis and Christos Strydis

Square-Rich Fixed Point Polynomial Evaluation on FPGAs
Simin Xu, Suhaib Fahmy and Ian McLoughlin

4:25pm **Break before banquet**

6:30pm **Banquet & Panel (Marriott)**

Friday February 28

9:00am **Session 5: Processors and Systems (Steinbeck Forum)**

Chair: Miriam Leeser, Northeastern University, USA

Soft Vector Processors with Streaming Pipelines
Aaron Severance, Guy Lemieux, Hossein Omidian and Joe Edwards

MORP: Makespan Optimization for Processors with an Embedded Reconfigurable Fabric
Artjom Grudnitsky, Lars Bauer and Jörg Henkel

OmpSs@Zynq All-Programmable SoC Ecosystem
Antonio Filgueras, Eduard Gil, Daniel Jimenez, Carlos Alvarez, Xavier Martorell, Jan Langer and Juanjo Noguera

A FPGA Prototype Design Emphasis on Low Power Technique (short)
Xu Hanyang, Lai Jinmei and Wang Jian

10:05am **Poster Session 3 (Colton Room)**

11:00am **Session 6: Applications 2 (Steinbeck Forum)**

Chair: Lesley Shannon, Simon Fraser University, Canada

Hardware Acceleration of Database Operations

Jared Casper and Kunle Olukotun

A Scalable Sparse Matrix-Vector Multiplication Kernel For Energy-Efficient Sparse-BLAS On FPGAs
Richard Dorrance, Fengbo Ren and Dejan Markovic

Binary Stochastic Implementation of Digital Logic
Yanzi Zhu, Peiran Suo and Kia Bazargan

Accelerating Parameter Estimation for Multivariate Self-Exciting Point Processes (short)
Ce Guo and Wayne Luk

Energy-Efficient Multiplier-Less Discrete Convolver through Probabilistic Domain Transformation (short)
Mingjie Lin

12:10pm Lunch

2:00pm Session 7: Tools and Models 1 (Steinbeck Forum)

Chair: Deming Chen, University of Illinois at Urbana-Champaign, USA

Wordwidth, Instructions, Looping, and Virtualization: The Role of Sharing in Absolute Energy Minimization
Andre DeHon

Theory and Algorithm for Generalized Memory Partitioning in High-Level Synthesis
Yuxin Wang, Peng Li and Jason Cong

Using High-level Synthesis and Formal Analysis to Predict and Preempt Attacks on Industrial Control Systems (short)
Lee W. Lerner, Zane R. Franklin, William T. Baumann and Cameron D. Patterson

MPack: Global Memory Optimization for Stream Applications in High-Level Synthesis (short)
Jasmina Vasiljevic and Paul Chow

A soft error vulnerability analysis framework for Xilinx FPGAs (short)
Aitzan Sari, Dimitrios Agiakatsikas and Mihalis Psarakis

A Power-Side-Channel Based Digital to Analog Converter for Xilinx FPGAs (short)
Danny Savory, Joshua Monson and Brad Hutchings

Accelerating Frequent Item Counting with FPGA (short)
Yuliang Sun, Zilong Wang, Sitao Huang, Lanjun Wang, Yu Wang, Rong Luo and Huazhong Yang

3:05pm Poster Session 4 (Colton Room)

3:55pm Session 8: Tools and Models 2 (Steinbeck Forum)

Chair: Kyle Rupnow, Nanyang Technological University, Singapore

Combining Computation with Communication Optimizations in System Synthesis for Streaming Applications
Jason Cong, Muhuan Huang and Peng Zhang

Quantifying the Cost and Benefit of Latency Insensitive Communication on FPGAs
Kevin Edward Murray and Vaughn Betz

4:35pm **Best Paper Award and Closing Remarks (Steinbeck Forum)**

George A. Constantinides and Vaughn Betz

Posters

Poster Session 1:

FPGA LUT Design for Wide-band Dynamic Voltage and Frequency Scaled Operation
Monther Abusultan and Sunil Khatri

A Configurable MapReduce Accelerator for Multi-core FPGAs
Christoforos Kachris, Georgios Sirakoulis and Dimitrios Soudris

A New Basic Logic Structure for Data-Path Computation
Pierre-Emmanuel Gaillardon, Luca Amaru and Giovanni De Michele

A Methodology for Identifying and Placing Heterogeneous Cluster Groups Based on Placement Proximity Data
Farnaz Gharibian, Lesley Shannon and Peter Jamieson

A Scalable Routability-driven Analytical Placer with Global Router Integration for FPGAs
Ka Chun Lam, Wai-Chung Tang and Evangeline F.Y. Young

Towards High Performance GHASH for Pipelined AES-GCM Using FPGAs
Karim Abdellatif

Hierarchical Library Based Power Estimation for Versatile FPGAs
Hao Liang, Yi-Chung Chen, Wei Zhang and Hai Li

Network-level FPGA acceleration of low latency market data feed arbitration
Stewart Denholm, Hiroaki Inoue, Takashi Takenaka and Wayne Luk

Optimally Mitigating BTI-Induced FPGA Device Aging with Discriminative Voltage Scaling
Mingjie Lin

Poster Session 2:

Loop Transformations for Throughput Optimization in High-Level Synthesis
Peng Li, Louis-Noel Pouchet, Deming Chen and Jason Cong

On Hybrid Memory Allocation for FPGA Behavioral Synthesis
Qian Zhang, Chenfei Ma and Qiang Xu

Pushing the Performance Boundary of Linear Projection Designs Through Device Specific Optimisations
Rui Policarpo Duarte and Christos-Savvas Bouganis

Accelerating Hash-based Algorithms for Mapping Massive Next Generation Sequencing Data
Guangming Tan

Application Specific Processor with High Level Synthesized Instructions

Viktor Puš and Pavel Benáček

Design, Implementation and Security Analysis of Hardware Trojan Threats in FPGA
Devu Manikantan Shila and Vivek Venugopal

A Power-Efficient Adaptive Heapsort for FPGA-based Image Coding Application
Yuhui Bai, Syed Zahid Ahmed and Bertrand Granado

MapReduce and FPGA Hybrid Architectures for Big Data Genome Sequencing Problem
Chao Wang, Xuehai Zhou and Ray Cheung

Low-Power Reconfigurable Controllers for Wireless Sensor Network Nodes
Vivek D. Tovinakere, Olivier Sentieys and Steven Derrien

A Platform for Frequent Pattern Mining in FPGA Devices
Ali Ebrahim, Jalal Khalifat and Tughrul Arslan

BMP: A Fast B*-Tree based Modular Placer for FPGAs
Fubing Mao, Yi-Chung Chen, Wei Zhang and Hai Li

Redefining the Role of FPGAs in the Next Generation Avionic Systems
Venkatasubramanian Viswanathan, Rabie Ben Atitallah, Jean-Luc Dekeyser, Benjamin Nakache and Maurice Nakache

Co-processing with Dynamic Reconfiguration on Heterogeneous MPSoC: Practices and Design Tradeoffs
Chao Wang and Xuehai Zhou

Control Signal Aware Slice-Level Window Based Legalization Method for FPGA Placement
Yu Wang, Sohail Muhammad, Donghoon Yeo and Hyunchul Shin

Poster Session 3:

Future Inter-FPGA Communication Architecture for Multi-FPGA Based Prototyping
Qingshan Tang, Matthieu Tuna and Habib Mehrez

FPGA Implementation of EM Algorithm for 3D CT Reconstruction
Young-kyu Choi and Jason Cong

1K Manycore FPGA Shared Memory Architecture for SOC
Yosi Ben Asher, Jacob Gendel, Oren Segal, Yousef Shajrawi and Gadi Haber

Non-Adaptive Sparse Recovery and Fault Evasion using d-disjunct Reconfigurable Logic Resources
Ahmad Alzahrani and Ronald DeMara

Novel FPGA Clock Network with Low Latency and Skew
Lei Li, Jian Wang and Jinmei Lai

Asynchronous Physical Unclonable Function using FPGA-based Self-Timed Ring Oscillator
Roshan Silwal and Mohammed Niamat

APMC: Advanced Pattern based Memory Controller
Tassadaq Hussain, Oscar Palomar, Adrián Cristal, Osman Unsal, Eduard Ayguadé and Mateo Valero

On Energy Efficiency and Amdahl's Law in FPGA Based Chip Heterogeneous Multiprocessor Systems

Sen Ma and David Andrews

Producing High-Quality Real-Time HDR Video System with FPGA
Tao Ai, Mir Adnan Ali, Gregory Steffan, Kalin Ovtcharov, Sarmad Zulfiqar and Steve Mann

xDEFENSE: An Extended DEFENSE for mitigating Next Generation Intrusions
James Lamberti, Devu Manikantan Shila and Vivek Venugopal

Coordinating Routing Resources for Hex PIPs Test in Island-style FPGAs
Zhang Fan, Chen Lei and Xu Wenyao

Pipelining FPGA Based Defect Detection for FPD
Meng Lin, Matsuyama Keisuke, Nojiri Naoto, Izumi Tomonori and Yamazaki Katsuhiro

Poster Session 4:

EPEE: An Efficient PCIe Communication Library with Easy-host-integration Property for FPGA Accelerators
Jian Gong, Jiahua Chen, Haoyang Wu, Fan Ye, Songwu Lu, Jason Cong and Tao Wang

Implementing FPGA-based Energy-efficient Dense Optical Flow Computation with High Portability in C
Zhibin Wang, Wenmin Yang, Jin Yu and Zhilei Chai

Methodology to Generate Multi-Dimensional Systolic Arrays for FPGAs using OpenCL
Nick Ni

Improving the security and the scalability of the AES algorithm
Alessandro A. Nacci, Vincenzo Rana, Marco D. Santambrogio and Donatella Sciuto

Power Estimation Tool for System on Programmable Chip based Platforms
Santhosh Kumar Rethinagiri, Oscar Palomar, Rabie Ben atitallah, Adrián Cristal and Osman Ünsal

Using DSP blocks to compute CRC hash in FPGA
Tomáš Závodník, Lukáš Kekely and Viktor Puš

Implementation of Gradient based adaptive interpolation on FPGA
Usha Patel and Vibha Patel

Exploring Duty Cycle Distortions along Signal Paths in FPGAs
Matthias Hinkfoth, Ralf Joost and Ralf Salomon