



Bandwidth Extension

Welcome to "Circuit Intuitions!" This is the fifth article of a column series that appears regularly in this magazine. As the title suggests, each article provides insights and intuitions into circuit design and analysis. These articles are aimed at undergraduate students but may serve the interests of other readers as well. If you read this article, I would appreciate your comments and feedback, as well as your requests and suggestions for future articles in this series. Please send your e-mails to ali@ece.utoronto.ca.

The past four articles in this series were all related to the small-signal operation of MOS circuits at low frequencies, and as such, we ignored all the parasitic capacitances in the circuits. In this article, we look at circuit behavior at higher frequencies, where the effect of parasitic capacitances cannot be ignored. We review a quick way of determining the bandwidth of single-pole circuits, and present methods of extending bandwidth.

A small-signal model of a transistor including its parasitic capacitances is shown in Figure 1, where g_m and r_o are the small-signal parameters at low frequencies, as introduced in the first article of this series, and C_{gs} , C_{gd} , C_{db} , and C_{sb} are parasitic capacitances when the transistor is in saturation region. We ignore g_{mb} in this model so as to simplify the analysis. We will now use this model to provide intuition into the frequency behavior of a common-source amplifier.

In the first article in this series, we said looking into a node we see the

Norton (or Thevenin) equivalent circuit, which consists of a current source in parallel with a resistor. Extending this concept to higher frequencies, we must replace the equivalent *resistance* by an equivalent *impedance* to take into account the effects of parasitic capacitances. Determining the frequency response of a circuit then becomes equivalent to determining the frequency response of RC circuits (assuming we have no inductors for now). Let us apply this idea to a simple common-source amplifier.

Figure 2 shows a common-source circuit with a capacitive load C_L being driven by an ideal voltage source V_{in} . We would like to determine the Norton equivalent of this circuit looking into its output node.

The short circuit current (I_{sc}) at the output can be written as

$$I_{sc} = (-g_m + sC_{gd})V_{in}.$$

This current is only affected by C_{gd} as all other capacitors are either shorted in this process (such as C_{db} , C_L , C_{sb}) or draw their own currents from the signal source but have no influence on I_{sc} .

Now let us determine the impedance looking into the output node. For this, we zero the voltage source and observe that the equivalent impedance is

$$Z_{eq} = R_{eq} \parallel \frac{1}{sC_{eq}},$$

where $R_{eq} = r_o \parallel R_L$, and $C_{eq} = C_L + C_{dg} + C_{db}$. Since $V_o = I_{sc} \times Z_{eq}$, we can write

$$\frac{V_o}{V_{in}}(s) = -g_m R_{eq} \frac{(1 - sC_{gd}/g_m)}{(1 + sR_{eq}C_{eq})}.$$

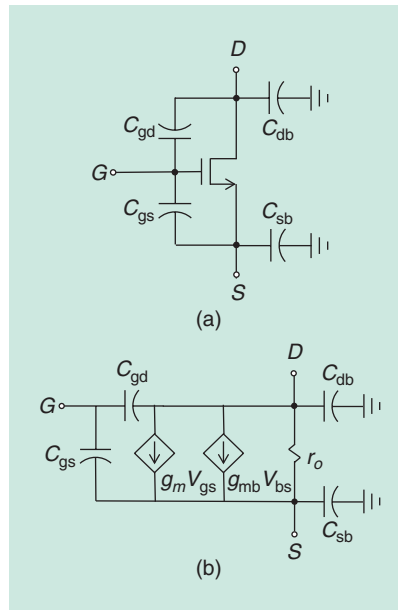


FIGURE 1: (a) An MOS transistor and its parasitic capacitances and (b) a MOS transistor small-signal model at high frequencies.

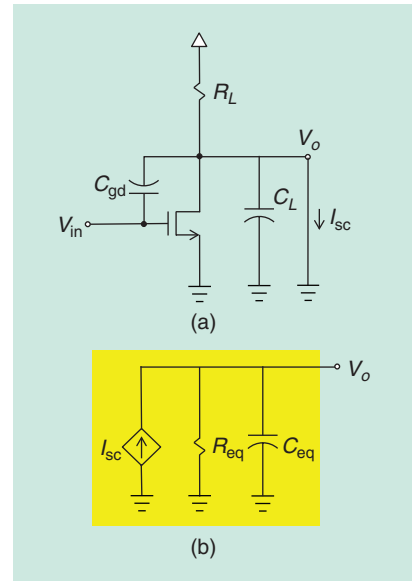


FIGURE 2: (a) A common-source amplifier with its load resistance and capacitance and (b) the Norton equivalent circuit at the output node.

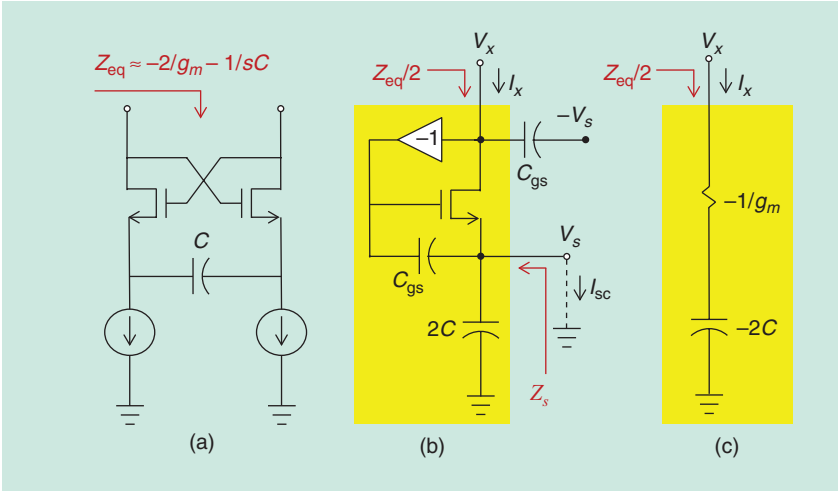


FIGURE 3: (a) A differential circuit creating negative capacitance, (b) a half-circuit equivalent, and (c) a simplified half-circuit equivalent.

The low-frequency ($s \approx 0$) gain of this amplifier is $-g_m R_{eq}$ and its bandwidth is given by

$$f_{3dB} = \frac{1}{2\pi R_{eq} C_{eq}},$$

which is also the bandwidth of the output impedance. In this example, the bandwidth is limited by the RC time constant at the output node. The question we would like to answer is how to extend the bandwidth of the circuit.

Since the bandwidth increases if we reduce $R_{eq} C_{eq}$, it seems natural to look at ways to reduce either R_{eq} or C_{eq} . Reducing R_{eq} has an undesirable effect of reducing the low-frequency gain. Let us then consider reducing the capacitance at the output node.

An effective way to reduce the capacitance of a node is to add

negative capacitance to that node. Since capacitances add when they are in parallel, the addition of negative capacitance in parallel reduces the equivalent capacitance without sacrificing the low-frequency gain.

Figure 3(a) shows one way to construct negative capacitance. To analyze this circuit, we draw its half circuit in Figure 3(b). To find the impedance of this circuit, we apply a voltage source, V_x , to the drain terminal and find its associated current I_x . Since $I_x \approx 2sCV_s$, we will first try to find V_s by finding the short-circuit current (to ground) from the source terminal and the equivalent impedance at the same terminal. Accordingly, we can write

$$\begin{aligned} I_{sc} &= (-g_m - sC_{gs})V_s \\ Z_s &= [g_m + s(C_{gs} + 2C)]^{-1} \\ V_s &= I_{sc}Z_s = \frac{-(g_m + sC_{gs})V_x}{g_m + s(C_{gs} + 2C)}. \end{aligned}$$

Given $I_x \approx 2sCV_s$, (ignoring the current through C_{gs}), we can now find an expression for V_x/I_x as in the following:

$$\begin{aligned} \frac{Z_{eq}}{2} &\approx -\frac{g_m + s(C_{gs} + 2C)}{(g_m + sC_{gs})(2sC)} \\ Z_{eq}/2 &\approx -1/g_m - 1/2sC, \end{aligned}$$

where the final approximation is made assuming $C_{gs} \ll 2C$ and $sC_{gs} \ll g_m$. The first of these two assumptions is made through the design choice. The

latter translates to operating the circuit at frequencies much lower than the transistor f_t , the frequency at which the short-circuit current gain of the transistor becomes unity.

The final equation clearly shows that looking into the drain of the transistor in Figure 3(b), we see a negative resistance ($-1/g_m$) in series with a negative capacitance ($-2C$), as depicted in Figure 3(c). These results can be explained intuitively as follows: At low frequencies, $-2C$ dominates the total impedance, and hence we see $-2C$ as the equivalent circuit for the half circuit or $-1C$ for the differential circuit. Note that the voltage seen by $2C$ is $-V_x$ (due to the source follower behavior of the transistor) while the voltage applied to the circuit is $+V_x$. This reversal of voltage causes a current in the opposite direction, effectively creating a negative capacitance.

Another method of increasing the bandwidth comes as a result of “thinking outside the box.” Since the bandwidth corresponds to the pole of the circuit, we can create a zero in the transfer function (in the vicinity of the original pole) so as to extend the bandwidth. This can be done by adding an inductor in series with the resistor connecting the drain terminal to the power supply, as shown in Figure 4, in a configuration known as shunt-peaking. Intuitively, the addition of the inductor does not change the short-circuit current at the output node (as the entire load is shorted to ground). However, it does change the output impedance as a function of frequency. While the impedance of the original circuit has a constant R_D in parallel with the C , the shunt-peaking circuit has $(R_D + j\omega L)$ in parallel with the same C . Since $(R_D + j\omega L)$ increases in magnitude with frequency, the overall impedance does not fall as quickly with frequency, and this leads to increased bandwidth. It can be shown [1] that the bandwidth of the shunt-peaking circuit can be higher than the original circuit by as much as 80%.

The added inductor could be designed as a passive element or as an active inductor using a MOS transistor with a resistor in its gate. Figure 5 shows

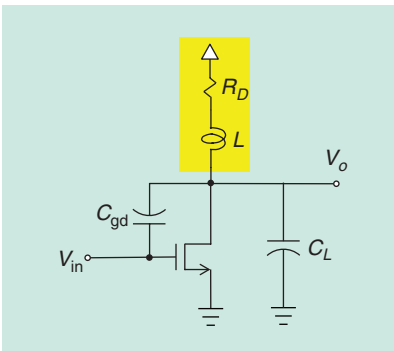


FIGURE 4: A common-source amplifier with added inductor in series with the load resistor (inductive peaking).

a differential design of an active inductor along with its equivalent half-circuit. We show intuitively that the equivalent circuit looking into the source is indeed an inductor in series with a resistor. For simplicity, we ignore all parasitic capacitances except for C_{gs} , and we ignore Body effect ($g_{me} = g_m$). At low frequencies, C_{gs} is open circuit, and we see $1/g_m \parallel r_o$ (see the first article in this series). At high frequencies, the capacitor becomes short, and hence we see $R \parallel r_o$. If we design the circuit such that $1/g_m < R$, then the impedance looking into the source increases with frequency, similar to an inductor in series with a resistor.

The reader can easily verify that the impedance looking into the source of the half circuit is given by

$$Z_{eq}/2 = (r_o \parallel \frac{1}{g_m}) \frac{1 + sRC_{gs}}{1 + s \frac{(r_o + R)C_{gs}}{1 + g_m r_o}}.$$

A magnitude plot of this impedance as a function of frequency is shown in Figure 5(c), where the impedance

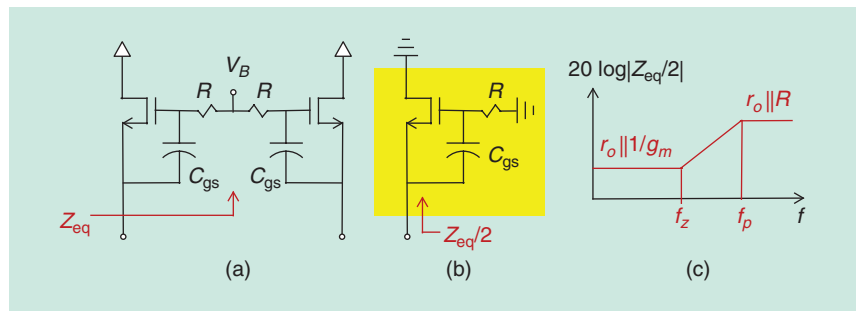


FIGURE 5: (a) A differential circuit implementing an active inductance, (b) a half-circuit equivalent, and (c) an equivalent impedance magnitude as a function of frequency.

behavior is that of a resistor in series with an inductor (up to the pole frequency f_p). If we assume $g_m r_o \gg 1$, for frequencies below f_p , the above impedance can be approximated by $Z_{eq}/2 \cong 1/g_m + sRC_{gs}/g_m$, which is a resistor ($1/g_m$) in series with an effective inductor $L_{eq} = RC_{gs}g_m$. To use this circuit in series with a resistor as in Figure 4, the position of the resistor and the inductor must be swapped so that one side of the inductor will be small-signal ground.

In summary, adding a negative capacitor in parallel to the load or

adding an inductor in series with the resistor in the drain terminal are two ways of extending the circuit bandwidth. In a future article, we will review the use of feedback as another method of extending the bandwidth.

References:

- [1] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004. For basic analysis of transistor circuits, refer to: A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. London, U.K.: Oxford Univ. Press, 2014. B. Razavi, *Fundamentals of Microelectronics*. Hoboken, NJ: Wiley, 2008.

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CHINA CONNECTION

(Continued from p. 7)

holds little attraction to private investors, with the goal of increasing China's share in IC manufacturing. The fund is innovative in that it is leveraging state capital to attract the market's internal forces and thus determine the best strategy for deployment of funds to accelerate the rise of China's IC industry in the global market.

However, Chinese companies have almost zero experience in the acquisition of international enterprises in the IC industry. Even in Silicon Valley, most acquisitions end up failing. Chinese enterprises should expect to "pay some

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tuition" in gaining experience and learn from their failures along the way. Nonetheless, over the next decade, the IC industry in China will likely grow via mergers and acquisitions and

gradually become the focus of attention of the global IC industry.

While capital can be funded through strong government support, what about talent and technology? These pose more daunting challenges because they take a long time to cultivate, nurture, and develop. As an old Chinese idiom says, success in anything requires the perfect combination of timing, place, and people. It appears that the success of China's IC industrial revolution will hinge on the third element—nurturing and training enough talented people.

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