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Source Degeneration

Welcome to "Circuit Intuitions"! This is the second article of a series that will appear regularly in this magazine. As the title suggests, each article provides insights and intuitions into circuit design and analysis. These articles are aimed at undergraduate students but may serve the interests of other readers as well. If you read this article, I would appreciate your comments and feedback as well as your requests and suggestions for future articles in this series. Please send your e-mails to ali@ece.utoronto.ca.

We said in the previous article that looking into a node, one can see the Thevenin or Norton equivalent circuit for that node. We now look deeper into one particular circuit that consists of an NMOS transistor with a resistor in series with its source terminal in a configuration known as *NMOS transistor with source degeneration*. We offer a simple method for the small-signal analysis and design of this configuration. The case for the PMOS transistor is similar but not discussed in this article for brevity.

Figure 1 shows a source-degenerated NMOS transistor along with equations for its Thevenin and Norton equivalents. These include the open-circuit voltage (v_{oc}), the short-circuit current (i_{sc}), and the equivalent resistor (R_{eq}). We make three observations regarding the role of the series resistance R_s in this configuration:

1) R_s has no effect on the open-circuit voltage (v_{oc}).
2) Including R_s increases the resistance looking into the drain.
3) Including R_s reduces the overall transconductance of the circuit (i.e., i_{sc}/v_{in}).

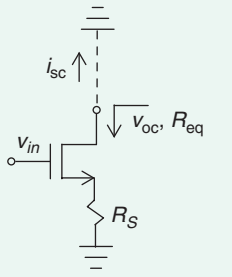
We now elaborate on these effects and capture them in a new equivalent transistor to be used in the analysis and design of other circuits containing this configuration.

To determine the open-circuit voltage (the Thevenin equivalent voltage) at the drain, we assume there is zero small-signal current flowing into the drain of the transistor, as shown in Figure 1. This zero current forces the voltage across R_s to be zero and, hence, renders R_s irrelevant to v_{gs} and v_{oc}.

The equivalent resistance looking into the drain is increased by $(1 + g_{me}R_s)$, where g_{me} is the effective g_m of the transistor (taking into account the transistor's body effect). This multiplying effect is the same effect that we explore in cascading transistors.

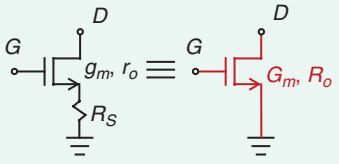
The short-circuit current is reduced by the same factor that increases the output resistance. This is simply because $i_{sc} = v_{oc}/R_{eq}$ and v_{oc} is independent of R_s.

Now let us combine these properties to construct an equivalent transistor for a source-degenerated NMOS transistor. Since the overall effect of including R_s is to have a higher output impedance (call it R_o) and a lower equivalent transconductance (call it G_m), we can capture these two properties in a new equivalent transistor with a new G_m and R_o, as shown in Figure 2. We can do this because a transistor in small signal is effectively a transconductance in parallel with a resistor. Note that by defining G_m and R_o according to the



$$v_{oc} = -g_m r_o v_{in}$$
$$R_{eq} = R_s + r_o + g_{me} r_o R_s$$
$$i_{sc} = \frac{v_{oc}}{R_{eq}} = -\frac{g_m r_o}{R_{eq}} v_{in}$$

FIGURE 1: A Norton/Thevenin equivalent circuit looking into the drain of an NMOS transistor with source degeneration.



$$G_M = -i_{sc}/v_{in} = g_m r_o / R_o$$
$$R_o = R_{eq} = R_s + r_o + g_{me} r_o R_s$$

$$G_m \approx \frac{g_m}{1 + g_{me} R_S} \quad \text{if } g_{me} r_o >> 1$$
$$\approx \frac{1}{R_S} \quad \text{if } g_{me} R_S >> 1$$

FIGURE 2: An NMOS transistor with source degeneration is equivalent to a single transistor with a smaller transconductance (G_m) and larger output impedance (R_o).

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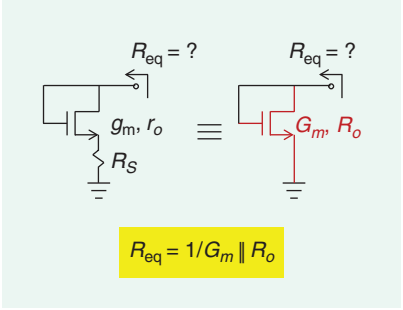

FIGURE 3: The equivalent resistance of a diode-connected NMOS with source degeneration.

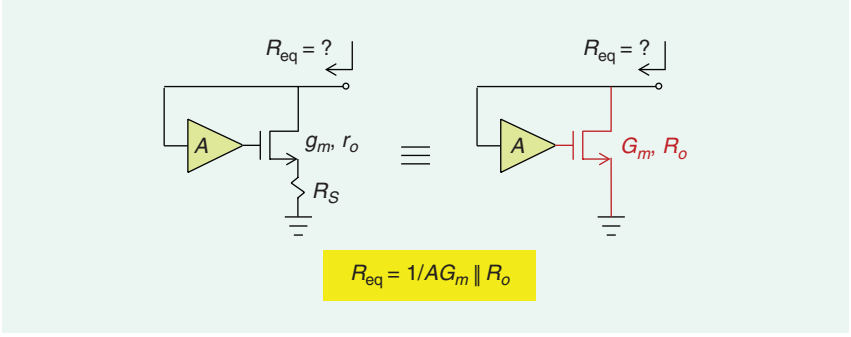

FIGURE 4: The equivalent resistance looking into the drain when a voltage gain amplifier, *A*, is inserted between the drain and the gate of a source-degenerated NMOS transistor.

equations presented in Figure 2, we have also guaranteed that v_{oc} of the equivalent transistor is independent of R_s. In other words, the new transistor has the same Thevenin and Norton equivalent circuits as those of the original source-degenerated NMOS transistor.

Before utilizing this equivalent transistor in the analysis and design of other circuits, let us entertain a few simplifying assumptions for further intuition. If we assume $g_{me} r_o \gg 1$ and $g_{me} R_s \gg 1$, then the equivalent G_m becomes $1/R_s$, independent of the transistor parameters. This outcome is significant because it shows how a constant transconductance can be produced despite variations and the unpredictability of transistor parameters. Note that even if the assumptions on $g_{me} r_o$ and $g_{me} R_s$ are not valid, the fact remains that the equivalent transconductance is less dependent on transistor parameters when R_s is included. Another consequence of including R_s is an increase in linearity of the circuit due to negative feedback. We will discuss this in detail in a future article.

Now let us use the equivalent transistor we just introduced to analyze a couple of sample circuits. In Figure 3, we attempt to find the equivalent resistance looking into the drain of a diode-connected NMOS transistor with source degeneration. This can be done by simply replacing the source-degenerated NMOS with the equivalent transistor. Now using Element #4, which was discussed in the previous article, one can quickly observe that the equivalent resistance is $1/G_m \| R_o$. Since both $1/G_m$ and R_o are higher (approximately by a factor of $g_{me} R_s$) compared to those of the original transistor, the equivalent resistance of this circuit is also higher by the same factor compared to a diode-connected NMOS transistor.

In other words, the new transistor has the same Thevenin and Norton equivalent circuits as those of the original source-degenerated NMOS transistor.

Figure 4 shows another common circuit in which a voltage gain A is inserted between the drain and the gate of a source-degenerated NMOS transistor. Again, we can find the equivalent resistance of this circuit by simply replacing the source-degenerated NMOS transistor with its equivalent transistor. The equivalent circuit is slightly different in this case than Element #4 of the previous article; nevertheless the equivalent resistance can be calculated easily. To this end, we apply a small-signal voltage source (v_x) to the output node and find the current it provides to the circuit. The voltage source can be replaced by two independent voltage sources: one that is applied only to the drain of the transistor and one that is applied only to the input of the amplifier, producing Av_x at the gate of the transistor. Now, we use superposition to find the current. We first zero the voltage source feeding the drain and then zero the voltage source feeding the gate of the transistor (one at a time), finding the drain current each time. By superposition, the total current drawn from v_x is the sum of $G_m A v_x$ and v_x/R_o. Therefore, the equivalent resistance is $1/AG_m \| R_o$.

In summary, including R_s in the source of an NMOS transistor effectively creates a new NMOS transistor with a transconductance (G_m) that is more robust to variation and an output resistance (R_o), which is much higher than r_o of the transistor.

References

For Thevenin and Norton equivalent circuits, refer to R. E. Thomas, et al., *The Analysis & Design of Linear Circuits*, 7th ed. New York: Wiley, 2012, pp. 109–122.

For small-signal analysis of transistor circuits, refer to A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 6th ed. London, U.K.: Oxford Univ. Press, 2010.

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