

Brett Grady

✉ bgrady@ece.utoronto.ca
🌐 [linkedin.com/in/brett-grady](https://www.linkedin.com/in/brett-grady)

SKILLS

Languages:

C, C++, Python, Perl,
Haskell, Verilog, VHDL

Tools:

Git, gdb, make,
bash/csh/zsh,
Altera/Intel Quartus,
Cadence Encounter,
Synopsys Design Compiler

OS:

Linux/Unix

EDUCATION

University of Toronto

Department of Electrical Computer
Engineering
MAsc in Computer Engineering
Exp. Grad. January 2019
Cum. GPA: 4.0

Ryerson University

Department of Electrical and
Computer Engineering
BEng in Computer Science
Grad. May 2017
Cum. GPA: 3.88

COURSEWORK

EDA
Parallel Programming
Data Structures & Algorithms
Computer Hardware
Computer Architecture
Digital Design

AWARDS

Ontario Graduate Scholarship
(OGS)

11.20.2018

EXPERIENCE

Intel Labs - Microarchitecture Research Lab

Research Scientist Intern

Jun 4 – present
Santa Clara, California

- Investigated architecture and applications for next generation domain-specific embedded FPGAs.
- Adapted existing internal EDA tooling for use with FPGA soft IP (bitstream generation, programmatic RTL generation).
- Performed in depth analysis of machine learning FPGA accelerator overlays to evaluate potential architecture changes.

Advanced Micro Devices (AMD)

Engineering Intern

May 2014 - Sep 2015
Markham, Canada

- Improved existing software testing infrastructure (Python, Perl) in conjunction with other teams. Wrote extensive documentation as part of an internal quality initiative.
- Handled build, QA and release of 3rd Party Standard Cell IP for the first generation of external standard cell IP at AMD.
- Performed various physical design tasks (e.g. characterization, technology migration, layout and schematic tweaks).

PROJECTS

Neural Network Accelerator Prototype

- Worked with industrial partner (Samsung) to prototype scalable neural network accelerator using FPGAs for proof-of-concept.
- Handled driver software, IP integration, hardware accelerator design, optimization, and verification.
- Paper published in IEEE-SOCC 2017.

FPGA-based High Frequency Trading Toolkit

- Developed an ultra low latency (<1us) subsystem for High Frequency Trading using Xilinx FPGAs. System handled networking, protocol decoding and order-book keeping of incoming market orders (bids/asks).
- Provided simplified hardware interface such that trading algorithms could be implemented more rapidly.
- Published in ReConFig 2017.

TEACHING EXPERIENCE

APS106 (Winter 2018) - Tutorial and Lab TA

Introduction to programming for freshman students (civil and mechanical engineering APS105 equivalent). Focused on key basic programming concepts (data structures, control flow, strings, numerical formats, iteration, recursion, etc).

RESPONSIBILITIES

- Supervise lab sessions
- Answer student questions regarding lab materials
- Formulate midterm questions with other TA's and professor
- Mark midterm papers

COURSE FEEDBACK

"Brett was very helpful. He answered questions about the labs on Piazza and also helped explain difficult topics, such as recursion or linked lists, in an easier way, during the tutorials."

"Knowledgeable, helpful."

"Awesome TA. Very helpful. Always willing to go that extra mile to help with understanding and applying the material."

"Very helpful and thoughtful, always willing to help the students understand the material"

CSC326 (Fall 2017) - Lab TA

Broad survey of modern programming paradigms including imperative, array, functional, and object-oriented programming. Course project had emphasis on practical web application development.

RESPONSIBILITIES

- Supervise lab sessions
- Answer students questions on lab, course project, and take home assignments
- Revise lab handouts for clarity and correctness
- Formulate marking rubrics with other TA's and professor
- Create midterm solution guide
- Mark lab assignments, midterm and final exam papers