A 112 Gb/s -8.2 dBm Sensitivity 4-PAM Linear TIA in 16nm CMOS with Co-Packaged Photodiodes

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Low-cost optical receivers (RX) operating at 100+ Gb/s 4-PAM with low power are in high demand to support 400GBASE-DR4/FR4 links in data centers. Existing pluggable solutions generally realize the RX front-end in BiCMOS. However, a more integrated solution, with the RX front-ends integrated onto a CMOS host IC and co-packaged alongside the photodiodes (PDs), offers the potential for smaller size, lower cost, and lower power [1, 2]. This work demonstrates a 112 Gb/s 4-PAM linear TIA in CMOS flip-chip co-packaged with commercial PDs and different PD-to-RX interconnect lengths (Fig. 1a).

The interconnect between PD and RX runs along the package substrate, and its design impacts the front-end bandwidth (BW). When written in terms of its specific inductance and capacitance, we see that increasing the interconnect's characteristic impedance ($Z_0 = \sqrt{(L/C)}$) makes it more inductive. This inductance appears between PD and RX capacitances and can perform series peaking. An optimized Z_0 is obtained by selecting the appropriate interconnect width. We did so for two different PD-to-RX interconnect lengths, as shown in Fig. 1b. Optimal Z_0 of 75 Ω and 50 Ω were achieved for 250 µm and 500 µm long interconnects, respectively resulting in similar BWs of approximately 60 GHz from the optical input to the PD to the TIA input in simulation (Fig. 1b).

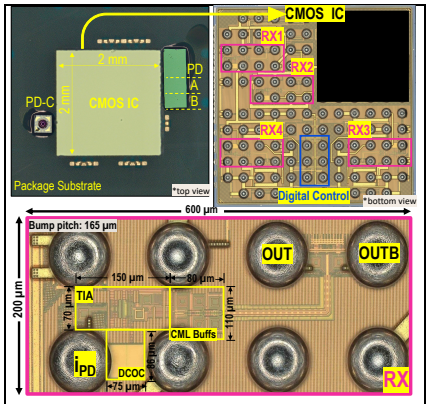
The proposed single-ended inverter-based TIA is shown in Fig. 2. A T-coil between the pad (100 fF) and TIA input with the center-tap connected to the ESD diode (80 fF) extends the BW. The TIA 1st stage is a shunt-feedback inverter providing 48 dBΩ of gain with 10 GHz of BW. Designing the 1st stage for a modest BW, 1/3 the overall TIA BW, allows for higher shunt resistor (Rf1) resulting in higher gain and lower input-referred current noise than a design with its full BW in the first TIA stage [3]. Subsequent equalizer stages restore the front-end to its targeted BW. The 1st stage is followed by a CTLE comprising an inverter-based transconductor for low-frequency gain in parallel with a CR high-pass filtered inverter. The high-pass filter cutoff frequency, and hence CTLE peaking, are adjusted by programmable resistors (R_{e1}). The NMOS and PMOS transconductances are separately high-pass filtered to provide more programmability. A transimpedance stage (TIS) with shunt-feedback converts the CTLE transconductors' output current back to voltage. Overall, the 2nd stage provides a maximum of 4 dB boost around 25 GHz. The 3rd stage comprises a programmable inverter-based VGA in parallel with another CTLE similar to the one in the 2nd stage for further equalization. Finally, a large TIS with L1 in series and L2 in shunt-feedback provides further BW extension. The 3rd stage provides an additional 7 dB boost at 30 GHz.

The output node, DN, and the input node, DP, of the final TIS stage together form the TIA's pseudo-differential output. Deferring the single-ended to differential (S2D) conversion to the last stage allows for a lower power and lower noise single-ended TIA than a replica-based pseudo-differential TIA [4] or having S2D in the 1st stage [5]. Though not required in this work, a dedicated on-chip voltage regulator for the TIA can mitigate any additional supply noise [1, 2].

A 3-stage CML buffer with shunt-inductive peaking drives the TIA outputs for off-chip measurements while also reducing the common-mode content of the S2D pseudo-differential output signal. Overall, the CML buffers have 0 dB gain and 45 GHz 3dB-BW in simulations.

The RX prototype is fabricated in 16nm CMOS FinFET. Fig. 3 shows the electrical measurements of RX4 with TIA and CML buffers operating at 0.9 V and 1.2 V, respectively. They reveal a transimpedance gain of 63 dBΩ, BW of 32 GHz, dynamic range of 9 dB, and group delay variation of <±5 ps up to 32 GHz. Total harmonic distortion (THD) measurements show that up to 670 µApp of input PD current can be handled with 8% of THD. 1-dB compression point with maximum gain occurs at 320 μA_{PP}. Measured output voltage noise distribution reveals input-referred current noise density of 16.9 pA/√Hz.

As shown in the die micrograph figure, two commercial back-illuminated InP PD ICs were flip-attached onto the package substrate alongside the CMOS prototype TIAs. PD-C is a singlet with a responsivity of 0.7 A/W, whereas PD-A and PD-B are two from an array of four PDs with a responsivity of 0.6 A/W. The TIA (including ESD diode and T-coil) + DCOC blocks are seen to occupy 0.0165 mm² area.



Die micrograph.

A 112 Gb/s 4-PAM QPRBS13 pattern from an arbitrary waveform generator is amplified by a discrete driver and applied to a commercial Mach-Zehnder Modulator (MZM). A 1310nm laser source feeds the MZM through a single-mode fiber resulting in 4-PAM eyes with RLM >0.95 and outer ER >3 dB. Differential electrical outputs are observed through pads on top of the package.

Fig.4 (top) shows the individually measured 112 Gb/s 4-PAM differential output eye diagrams from RX[1:3] with -6.1 dBm OMA, each satisfying a minimum pre-FEC symbol error rate (SER) requirement of 4.8×10^{-4} without any on-scope equalization. Eye diagrams from RX1 and RX2, both having the same PD but with different package Z_0 optimized for their respective PD-to-RX interconnect lengths, achieved similar eye quality. PD-C (in RX3) with 14% higher responsivity than PD-A/B achieved slightly better eye-opening compared to RX1/2. At its maximum gain setting, the TIA consumes 47 mW while the CML buffers consume 30 mW of power.

RX1 (w/ PD-A) eye diagrams after on-scope 4-tap FFE and 4-tap FFE + 4-tap DFE equalization are shown in Fig. 4 (bottom) further improving the eye quality. Fig. 5a shows the SER across input OMA indicating a sensitivity of -8.2 dBm at 112 Gb/s 4-PAM without scope equalization on RX1. Note that the SER does not reduce when the OMA is increased above -3 dBm limited by nonlinearity. Measurements with a 72 Gb/s NRZ PRBS13 input are shown in Fig. 5b achieving bit error rate (BER) < 1×10^{-12} at -5.6 dBm without scope equalization. The BER further reduces to 1×10^{-16} with 4-tap FFE on-scope equalization as shown in Fig. 5b (bottom).

Fig. 6 shows a comparison with recent works in CMOS and a summary of the sensitivity measurements. Even with approximately 40% lower PD responsivity and higher PD+ESD capacitance, this work offers the highest data rate and best sensitivity at the same data rates compared with [1] and [2]. This work offers a data rate similar to [6], but with optical measurements (instead of only electrical) and with lower noise and power. Compared to [4], this work offers 56 Gb/s (5.7% higher) NRZ data rate with 5.7 dB better sensitivity at the cost of 26% higher power consumption. In summary, this proposed linear TIA co-packaged with commercial PDs and an optimized PD-to-RX interface demonstrates the potential for more integrated future 100+ Gb/s optical receivers.

References:

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[4] L. Szilagyi *et al.*,"A 53-Gbit/s Optical Receiver Frontend With 0.65 pJ/bit in 28-nm Bulk-CMOS," JSSC, March. 2019.

[5] A. Cevrero et al.,"A 64Gb/s 1.4pJ/b NRZ optical-receiver data-path in 14nm CMOS FinFET," ISSCC, Feb. 2017.

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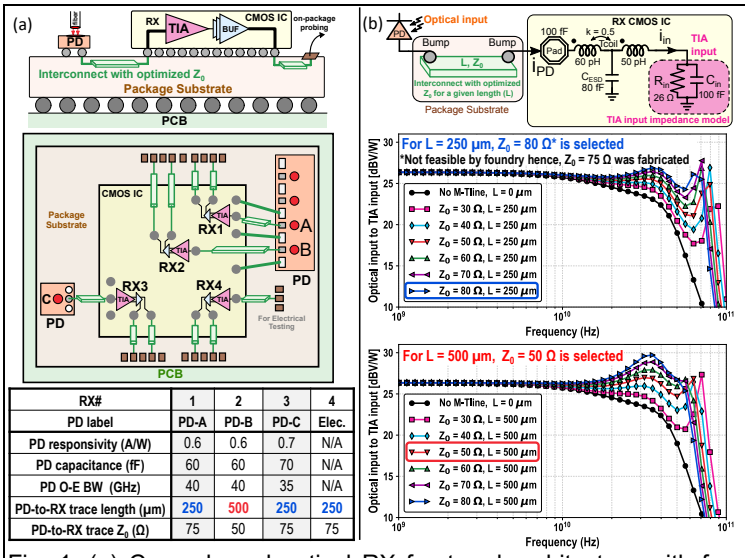

RX#	1	2	3	4
PD label	PD-A	PD-B	PD-C	Elec.
PD responsivity (A/W)	0.6	0.6	0.7	N/A
PD capacitance (fF)	60	60	70	N/A
PD O-E BW (GHz)	40	40	35	N/A
PD-to-RX trace length (μm)	250	500	250	250
PD-to-RX trace Z_0 (Ω)	75	50	75	75

Fig. 1. (a) Co-packaged optical RX front-end architecture with four identical TIAs exercised with various PDs and PD-to-RX interconnect lengths (b) Passive front-end optimization.

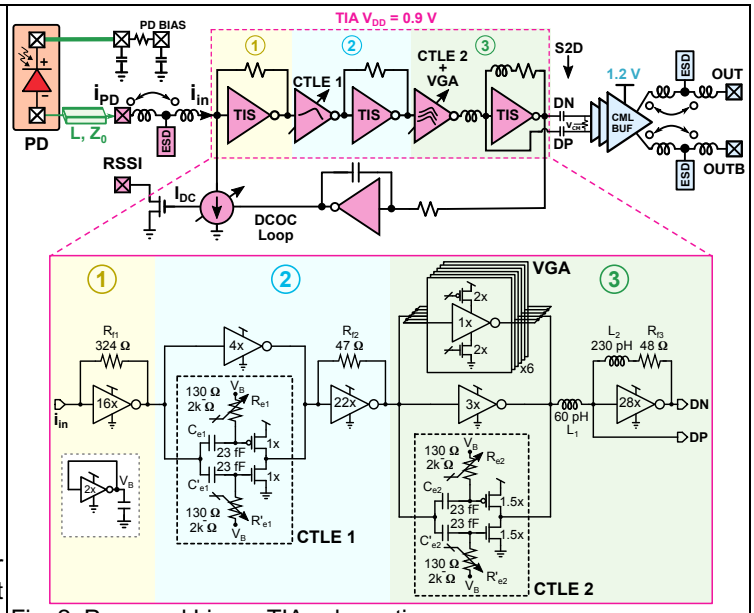

Fig. 2. Proposed Linear TIA schematic.

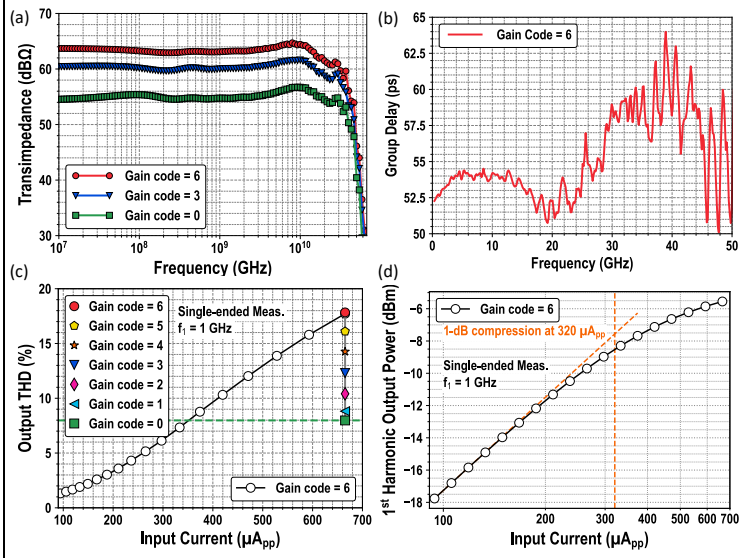

Fig. 3. Electrical measurements: (a) transimpedance, (b) group delay, (c) output THD and (d) 1-dB compression point.

Fig. 4. 112 Gb/s 4-PAM RX differential output eye diagrams with -6.1 dBm input OMA.

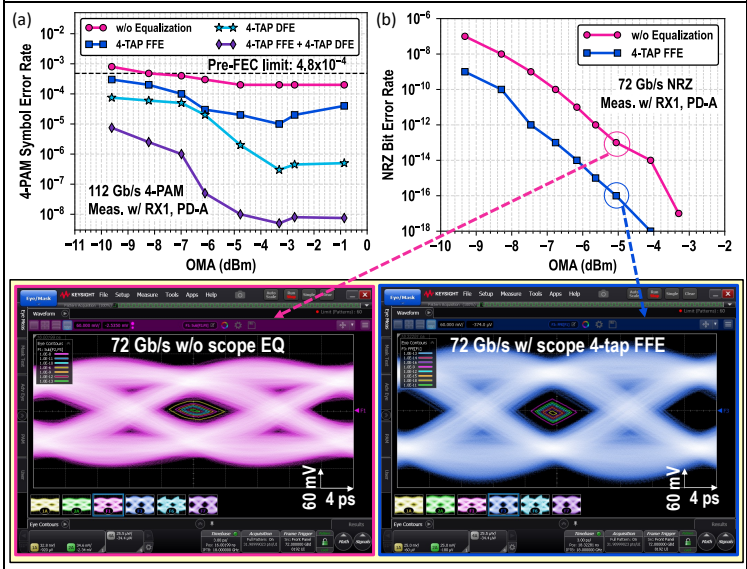

Fig. 5. (a) 112 Gb/s 4PAM SER (b) 72 Gb/s NRZ BER and differential output eye diagrams at -5.1 dBm OMA measured on RX1, PD-A.

	[4]	[6]	[2]	[1]	This Work
CMOS technology	28nm Bulk	28nm Bulk	16nm FinFET	28nm Bulk	16nm FinFET
Supply (V)	1.2	1.2, 2.5 (Vreg.)	1.8 (Vreg.)	1.5 (Vreg.)	0.9
Datarate (Gb/s)	53	112	106.25	100	112
Signaling	NRZ	4-PAM	4-PAM	4-PAM	4-PAM
TIA gain (dBΩ)	74	65	78	66*	63
TIA 3dB-BW (GHz)	27	60	27	20*	32
Max 4-PAM output swing w/ 50 Ω term. ($mV_{p\text{-}p\ diff}$)	N/A	300	300	620	450
Input ref. noise (pA/√Hz)	14*	19.3	16.7	21.2*	16.9
TIA power (mW)	34.6	107**	60.8**	117**	47
Input ESD (Yes/No)	No	No	No	No	Yes (80 fF)
PD capacitance (fF)	80	N/A (Electrical measurements only)	10	70	60
PD responsivity (A/W)	0.55		0.96	1	0.6
NRZ sensitivity at < $1x10^{-12}$ BER (dBm)	–6 dBm @53 Gb/s w/o scope eq.		N/A	N/A	–11.7 @56 Gb/s –5.6 @72 Gb/s w/o scope eq.
4-PAM sensitivity at < $4.8x10^{-4}$ SER (dBm)	N/A		–11 dBm @106.25 Gb/s w/ 5-tap FFE scope eq.	–8.3 dBm @100Gb/s w/ 2-tap FFE + 2-tap DFE on-chip eq.	–15 @100 Gb/s < –12.3 @106.25 Gb/s < –9.6 @112 Gb/s w/ 4-tap FFE + 4-tap DFE scope eq.

*Simulated **w/ output buffers and voltage regulators (approx. 20 – 40% of power consumed in voltage regulation)

4-PAM sensitivity summary at pre-FEC SER limit of $4.8x10^{-4}$ (dBm)				
Datarate (Gb/s)	w/o EQ	4-tap FFE	4-tap DFE	4-tap FFE + 4-tap DFE
100	–12.5	–13.5	–14.5	–15
106.25	–10.6	<–12.3		
112	–8.2	< –9.6		

NRZ sensitivity summary at pre-FEC BER of $1x10^{-12}$ (dBm)		
Datarate (Gb/s)	w/o EQ	4-tap FFE
50	–13.9	< –15.1
56	–11.7	–12.7
64	–7.6	–10.4
72	–5.6	–7.5

Fig. 6. Comparison to prior works and performance summary.