Body Biased Sense Amplifier with Auto-Offset Mitigation for Low-Voltage SRAMs

Dhruv Patel, *Student Member, IEEE*, Adam Neale, *Member, IEEE*, Derek Wright, *Member, IEEE*, and Manoj Sachdev, *Fellow Member, IEEE*

***Abstract*—This paper proposes a Differential-Input Body Bias Sense Amplifier (DIBBSA) with an auto-offset mitigation feature suitable for low-voltage SRAMs where the differential bitline signals are applied to the sources as well as to the body of the critical sensing transistors. We simulated and fabricated the proposed DIBBSA architecture with various operational modes in 65-nm CMOS technology to analyze body biasing's effectiveness in mitigating the offset. The standard deviation of offset (σ_{OS}) was measured over 5120 SAs in 10 ICs. The iso-gate area reduction in σ_{OS} for the proposed DIBBSA-FL and DIBBSA-PD modes resulted in 68.1% and 61.9% compared to conventional Current Latch SA (CLSA) and 24.1% and 18.1% compared to Voltage Latch SA (VLSA) at 0.4 V supply and 25 ˚C, respectively. Carried out measurements on 512 SAs in an IC show the minimum required differential input voltage across the temperature range of 0 ˚C to 75 ˚C at 0.4 V is achieved to be 48% lower compared to CLSA and 28% lower compared to VLSA by both the DIBBSA-FL and DIBBSA-PD modes.**

***Index Terms*— Offset Cancellation, Static Random Access Memory (SRAM), Dynamic Body Biasing, Threshold Voltage Mismatch, Comparator, Variation Tolerant Circuits, Latch.**

I. Introduction

Applications with stringent energy constraints such as health monitoring, Internet of Things (IoT), bio-implantable, wearable, and many other battery-operated devices are the impetus for low-energy, low-voltage, and reliable System on Chips (SoCs). Such SoCs are primarily occupied by the Static Random Access Memory (SRAM) used for cache data storage [1]. Therefore, SRAM is a critical block that determines the performance, yield and reliability of SoCs. A Sense Amplifier (SA) is a critical SRAM circuit responsible for faithfully amplifying and digitizing the data signal sensed from the SRAM cell [2]. The key SRAM performance metrics, such as minimum supply voltage, minimum read access time, and power consumption, significantly rely on the SA's performance [3, 4]. Several key characteristics of SA, such as minimum differential input voltage (ΔV_{BL-min}), power consumption, and sensing delay, are the most important [5].

Nanoscale CMOS technologies' aggressive downscaling poses a significant design challenge for reliable low-voltage operation due to increased random mismatch variations and leakage [6-10]. The SA design's primary challenge is to make the correct decisions with the smallest possible ΔV_{BL-min} while tolerating any adverse mismatch conditions. Minimizing ΔV_{BL-min} improves overall SRAM read sensing delay as it would take less time to discharge highly capacitive bit-lines; thus, this would also reduce energy consumption. The smallest possible ΔV_{BL-min} is mainly determined by the SA input offset, V_{OS} [3, 12-15]. The work from Abu Rahma et al. [16], implementing 16 Mb SRAM in 28 nm technology, highlighted that a single mV of increase in the standard deviation of SA offset distribution (σ_{OS}) requires 10 mV of additional bitline discharge to maintain the read yield threshold of 97%. Hence, the V_{OS} of the SA significantly affects the overall SRAM performance.

The overall V_{OS} of a SA is an aggregate of the mismatches in the threshold voltages (V_T), the drain currents, the gain factors, and the physical SA layout [8,17,18]. However, the V_T mismatch is the most significant factor determining the V_{OS} [19-24]. Strategies to compensate for SA's V_T mismatches fall into two categories: calibration techniques and offset compensation techniques. The simplest way to reduce V_{OS} is by increasing the size of devices [25]; however, the consequences are increased die area, bit-line loading, and power dissipation. One approach is to add additional devices to provide: a feedback mechanism to reduce the sensitivity to V_T mismatches [26-29]; or calibrate the offset, either dynamically [18, 24, 30-33] or with post-process trimming [34-37]. Another alternative is to use multistage timing, where the connections between the SAs are changed to reduce V_T mismatches [38-40]. While there are many potential solutions to the offset problem, they incur added costs in die area, power dissipation, or design complexity. Many researchers have exploited the body terminal to fine-tune circuit performance in CMOS technologies [41-53]. However, few researchers have used the body terminal to calibrate and mitigate the V_{OS} of SAs [54, 55], the cost being increased circuit area and required periodic recalibration to mitigate ageing effects on V_{OS}.

This paper builds on our previous work [56] and presents a Differential Input Body Biased Sense Amplifier (DIBBSA) that is suitable for low-voltage SRAMs, does not require calibration, and can compensate the V_{OS} dynamically. It is compatible with most symmetrical and fully-differential 6T, 8T, and 10T SRAM cells. The rest of the paper is organized as follows: Section II provides a detailed operation of the DIBBSA. Section III analyzes the offset tolerance and estimation. Section IV analyzes the sensing delay and power consumption. Section V analyzes the effectiveness of body bias across the supply voltage. Section VI and VII show the test chip implementation and

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Dhruv Patel was with the University of Waterloo and is now with the Electrical and Computer Engineering Department, University of Toronto, Toronto, ON M5S 3G4 (e-mail: dhruv.patel@isl.utoronto.ca).

Adam Neale was with the University of Waterloo and is now with Intel, Hillsboro, OR 97124, USA (e-mail: adam.neale@gmail.com).

Derek Wright, and Manoj Sachdev are with the Electrical and Computer Engineering Department, University of Waterloo, Waterloo, ON N2L 3G1. (e-mails: derek.wright@uwaterloo.ca, msachdev@uwaterloo.ca).

measurement results. Section VIII makes the comparison of the proposed DIBBSA with the state-of-the-art SAs. Finally, Section IX concludes the paper.

II. Differential Input Body Biased Sense Amplifier

A. Body Bias and Threshold Voltage Shift

Body biasing's role is that the source to body voltage (V_{SB}) of a transistor can manipulate V_T. The threshold voltage can be modeled by (1), where V_{T0} is the threshold voltage without body bias (i.e. $V_{SB} = 0$), γ is the body effect coefficient, and φ is the Fermi potential [57].

$$V_T = V_{T0} + \gamma\left(\sqrt{|(-2)\varphi_F + V_{SB}|} - \sqrt{|-2\varphi_F|}\right) \quad (1)$$

Fig. 1 shows the impact of applying a V_{SB} on the magnitude of a PMOS transistor's V_T, $|V_{TP}|$, in 65-nm CMOS. The forward body bias ($V_{SB} > 0$) lowers, and the reverse body bias ($V_{SB} < 0$) raises the $|V_{TP}|$, respectively. Simulations of a saturated PMOS transistor at 0.4 V and 1.0 V show, for example, that changing the V_{SB} from –40 mV to +40 mV lowers $|V_{TP}|$ by 8 mV and 10 mV, respectively. A judicious application of body bias can partially offset the impact of V_T mismatches in the SA, which is critical in reducing ΔV_{BL-min} [18, 54, 56]. The proposed DIBBSA exploits this technique to dynamically alter the V_T of critical sensing transistors to reduce V_{OS}.

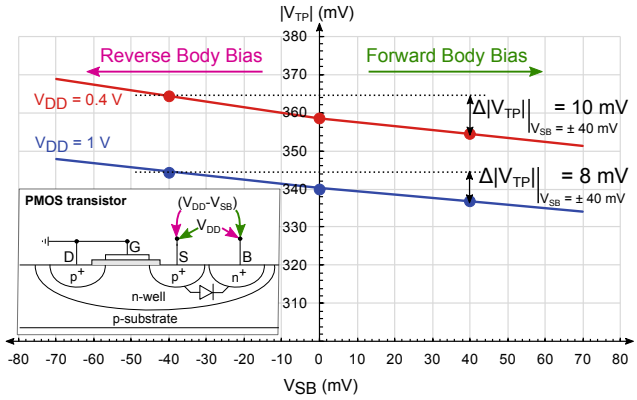

Fig. 1. Impact of body bias on the V_T of the PMOS device in a saturation region. Simulations performed at V_{DD} = 0.4 V and 1.0 V with a V_{SB} resolution of 1 mV.

B. DIBBSA Design and Operation

Fig. 2 (a) and (b) shows the schematic of the proposed DIBBSA-FL (7T) and DIBBSA-PD (9T) modes. The only difference between the DIBBSA-FL and DIBBSA-PD is that the latter has additional N3/N4 transistors to predischarge (PD) output nodes, whereas the former only equalizes the output nodes with N5 leaving the outputs float (FL) before the sensing phase. We describe the DIBBSA operation for the DIBBSA-PD mode that enables both body bias and predischarge.

The transistors P1/P2 are connected to the bitlines, BL/BLB while their bodies are connected to BLB/BL, respectively. Transistors N1/N2, together with P1/P2, complete the latching element. Transistors P3/P4 act as switches and provide operational control of the DIBBSA-PD. Arguably, P3/P4 can be merged with the column select signal (Y_{mux}) of the SRAM architecture; however, in this arrangement, it provides an additional benefit as their respective sources and body terminals receive BL/BLB inputs. The N5 transistor equalizes the OUT/OUTB before the sensing phase.

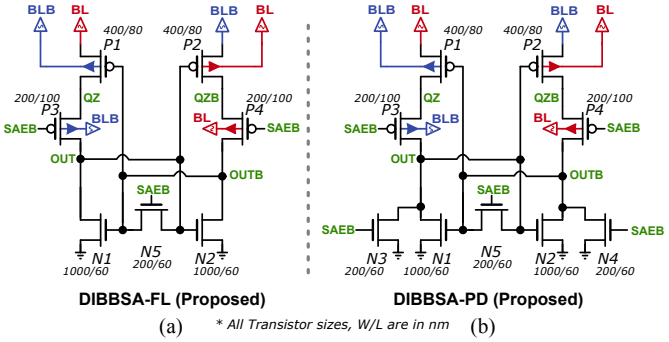

Fig. 2. Schematic of the proposed (a) DIBBSA with floating output nodes (DIBBSA-FL) and (b) DIBBSA with predischarge output nodes (DIBBSA-PD).

The operation of DIBBSA-PD is as follows. Initially, the SAEB signal is high, which disconnects P3 and P4 and turns-on N3/N4/N5 to equalize outputs, discharging OUT/OUTB to GND. The sensing operation starts once an adequate ΔV_{BL} signal is developed. Assuming that $V_{BL} = V_{DD}$ while $V_{BLB} = V_{DD} - \Delta V_{BL}$, then P1 is forward body biased by ΔV_{BL} while P2 is reverse body biased by the same voltage. Subsequently, SAEB transitions to '0', activating the DIBBSA-PD and making P3 and P4 similarly forward and reverse body biased, respectively. P1/P3 being forward body biased provides a relatively lower resistance to the OUT node, while P2/P3 being reversed body biased provides a relatively higher resistance to the OUTB node. This arrangement creates a current race scheme where OUT starts to charge up faster than OUTB, amplifying their voltage difference. At some point, with N1/N2 transistors conducting, the regenerative feedback kicks in, converging OUT to V_{DD} and OUTB to GND.

Fig. 3 (a) shows the implemented DIBBSA architecture in a 65-nm GP CMOS with four different operational modes including its non-body biased Differential Input SA (DISA) modes, DISA-FL/PD selectable with SEL[0:1] control signals. The layout of the proposed DIBBSA-PD without test mode devices (i.e. multiplexers and switches) is shown in Fig. 3 (b). The DIBBSA-FL layout removes N3/N4 devices, further reducing the area. The post-layout parasitic capacitance on each n-well is extracted to be 0.6 fF, two to three orders of magnitude smaller than the typical SRAM bitline capacitance range. These modes are listed in Table I. The effectiveness of dynamic body bias is independently controlled and characterized using the mode selection feature. Comparing the differences in performance between modes per-cell helps isolate the differences due to body biasing by avoiding discrepancies between cells, such as process variations and node capacitances.

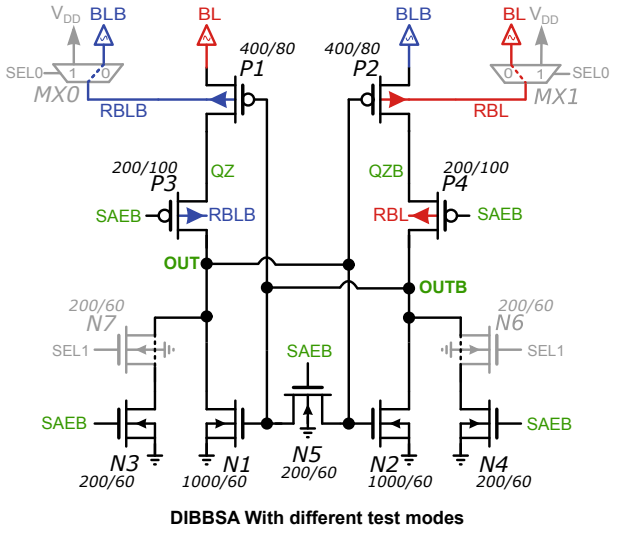

Fig. 3. (a) On-chip implemented proposed DIBBSA with different operational test modes for characterization purposes. (b) DIBBSA-PD layout (stripped without test mode selection switches).

TABLE I
BODY BIAS SAS WITH OPERATIONAL TEST MODES FOR CHARACTERIZATION

SEL1	SEL0	Mode Name	Mode Description
0	0	DIBBSA-FL (proposed mode)	Signals (BL/BLB) to Body, Outputs equalized but not pre-discharged to GND
0	1	DISA-FL	V_{DD} to Body, Outputs equalized but not pre-discharged to GND
1	0	DIBBSA-PD (proposed mode)	Signals (BL/BLB) to Body, Outputs equalized and pre-discharged to GND
1	1	DISA-PD	V_{DD} to Body, Outputs equalized and pre-discharged to GND

Fig. 4 (a) and (b) shows the conventional CLSA and VLSA, respectively, which are also simulated and fabricated alongside the DIBBSA architecture on the same chip for comparison.

Fig. 5 compares the DIBBSA and conventional architectures with transistor gate area and layout area normalized to the respective area of the VLSA. The layout area for the DIBBSA-FL/PD includes the area required to provide the n-well contacts. The proposed DIBBSA-FL and DIBBSA-PD result in a 14% and 1.5% reduction in layout area and 23.4% and 15.6% reduction in total transistor gate area than the VLSA.

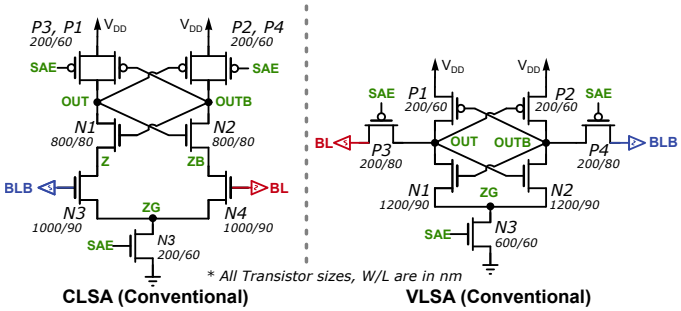

Fig. 4. On-chip fabricated conventional (a) CLSA and (b) VLSA.

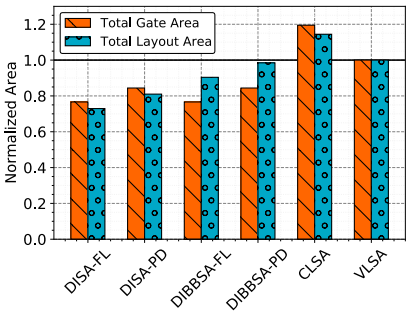

Fig. 5. SA comparison of relative gate and layout area in 65-nm CMOS.

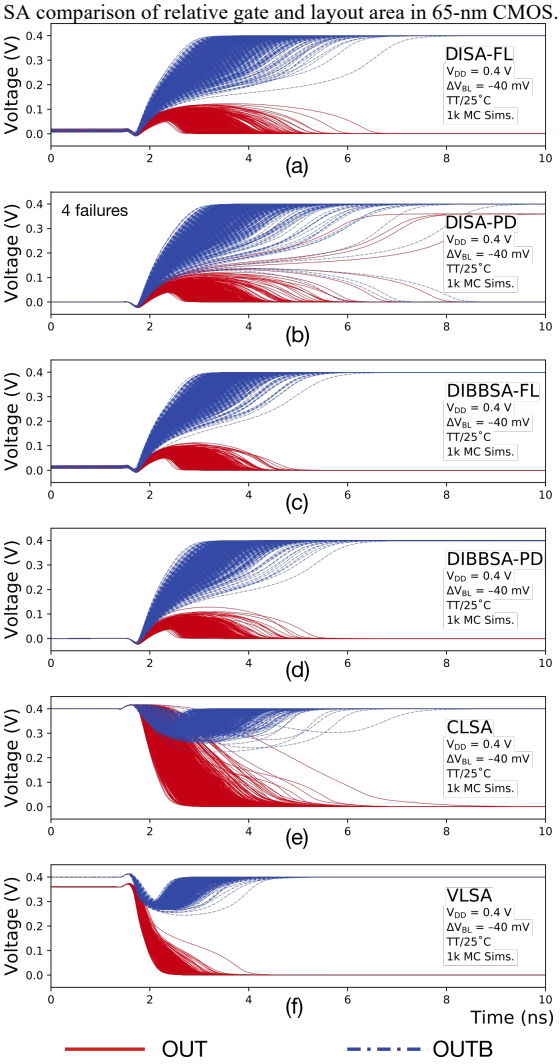

Fig. 6. 1000 Monte-Carlo transient simulation of decision-making OUT/OUTB signals of SAs (a) DISA-FL (b) DISA-PD (c) DIBBSA-FL (d) DIBBSA-PD (e) CLSA (f) VLSA at V_{DD} = 0.4 V, ΔV_{BL} = −40 mV and TT/25 °C.

1k Monte-Carlo transient simulations of the DIBBSA modes, VLSA, and CLSA are performed at $V_{DD} = 0.4$ V, $\Delta V_{BL} = -40$ mV, and TT/25 ˚C as shown in Fig. 6. It reveals that at $V_{DD} = 0.4$ V, all SAs can make correct decisions under such operating conditions except DISA-PD.

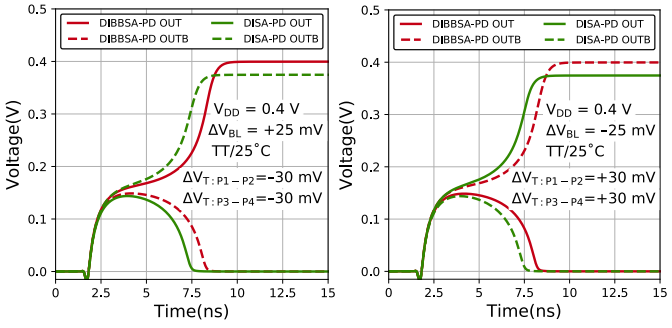

Fig. 7. Transient response of the DISA–PD and the proposed DIBBSA-PD at $V_{DD} = 0.4$ V and TT/25 ˚C with (a) $\Delta V_{BL} = +25$ mV, $\Delta V_{T:P1-P2} = -30$ mV and $\Delta V_{T:P3-P4} = -30$ mV. (b) $\Delta V_{BL} = -25$ mV, $\Delta V_{T:P1-P2} = +30$ mV and $\Delta V_{T:P3-P4} = +30$ mV.

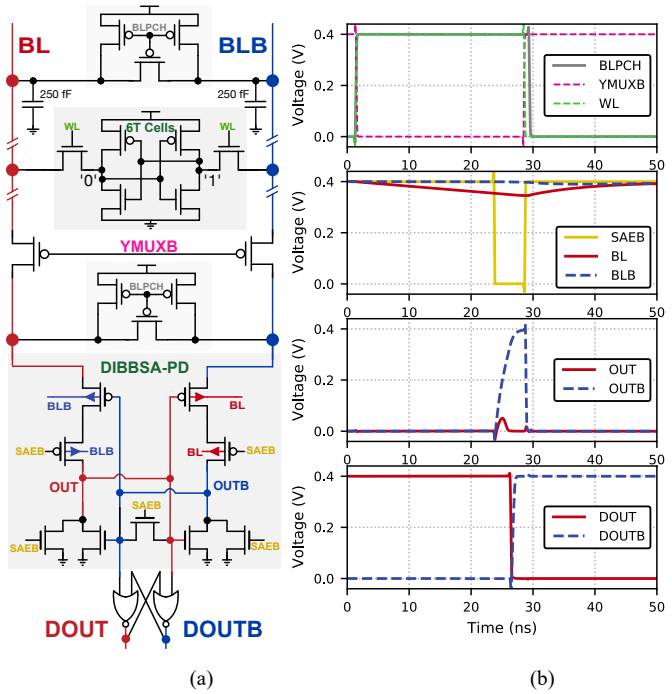

Fig. 8. (a) Design concept and (b) the corresponding signals of the proposed DIBBSA-PD realized with symmetric and fully differential 6T SRAM cells and peripheral circuits in 65-nm CMOS technology at $V_{DD} = 0.4$ V and TT/25 ˚C.

To distinguish between the DISA and DIBBSA modes, transient simulations are performed with adversely forced V_T mismatches in the critical sensing transistor pairs P1/P2 (i.e. $V_{TP1} - V_{TP2} = \Delta V_{T:P1-P2}$) and P3/P4 (i.e. $V_{TP3} - V_{TP4} = \Delta V_{T:P3-P4}$). For simplicity, the non-critical N1-N5 transistors are kept perfectly matched and are initially either predischarged or equalized close to GND, leaving them off during the critical amplification phase. The $\Delta V_{T:P1-P2}$ and $\Delta V_{T:P3-P4}$ mismatches are explicitly enforced in the undesirable direction by parametrizing the V_{TP} of the PMOS transistor in the model file. For example, to enforce the $\Delta V_{T:P1-P2}$ of 30 mV, the V_{TP} of P1 and P2 would be set as $|V_{TP1}| = |V_{TP0}| + 15$ mV and $|V_{TP2}| = |V_{TP0}| - 15$ mV, where $|V_{TP0}|$ is the magnitude of the nominal V_T of the PMOS transistor given by the foundry model. Fig. 7 (a) shows the transient simulation comparison between DIBBSA-PD and DISA-PD modes with $\Delta V_{BL} = -25$ mV and $\Delta V_{T:P1-P2} = V_{T:P3-P4} = +30$ mV at $V_{DD} = 0.4$ V and TT/25 ˚C. Fig. 7 (b) illustrates a complementary situation with the polarity of the mismatch and ΔV_{BL} changed. In both Fig. 7 (a) and (b), under such adverse mismatch conditions, DIBBSA-PD with dynamic body biasing makes correct decisions, whereas DISA-PD makes incorrect decisions. Note that the DISA-PD logic '1' resolves at the $V_{DD} - \Delta V_{BL}$ instead of V_{DD} when it makes an incorrect decision as the BL/BLB are supplied to the PMOS transistors' source.

The design concept of the proposed DIBBSA in symmetrical and fully diffeerential SRAM cells is similar to that of the conveontional SAs. For example, Fig. 8(a) shows the utilization of the DIBBSA-PD with the conventional 6T SRAM cells along with the cooresponding transient signals shown in Fig. 8(b) at $V_{DD} = 0.4$ V and TT/25 ˚C.

III. Offset Tolerance and Estimation

To highlight the body bias impact alone on the V_T shift and how its judicial application in the proposed DIBBSA helps to mitigate the offset related to V_T mismatch, the total V_T mismatch (V_{TP-mis}) of the critical sensing transistors, P1/P2 and P3/P4 defined by (2) is analyzed.

$$V_{TP-mis} = |\Delta V_{T:P1-P2}| + |\Delta V_{T:P3-P4}| \quad (2)$$

Fig. 9 shows the distribution of V_{TP-mis}, extracted by evaluating the V_T of P1/P2 and P3/P4 from the 5120 Monte-Carlo DC simulations. The simulations are performed with $V_{DD} = 0.4$ V and in the presence of three different ΔV_{BL} conditions on the DIBBSA state just before the SAEB is about to make a 1→0 transition (i.e. SAEB $= V_{DD}$). The black graph illustrates the V_{TP-mis} distribution with no bitline signal (i.e. $V_{BL} = V_{BLB} = V_{DD}$ giving $\Delta V_{BL} = 0$ mV). This distribution of V_{TP-mis} at $\Delta V_{BL} = 0$ mV can be defined as an intrinsic V_T mismatch where the distribution is approximately centred at 0 V, as expected.

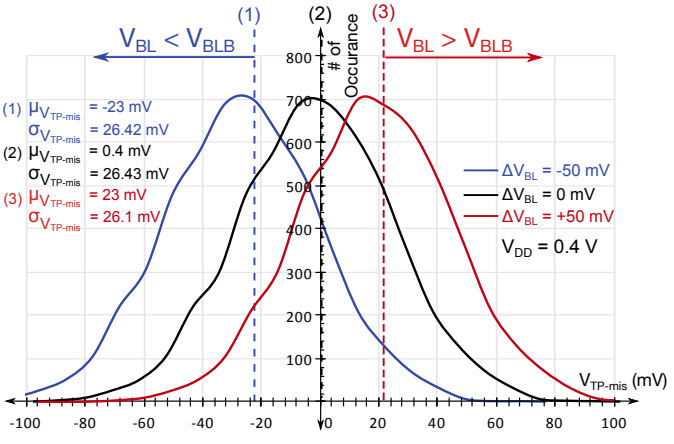

Fig. 9. Distribution of 5120 Monte-Carlo simulations evaluating the V_{TP-mis} of DIBBSA with $\Delta V_{BL} = -50$ mV, 0 mV and +50 mV at $V_{DD} = 0.4$ V. It shows the V_{TP-mis} distribution shifts towards the correct direction as $|\Delta V_{BL}|$ is applied.

The red graph depicts when V_{BL} is 400 mV and V_{BLB} is 350 mV, resulting in $\Delta V_{BL} = +50$ mV. In this case, P1/P3 are forward body biased, and P2/P4 are reverse body biased, all by 50 mV. The mean ($\mu_{V_{TP-mis}}$) and standard deviation ($\sigma_{V_{TP-mis}}$) of the red curve are +23 mV and 26.1 mV, respectively. Importantly, this positive shift of the V_{TP-mis} distribution for $V_{BL} > V_{BLB}$ indicates a lower V_T for P1/P3 and higher V_T for P2/P4 compared to the black graph when $\Delta V_{BL} = 0$ mV (i.e. no bitline signals applied to body). Hence, P1/P3 have become stronger, and P2/P4 have become weaker than the $\Delta V_{BL} = 0$ mV case. This further amplifies the voltage difference between OUT and OUTB in the correct direction of the expected digital output. The blue graph shows the complementary case. Hence, the auto-offset mitigation feature is achieved.

Several researchers have carried out offset estimation and offset model development for different types of SAs. Singh and Bhat [22] developed an analytical model for a VLSA. The intrinsic offset of the SA is mostly due to the V_T mismatch between the pair of NMOS latching transistors, while the extrinsic offset is caused by the V_T mismatch between the PMOS pass transistors. Woo et al. derived a complex offset model for CLSA and VLSA latching that considers secondary transistor effects [23]. In this work, we focus on factors that most significantly impact the V_{OS}, namely the transistors' V_T mismatches. Equation (3) models the contribution of the V_T mismatches within the transistor pairs P1/P2, P3/P4, and N1/N2 on the overall offset voltage of the DIBBSA due to V_T mismatches, V_{OS-T}.

$$V_{OS-T} = \boldsymbol{\alpha}|\Delta V_{T:P1-P2}| + \boldsymbol{\beta}|\Delta V_{T:P3-P4}| + \boldsymbol{\gamma}|\Delta V_{T:N1-N2}| \quad (3)$$

$\Delta V_{T:P1-P2}$, $\Delta V_{T:P3-P4}$, and $\Delta V_{T:N1-N2}$ are the V_T mismatches within the P1/P2, P3/P4, and N1/N2 pairs, respectively. The α, β, and γ are coefficients that determine the contribution of $\Delta V_{T:P1-P2}$, $\Delta V_{T:P3-P4}$, and $\Delta V_{T:P3-P4}$, respectively, to the overall V_{OS-T} of the DIBBSA.

Simulations in Fig. 10 (a) show the amount of $\Delta V_{T:P1-P2}$ mismatch in an undesirable direction that can be applied before making a wrong decision for a given ΔV_{BL}. The remaining SA transistors are kept perfectly matched to isolate the effect of P1/P2 mismatch. Simulations are performed at $V_{DD} = 0.4$ V and the TT/25 °C corner. To derive the offset coefficient, α associated with the $\Delta V_{T:P1-P2}$ mismatch, the inverse slopes of the mismatch tolerance plots from Fig. 10(a) are calculated and shown in Fig. 10 (b). Similar offset tolerance simulations and offset coefficient extraction are performend for P3/P4 and N1/N2 pairs as shown in Fig. 10 (c)-(f).

A few conclusions can be drawn from the offset tolerance analysis. N1/N2 are not a significant design target because they can tolerate a much higher mismatch. On the other hand, P1/P2 are the most critical as they are the least tolerable of mismatch, followed by P3/P4. TABLE II summarizes the resulting average values of the α, β and γ coefficients from Fig. 10 (b) (d) and (f) in the units of mV V_{OS-T} per mV ΔV_T for each of the DIBBSA modes. Lower offset coefficient values indicate higher tolerance in a given transistor pair. DIBBSA-FL/PD have the lowest coefficient values when compared with DISA-FL/PD, indicating that body biasing is mitigating the overall voltage offset.

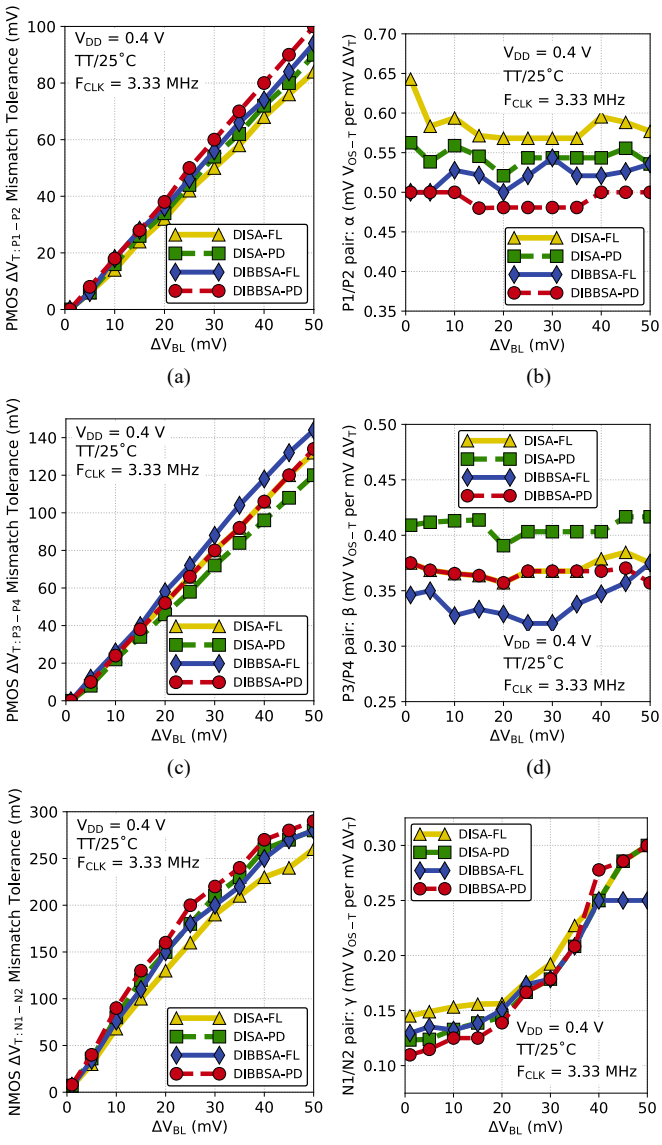

Fig. 10. Mismatch tolerance and derived offset factors of various modes of the proposed SA architecture across ΔV_{BL} at $V_{DD} = 0.4$ V, TT/25 °C and $F_{CLK} = 3.33$ MHz. (a) P1/P2: $\Delta V_{T:P1-P2}$, (b) α offset factor (c) P3/P4: $\Delta V_{T:P3-P4}$, (d) β offset factor, (e) N1/N2: $\Delta V_{T:N1-N2}$, and (f) γ offset factor

TABLE II
EXTRACTED OFFSET COEFFICIENTS FOR THE PREDICTION OF V_{OS-T} FOR OPERATIONAL TEST MODES OF THE DIBBSA ARCHITECTURE

Offset Coefficients (units of mV V_{OS-T} per mV ΔV_T)	α	β	γ
DISA-FL	0.584	0.370	0.199
DISA-PD	0.545	0.407	0.187
DIBBSA-FL	0.520	0.340	0.181
DIBBSA-PD	0.491	0.366	0.184

To further testify the benefit of dynamic body biasing, the mismatch offset tolerance analysis for critical P1/P2 and P3/P4 pairs is extended across various global corners at fixed $\Delta V_{BL} = 40$ mV and is shown in Fig. 11. It shows that across all global corners, DIBBSA-FL and DIBBSA-PD tolerates higher mismatch when compared to DISA-FL and DISA-PD, respectievly.

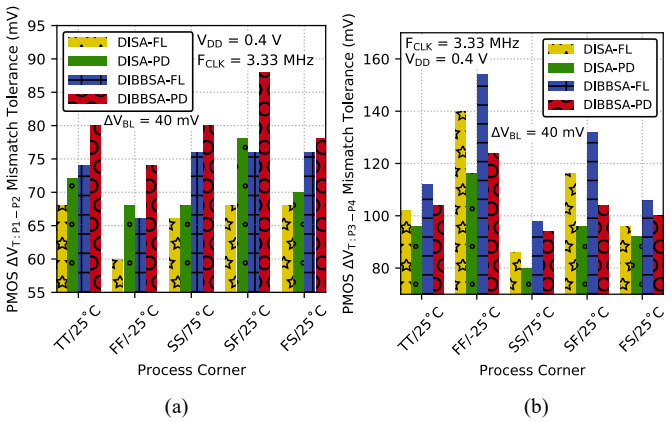

Fig. 11. Mismatch offset tolerance across various process corners for DIBBSA modes at V_{DD} = 0.4 V, ΔV_{BL} = 40 mV and F_{CLK} = 3.33 MHz.

A. *Offset tolerance across SAE pulse width*

The sensitivity of the critical transistor pair's mismatch tolerance to the SAEB pulse width (the sensing window) is analyzed. Fig. 12 (a) shows $\Delta V_{T:P1-P2}$ mismatch tolerance versus SAE pulse width, with ΔV_{BL} = 40 mV, V_{DD} = 0.4 V, and TT/25 °C. All transistors are noise enabled, and 5 mV_{rms} of white gaussian noise is superimposed on V_{DD}, SAEB, and BL/BLB to validate the offset tolerance more rigorously. Fig. 12 (b) shows a similar analysis for $\Delta V_{T:P3-P4}$ mismatch. Both Fig. 12 (a) and (b) show higher tolerance for the proposed DIBBSA-FL/PD modes than their corresponding non-body biasing DISA-FL/PD modes.

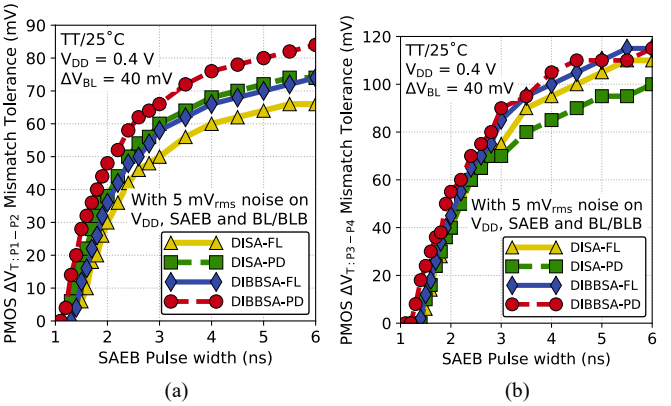

Fig. 12. (a) $\Delta V_{T:P1-P2}$, and (b) $\Delta V_{T:P3-P4}$ mismatch tolerance of various modes of the proposed SA architecture across SAEB pulse width at V_{DD} = 0.4 V, ΔV_{BL} = 40 mV, and TT/25 °C. Simulations are performed with 5 mV_{rms} noise superimposed on V_{DD}, SAEB, and BL/BLB, and transistor noise enabled.

IV. Sensing Delay and Power Analysis

A. *SA Sensing Delay Simulations*

The sensing delay is analyzed with each SA having the identical load and input driving conditions applied. The sensing delay is measured from the 50% rise of the SAEB to the 50% rise of the buffering inverter outputs following OUT/OUTB. Simulation results shown in Fig. 13 are performed by fixing ΔV_{BL} = −40 mV at TT/25 °C with the transistors being perfectly matched. Fig. 14 shows a snapshot of the sensing delay at V_{DD} = 0.4 V and highlights the proposed DIBBSA-FL/PD modes outperforming the DISA-FL/PD modes by about 10%. The conventional CLSA showed almost similar sensing delay compared to DIBBSA-FL/PD modes, and the conventional VLSA performed with 44% lower sensing delay than the proposed DIBBSA-FL/PD modes. Nevertheless, the sensing delay of an SA is a relatively small fraction of the overall SRAM read path delay. The majority of the overall delay primarily comes from discharging the highly capacitive bitlines dictated by the SA V_{OS} worst-case requirement, and hence, reducing the SA V_{OS} is most important [3, 58].

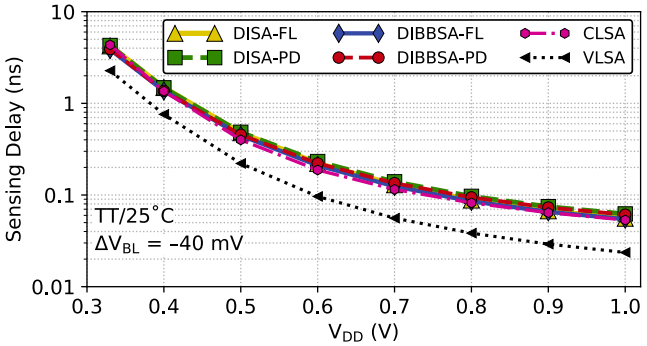

Fig. 13. Simulated sensing delay trend comparison of SAs across V_{DD} at ΔV_{BL} = −40 mV and TT/25 °C.

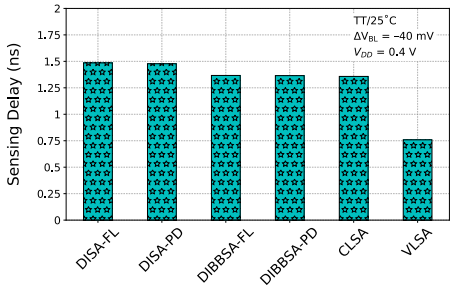

Fig. 14. Simulated sensing delay comparison of SAs at V_{DD} = 0.4 V, ΔV_{BL} = −40 mV and TT/25 °C.

B. *SA Power Consumption Simulations*

The power consumption of the SAs is also analyzed. The static power consumption of the SA ($P_{st\text{-}SA}$) in low-voltage, energy-limited applications is an essential metric for appropriate SA circuit selection since SRAMs predominately stay in an idle state. Fig. 15 shows the $P_{st\text{-}SA}$ comparison across V_{DD} and indicates that the VLSA has the highest $P_{st\text{-}SA}$, whereas DIBBSA-FL and DISA-FL have the lowest. The higher $P_{st\text{-}SA}$ of the VLSA is mainly from its relatively large devices, especially the higher W/L ratio of the footer SAE transistor, N3. Fig. 16 illustrates a snapshot of the $P_{st\text{-}SA}$ at V_{DD} = 0.4 V where the DIBBSA-FL and DIBBSA-PD consume 62% and 52% lower $P_{st\text{-}SA}$ than the VLSA, and 42% and 26% lower $P_{st\text{-}SA}$ than the CLSA, respectively.

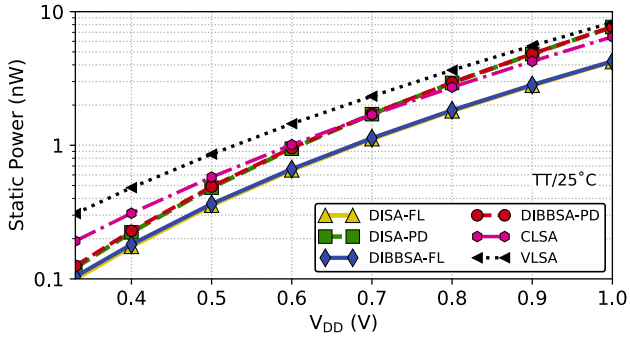

Fig. 15. Simulated static power consumption of SAs across V_{DD} at TT/25 °C.

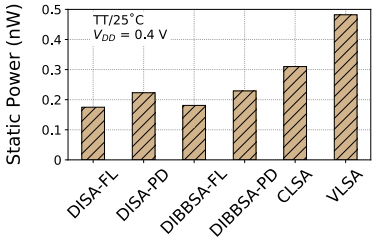

Fig. 16. Simulated static power consumption comparison of SAs at V_{DD} = 0.4 V and TT/25 ˚C.

The plot in Fig. 17 shows the total average power consumption (P_{AV-SA}) of the SAs across V_{DD} while fixing $\Delta V_{BL} = -40$ mV at $F_{CLK} = 3.33$ MHz and TT/25 ˚C. The trendlines indicate that the CLSA has the highest P_{AV-SA}, whereas both DIBBSA-FL and DISA-FL have the lowest. The snapshot and breakdown of the P_{AV-SA} at $V_{DD} = 0.4$ V are shown in Fig. 18. At 0.4 V supply, The DIBBSA-FL consumes 12% and 36% lower P_{AV-SA} compared to VLSA and CLSA, respectively. The proposed DIBBSA-PD consumes 0.7% and 30% lower P_{AV-SA} compared to VLSA and CLSA, respectively. The P_{AV-SA} breakdown is considered among SAEB loading, BL/BLB, and V_{DD} supply rail where applicable. As expected, the SAEB loading contribution is the least since it is only connected to the transistor gates, whereas the BL/BLB contribution is the most as they act as a supply for the SA via the sources of P1/P2.

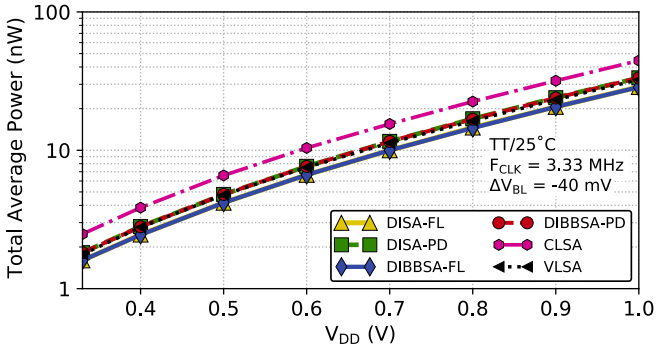

Fig. 17. Simulated total average power consumption trend comparison of SAs across V_{DD} at $\Delta V_{BL} = -40$ mV, $F_{CLK} = 3.33$ MHz and TT/25 ˚C.

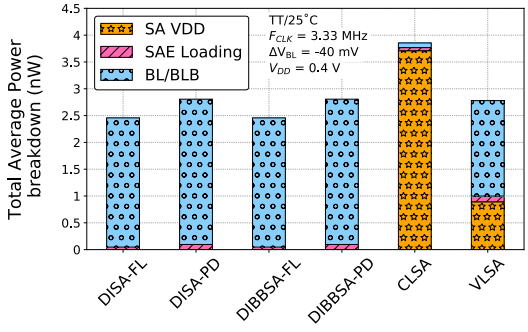

Fig. 18. Simulated total average power consumption breakdown comparison of SAs at V_{DD} = 0.4 V, $\Delta V_{BL} = -40$ mV, $F_{CLK} = 3.33$ MHz and TT/25 ˚C.

The SA dynamic power consumption, $P_{dy\text{-}SA}$, is derived at V_{DD} = 0.4 V, $F_{CLK} = 3.33$ MHz, and TT/25 ˚C by subtracting $P_{st\text{-}SA}$ from P_{AV-SA}, and is shown in Fig. 19 with a contribution breakdown. Compared to the VLSA, the total $P_{dy\text{-}SA}$ of the DIBBSA-FL is 2% lower, whereas the DIBBSA-PD is 12% higher. One may trade-off some sensing delay to reduce $P_{dy\text{-}SA}$ by altering the device sizes, but it must be done without impacting the offset voltage negatively. Nevertheless, the $P_{dy\text{-}SA}$ is a small fraction of the total dynamic read power ($P_{dy\text{-}read}$) of the SRAM read access, mainly due to discharging the highly capacitive bitlines [24, 33, 59, 60]. Ultimately, the offset reduction benefits of the DIBBSA reduce the overall $P_{dy\text{-}read}$, described in Section X.

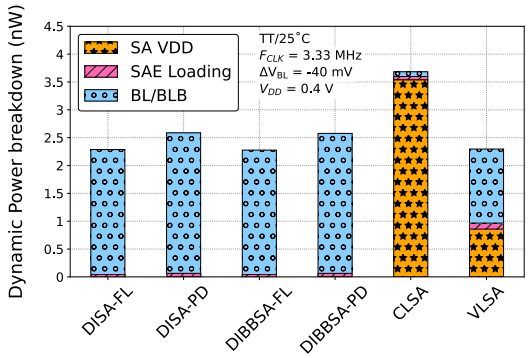

Fig. 19. Simulated dynamic power consumption breakdown of SAs at V_{DD} = 0.4 V, $\Delta V_{BL} = -40$ mV, $F_{CLK} = 3.33$ MHz and TT/25 ˚C.

V. Body Bias Effectiveness Across Supply

An appropriate supply voltage range for optimum sensing yield of the DIBBSA architecture is analyzed. It is determined by examining the differential drive strength of the current sensing branches at the critical sensing instant as a function of the supply voltage. The initial condition when the SAEB signal makes the 1 → 0 transition is critical in the SA outputs converging towards the correct trajectory and enabling the positive feedback mechanism. At this instant, OUT and OUTB are at GND; consequently, N1 and N2 are off and do not participate in setting the initial SA decision trajectory. Therefore, only transistors P1 through P4 responsible for this trajectory are shown in the equivalent circuits of Fig. 20 (a) and (b) for DISA-PD and DIBBSA-PD, respectively. The P3/P4 drains and P1/P2 gates are connected to GND since OUT and OUTB are predischarged at this instant. DC simulations are performed for these two equivalent circuits by sweeping V_{DD} while keeping $\Delta V_{BL} = +25$ mV and assuming perfectly matched devices. The transconductance model parameter of each transistor, g_m, is extracted. Finally, the differences are calculated to find the differential transconductance, $|\Delta g_m|$, which indicates the drive strengths for the P1/P2 and P3/P4 pairs. The $|\Delta g_m|$ trend is plotted on the left y-axis in Fig. 20 (c) as the key sensing strength indicator. The pink curve plotted on the right y-axis in Fig. 20 shows the $\frac{\Delta V_{BL}}{V_{DD}}$ ratio, indicating relative bitline signal strength.

The main takeaway from Fig. 20 (c) is that the maximum differential drive strength is achieved at around $V_{DD} = 0.5$ V for both the equivalent circuits of DIBBSA-PD and DISA-PD. This analysis suggests that these SAs should provide the best sensing yield at V_{DD} from 0.4 V to 0.7 V. Moreover, the $\frac{\Delta V_{BL}}{V_{DD}}$ ratio emphasizes that higher V_{DD} alone can lead to a higher g_m, but not necessarily to a higher $|\Delta g_m|$. Instead, the $\frac{\Delta V_{BL}}{V_{DD}}$ ratio must be increased for a higher $|\Delta g_m|$, which necessitates a higher ΔV_{BL}

and, therefore, higher power. Also, the P1/P2 pair's $|\Delta g_m|$ is lower than the P3/P4 pair's because P1/P2 are operating in the triode region, whereas P3/P4 are operating in the saturation region at that instant of interest. Lastly, owing to body biasing, the peak $|\Delta g_m|$ of the DIBBSA-PD is higher than the DISA-PD.

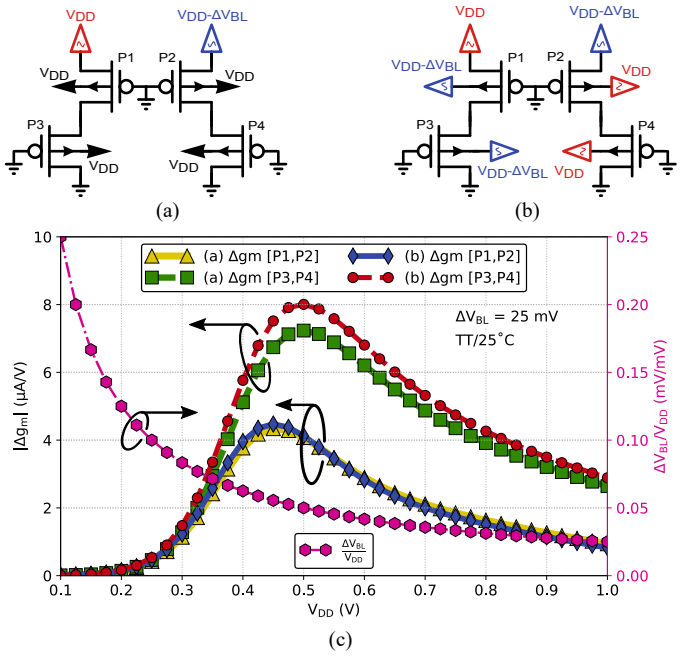

Fig. 20. (a) Equivalent circuit of DISA-PD (b) Equivalent circuit of DIBBSA-PD just when their SAEB signal makes the 1 → 0 transition. (c) The simulated magnitude of differential transconductance, $|\Delta g_m|$, of the transistor pair from (a) and (b) across V_{DD} is plotted on left y-axis. The pink curve plotted on the right y-axis shows $\frac{\Delta V_{BL}}{V_{DD}}$ ratio. Simulations are performed with $\Delta V_{BL} =$ 25 mV at TT/25 ˚C.

VI. Test Chip and Measurement Setup

Arrays of SAs are implemented on a 65-nm GP CMOS technology to measure the offset characteristics, similar to previous works [16, 21, 61]. A test chip with an SA array architecture shown in Fig. 21 is designed with 64 rows, each having 8 SAs of DIBBSA, VLSA and CLSA. Thus, a single test chip contains 512 SAs of each type that can be individually accessed with a row and a column decoder. Each row slice contains a common precharge and keeper circuit, a row selection driver, hold-path buffers, pull-down NMOS transistors, and a level shifter with a transparent latch. The BL/BLB signals are routed vertically throughout the array where ΔV_{BL} is achieved by setting appropriate voltages at the BL and BLB analog pads (e.g., $V_{BL} = V_{DD}$, $V_{BLB} = V_{DD} - \Delta V_{BL}$). All the address and control signals for the mode selection transistors operate under a fixed 1 V supply, whereas the rest of the circuitry, including SAs, operate under the desired V_{DD}. The fabricated test chip micrograph is shown in Fig. 22.

Fig. 23 (a) illustrates the test bench schematic, and Fig. 23 (b) shows the laboratory setup. CLK, ADDR and SEL signals are provided by the Tektronix DGA-200 data generator, and V_{DD}, BL, and BLB are provided by the benchtop precision power supplies. A Tektronix TLA-5101 logic analyzer captures DOUT. A temperature chamber controls the temperature of the test chip and the PCB.

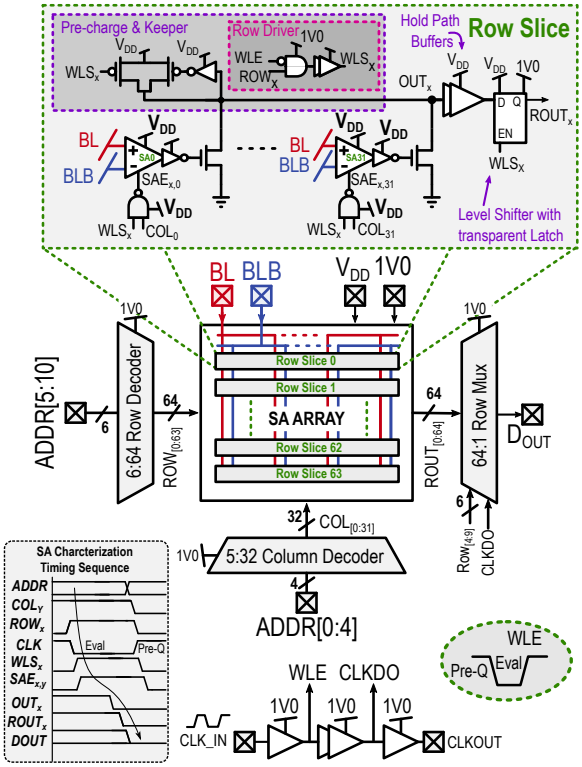

Fig. 21. Test chip architecture for characterizing SA offset.

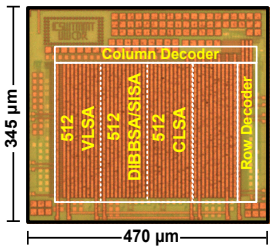

Fig. 22. Micrograph of the 65-nm GP CMOS test chip.

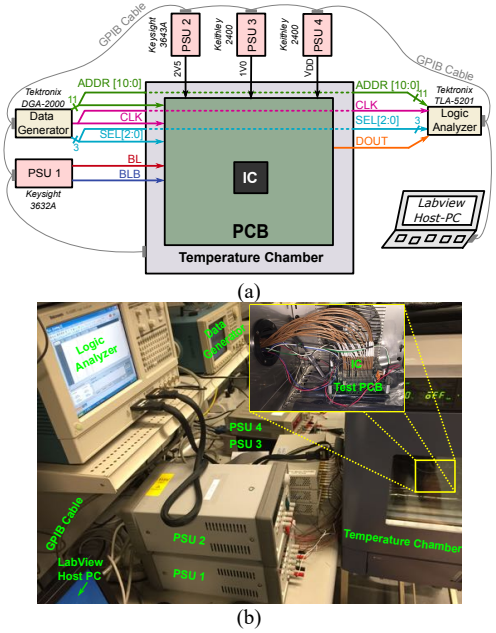

Fig. 23. (a) Test bench setup schematic. (b) Laboratory test bench setup.

VII. Measurement Results

All the offset measurements are performed across 10 ICs with the hysteresis stress test pattern of ΔV_{BL} and SAEB shown in Fig. 24. The hysteresis stress test pattern has two phases. The first phase is the stress phase, where a high negative ΔV_{BL} relative to the desired ΔV_{BL} under test is applied to ensure that all the SAs flip to the opposite state. The second phase is the test phase, where the desired ΔV_{BL} is applied, and the SA yield is recorded. For example, if the SA yield is to be measured for $\Delta V_{BL} = 10$ mV, then in the stress phase, a ΔV_{BL} of –70 mV is first applied to flip all SAs flip to logic '0'. Then in the test phase, the desired ΔV_{BL} of 10 mV is applied, and the yield of SAs that output the correct logic '1' is recorded. This procedure stimulates any adverse hysteresis effect caused by asymmetric parasitics and accounts them in the measurements of offset's standard deviation, σ_{OS} and the mean, μ_{OS}; which are the key metrics for SA's offset variation and skew, respectively.

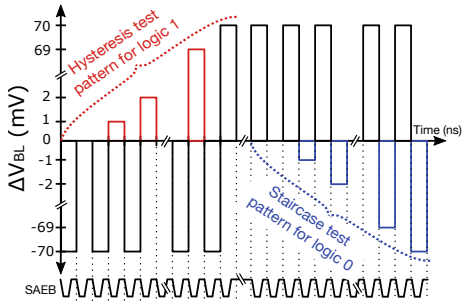

Fig. 24. Hysteresis stress test pattern of ΔV_{BL} used for SA V_{OS} characterization.

Fig. 25 shows the measured percentage of the SAs flipped to logic '1' across ΔV_{BL} at $V_{DD} = 0.4$ V composing a cumulative distribution function (CDF). These measurements are performed across 10 ICs, totalling 5120 SAs of each type at 25 ˚C, where ΔV_{BL} is applied with a 1 mV resolution using the hysteresis stress test pattern. The resulting probability density function (PDF) curves are presented in Fig. 26. They represent the portion of SAs flipped to logic '1' per ΔV_{BL}. The standard deviation of the measured PDF of each SA type is computed and indicated as σ_{OS}. The σ_{OS} of DISA-PD and DISA-FL is measured to be 11.8 mV and 11.7 mV, respectively. The conventional VLSA and CLSA performed with the σ_{OS} of 11.3 mV and 18.0 mV, respectively. Both the DIBBSA-FL/PD achieved the measured σ_{OS} of 10.2 mV; which is 9.7 % lower than VLSA and 43% lower than CLSA.

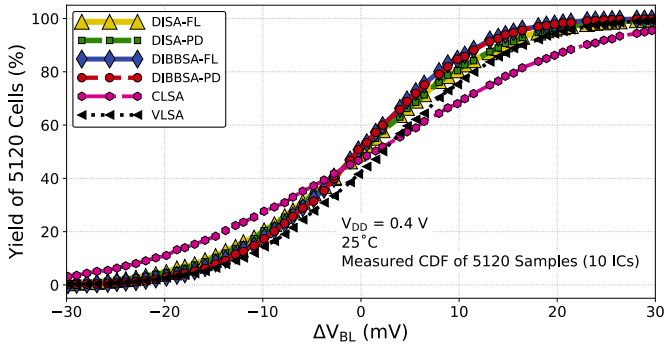

Fig. 25. Measured cumulative distribution showing the SA yield percentage across ΔV_{BL}. Measurements are performed at $V_{DD} = 0.4$ V and 25 ˚C across 5120 samples (from 10 ICs) of each SA type using the hysteresis stress test pattern of ΔV_{BL} with a step resolution of 1 mV.

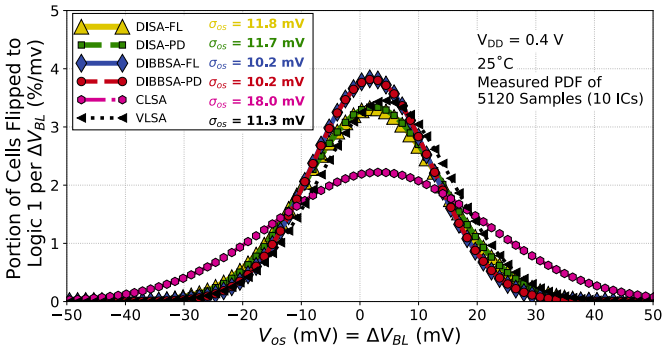

Fig. 26. Probability density derived from Fig. 25. It shows the portion of SAs flipped to logic '1' per mV of ΔV_{BL} at $V_{DD} =$ 0.4 V and 25 ˚C.

Similar σ_{OS} measurements are repeated across V_{DD} from 0.33 V to 1.0 V for all 10 ICs at 25 ˚C. The σ_{OS} versus V_{DD} is shown in Fig. 27. It highlights that DIBBSA-FL/PD performed similarly and had lower σ_{OS} compared to VLSA from V_{DD} of 0.33 V up to 0.7 V, with a minimum at 0.5 V. This optimum V_{DD} range for the DIBBSA manifests the differential drive strength analysis presented in Section V.

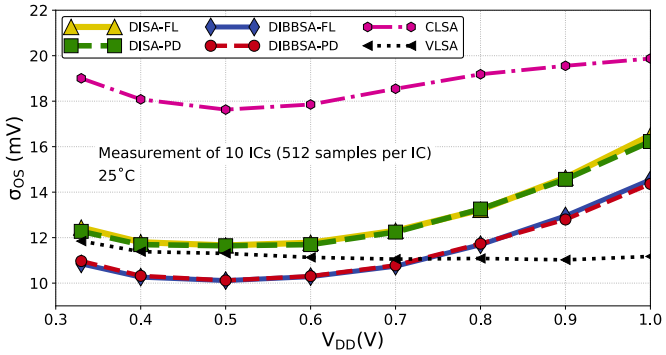

Fig. 27. Measured standard deviation of offset (σ_{OS}) from 5120 SAs (10 ICs) across V_{DD} with hysteresis stress test pattern at 25 ˚C.

The offset distributions parameters, σ_{OS} and μ_{OS}, from each of the 10 ICs at $V_{DD} = 0.4$ V are individually reported in Fig. 28 and Fig. 29, respectively. They show that both σ_{OS} and μ_{OS} remained lowest for the DIBBSA-FL/PD, highlighting its offset mitigation feature against within-die and inter-die variations.

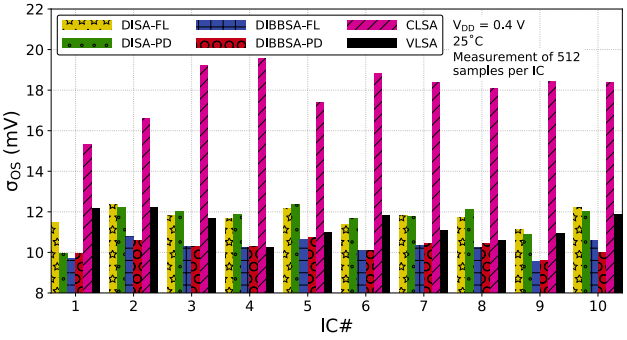

Fig. 28. Measured inter-die (die-to-die) standard deviation of offset distribution (σ_{OS}) from 512 SAs per IC across each of the 10 ICs with hysteresis stress test pattern at $V_{DD} = 0.4$ V and 25 ˚C.

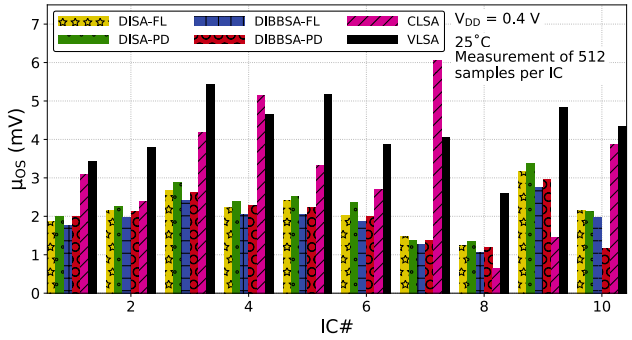

Fig. 29. Measured inter-die (die-to-die) mean of offset distribution (μ_{OS}) from 512 SAs per IC across each of the 10 ICs with hysteresis stress test pattern at V_{DD} = 0.4 V and 25 ˚C.

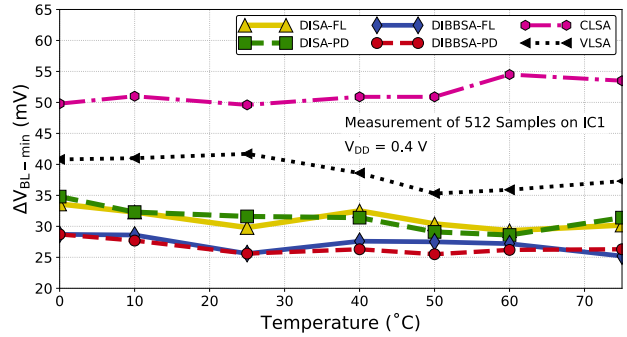

Fig. 30. Measured minimum required ΔV_{BL} (ΔV_{BL-min}) across temperature from 512 cells of IC #1 with hysteresis stress test pattern at V_{DD} = 0.4 V and 25 ˚C.

Equation (4) gives the minimum ΔV_{BL} necessary for all SAs to converge to a correct logic output, ΔV_{BL-min}. Fig. 30 shows ΔV_{BL-min} measured on IC #1 across temperatures from 0 ˚C to 75 ˚C.

$$\Delta V_{BL-min} = \max\begin{pmatrix} |\Delta V_{BL\,for\ 100\%\ \text{SAs in}\ Logic\ '1'}|, \\ |\Delta V_{BL\,for\ 100\%\ \text{SAs in}\ Logic\ '0'}| \end{pmatrix} \quad (4)$$

The DIBBSA-FL/PD performed best across the measured temperature range, with $\Delta V_{BL-min} = 27 \pm 2$ mV, compared to other SAs. On average, this is 28% and 48% lower than the VLSA and CLSA, respectively.

The $P_{dy-read}$, given by (5), is analyzed to determine the power savings using DIBBSA-FL/PD. The $P_{dy-read}$ is composed of bitline discharge, $P_{dy-BL/BLB}$, and P_{dy-SA}, specified in (6) and (7), respectively. The ΔV_{BL-min} is computed from (8), where the measured σ_{OS} of an SA is used as derived from Fig. 26. The ζ factor given by (9) represents the amount of ΔV_{BL-min} required per 1 mV of σ_{OS} to meet a certain read yield for a particular SRAM size in a given technology. Hence, it is a function of bitline capacitance, SRAM cell strength and targeted yield. The concept of ζ factor was previously mentioned in [16] for a 16 Mb SRAM in 28-nm CMOS and was measured to be ζ = 10 mV/mV for 97% yield. For this analysis in 65-nm CMOS technology, a value of ζ = 8 mV/mV is chosen as a starting point. The P_{dy-SA} is used from Fig. 19. Hence, the $P_{dy-read}$ is computed and its reduction compared to the VLSA is determined for DIBBSA-FL/PD and DISA-FL/PD. This analysis is plotted across a typical range of bitline capacitance, C_{BL} in Fig. 31. It predicts that DIBBSA-PD provide $P_{dy-read}$ savings for C_{BL} > 25 fF, where as DIBBSA-FL provide $P_{dy-read}$ savings unrestrictive of C_{BL}. Similar, analysis is repeated for probable range of ζ values where minimum requried C_{BL} for reduction in $P_{dy-read}$ compared to VLSA is shown in Fig. 32. It reveals that $P_{dy-read}$ is assured with DIBBSA-FL without any minimum required C_{BL}. For DIBBSA-PD, it requires C_{BL} > 32 fF to assure $P_{dy-read}$ reduction compared to VLSA.

$$P_{dy-read} = P_{dy-BL/BLB} + P_{dy-SA} \quad (5)$$

$$P_{dy-BL/BLB} = C_{BL} \cdot V_{DD} \cdot \Delta V_{BL-min} \cdot F_{CLK} \quad (6)$$

$$P_{dy-SA} = P_{dy-SA-V_{DD}} + P_{dy-SA-BL/BLB} + P_{dy-SA-SAE} \quad (7)$$

$$\Delta V_{BL-min} = \zeta \cdot \sigma_{OS} \quad (8)$$

$$\zeta = \frac{\Delta V_{BL-min}}{\sigma_{OS}} \left(\frac{mV}{mV}\right) \quad (9)$$

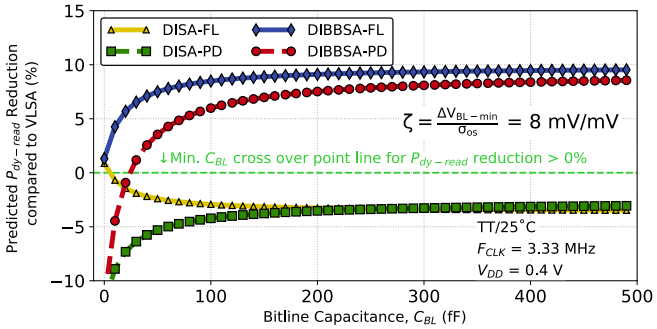

Fig. 31. Predicted read dynamic power ($P_{dy-read}$) reduction of the proposed DIBBSA architecture compared to VLSA across bitline capacitance (C_{BL}).

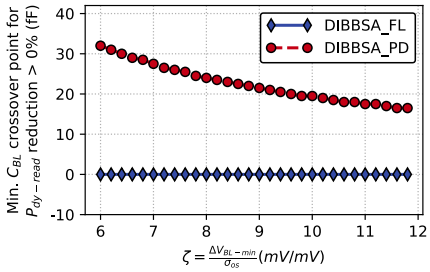

Fig. 32. Minimum C_{BL} crossover point for $P_{dy-read}$ improvement greater than 0% compared to VLSA across various values of ζ.

VIII. Comparison with State-of-the-Art

Table III compares state-of-the-art SAs to the proposed DIBBSA-FL/PD and other recent SAs with offset mitigation features in similar planner CMOS technologies. The SA from [33] with multi-phase MOS capacitor-based V_T matching implemented in 28 nm offers a 50% offset improvement at V_{DD} = 0.5 V compared to the VLSA. However, it takes an additional 4 transistors, 2 MOS capacitors, and 5 inverters, resulting in 3.2% area overhead in overall SRAM. [54], implemented in 65-nm CMOS, offers a 49% offset improvement compared to the CLSA, but with many additional devices per SA for body-bias-based offset calibration at startup; which results in a 3.5% overall SRAM area increase. [40] considers boosting the VLSA's differential and common mode ΔV_{BL} by adding a switched capacitor-based boosting circuit, providing a 23% offset improvement at V_{DD} = 0.3 V, but at the cost of a 12% SA area overhead and increased complexity in SA timing circuits. [62] simply precharges the CLSA outputs with

ΔV_{BL} to achieve 140 mV operation with a 1.7% improvement in SRAM read yield. [61] modifies the CLSA by judiciously precharging internal nodes with ΔV_{BL} to achieve a 7.6% iso-gate area improvement in offset at $V_{DD} = 0.4$ V. With the offset mitigation advantage of the dynamic body biasing with bitlines, the proposed DIBBSA-FL and DIBBSA-PD have reduced layout and total gate area compared to conventional VLSA and CLSA. Similar to [21] and [61], the iso-gate offset improvement of the proposed SAs can further be justified by using the Pelgrom's mismatch model, which gives the standard deviation of the V_T mismatch between two devices, $\sigma(\Delta V_T)$, given as

$$\sigma(\Delta V_T) = \frac{A_{T_0}}{\sqrt{WL}} \quad (10)$$

where A_{T_0}, W, and L are the technology-related area constant, width, and length of the two devices placed in proximity, respectively. If the additional 23.4% gate area is added to the DIBBSA-FL to equal the gate area of the VLSA, as shown in Fig. 5, it results in a further reduction of σ_{OS} by $\left(1 - \frac{1}{\sqrt{1-0.234}}\right) = 14.4\%$. Hence, the overall iso-gate-area improvement of σ_{OS} of the DIBBSA-FL results in $14.4\% + 9.7\% = 24.1\%$. Similarly, the iso-gate-area improvement for the DIBBSA-PD results in 18.1% compared to the VLSA. Table III makes similar comparisons with the CLSA.

It is noted that the body biasing dependence of the DIBBSA relies on the body-effect, which varies across technology and has become less significant as the technology scales down. Nevertheless, so long as the body terminal is available, this proposed DIBBSA-FL/PD can help provide a further reduction in offset with lower layout/gate area in low-voltage operations and hence, is a suitable replacement for the conventional VLSA and CLSA.

Table III.
COMPARISON OF THE PROPOSED DIBBSA-FL/PD WITH STATE-OF-THE-ART OFFSET MITIGATING SAS.

	[26] JSSC 2016	[45] JSSC 2014	[31] LSSC 2018	[52] JSSC 2017	[51] TCAS-I 2019		This work DIBBSA-FL		This work DIBBSA-PD	
Technology	28-nm HP	65-nm LP	65-nm GP	65-nm LP	65-nm GP		65-nm GP			
Measured Samples	2080	512	8192	16	5120		5120			
	(1 IC)	(1 IC)	(16 ICs)	(1 IC)	(10 ICs)		(10 ICs)			
Char. Type	Full SRAM	Full SRAM	SA array	Full SRAM	SA array		SA array			
Latch Type Sensing Topology	Multi-phase MOS capacitor-based threshold matching	CLSA with Body-bias offset calibration on power-up	Large signal differential and common mode boost, and using bitlines as SA supply	Precharging SA outputs with bitlines	Precharging multiple internal nodes with bitlines		Applying bitlines as a SA supply and at the body of the critical sensing transistors. Outputs are equalized before the evaluation.		Applying bitlines as a SA supply and at the body of the critical sensing transistors. Outputs are pre-discharged and equalized before the evaluation.	
# of Devices	11T+ 2 MOS Caps + 5 INV	15T + 2 NOR + 2 NAND + 3 INV + 1 Latch	11T + 2 MOS cap	9T	11T		7T		9T	
Design Effort Overhead	None	Static body biasing + calibration	Complex timing	None	None		Body-biasing with bitlines signals			
SA Area Reduction or Overhead [a.]	3.2% overhead in overall 128 kb SRAM (w.r.t VLSA)	3.5% overhead in overall 128 kb SRAM (w.r.t CLSA)	12% [d.] overhead w.r.t VLSA	16.8% overhead w.r.t CLSA	6.5% [c.], 4.5% [d] overhead w.r.t CLSA	30.7% [c.], 18.8% [d] overhead w.r.t VLSA	35.9% [c.], 21% [d.] reduction w.r.t CLSA	23.4% [c.], 14% [d.] reduction w.r.t VLSA	29.3% [c.], 16.2% [d.] reduction w.r.t CLSA	15.6% [c.], 1.5% [d.] reduction w.r.t VLSA
Offset Improvement	49% [a.] w.r.t VLSA @ 0.5 V, 85 °C	50% [a.] w.r.t CLSA @ 1.2 V	23.3% in Std. of offset @ 0.3 V, 25 °C	BER improvement from 2.8% to 1.1% [a.] @ 0.14 V, 25 °C	46.6% [f.] w.r.t CLSA	7.6% [f.] w.r.t VLSA	**68.1% [f.] w.r.t CLSA**	**24.1% [f.] w.r.t VLSA**	**61.8% [f.] w.r.t CLSA**	**18.1% [f.] w.r.t VLSA**
					@ 0.4 V, 25 °C		@ 0.4 V, 25 °C		@ 0.4 V, 25 °C	
$V_{DD\text{-}min}$ 25 °C	500 mV	370 mV	230 mV	140 mV	260 mV		330 mV		330 mV	

[a.] Compared to conventional topology implemented in respective work
[b.] Area overhead in 2 Metal layers only and not in
[c.] Total gate area overhead
[d.] Layout area overhead
[e.] Improvement in measured $\Delta V_{BL\text{-}min}$
[f.] Iso-gate area improvement in measured σ_{OS}

IX. CONCLUSION

The judicious application of body bias to the sensing transistors of a sense amplifier can help mitigate offset voltage, which reduces the required discharge of bitlines in SRAMs. We designed, simulated, fabricated, and tested proposed CMOS sense amplifiers, the DIBBSA-FL and DIBBSA-PD, that use the body bias effect to constructively reinforce output convergence to the right decision. The dynamic body biasing applied to the critical PMOS sensing transistors shifts the threshold voltages, setting the output trajectory in the correct direction towards the expected digital levels. The DIBBSA-FL/PD are the 7T and the 9T designs, respectively, with lower gate and layout area than the conventional VLSA. Importantly, DIBBSA-FL/PD provides iso-gate-area standard deviation of offset reduction by 24.1% and 18.1% compared to VLSA, respectively. This study also showed that the DIBBSA-FL/PD works reliably at $V_{DD} = 0.4$ V from 0 °C to 75 °C. Ultimately, for low-voltage applications,

DIBBSA-FL/PD can replace conventional SAs in SRAMs implemented in planner CMOS technologies.

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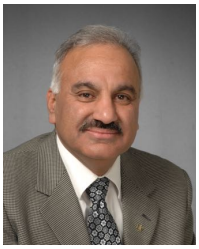
Dhruv Patel (M'12) received BASc. (Co-op, Hons.) and MASc. degrees in Electrical Engineering from the University of Waterloo and the University of Toronto in 2016 and 2020. He was involved with variation tolerant sub-threshold SRAM circuits research during undergraduate studies. Since 2019, he is pursuing a PhD. at the University of Toronto in integrated circuits for optical links.

Adam Neale (M'08) received the BASc., MASc. and Ph.D. degrees in Electrical and Computer Engineering from the University of Waterloo in 2008, 2010 and 2015. He is currently working as a Quality and Reliability Engineer with Intel Corporation in Hillsboro, Oregon, where he is responsible for developing radiation-induced upset reliability models. Dr. Neale was the Best Poster Paper Award recipient at the 2014 IEEE Custom Integrated Circuits Conference (CICC) for his work on multiple adjacent-bit upset error correcting codes for SRAMs.

Derek Wright (M'09) is a faculty member in the Electrical and Computer Engineering department at the University of Waterloo. His research interests include low-power digital circuit design, multidomain modeling and simulation, biomedical devices, and neuromorphic circuits and systems. He received the BASc. and MASc. degrees in Electrical and Computer Engineering from the University of Waterloo in 2003 and 2005, and the PhD degree in collaborative Electrical and Biomedical Engineering from the University of Toronto in 2010.



Manoj Sachdev (M'85-SM'97-F'12) received his B.E. degree (with Honors) in Electronics and Communication Engineering from IIT Roorkee (India), and Ph.D. from Brunel University (UK). He was with Semiconductor Complex Limited, Chandigarh (India) from 1984 till 1989 where he designed CMOS Integrated Circuits. From 1989 till 1992, he worked in the ASIC division of SGS-Thomson at Agrate (Italy). In 1992, he joined Philips Research Laboratories, Eindhoven (The Netherlands), where he researched on various aspects of VLSI testing and manufacturing.

Dr. Sachdev is a professor in the Electrical and Computer Engineering department, at the University of Waterloo, Canada. His research interests include low-power and high-performance digital circuit design, mixed-signal circuit design, test and manufacturing issues of integrated circuits. He has contributed to five books, two book chapters, and has co-authored over 200 technical articles in conferences and journals. He holds more than 30 granted and several pending US patents on various aspects of VLSI circuit design, reliability, and test. He, his students, and his colleagues have received several international awards. In 1997, at the IEEE European Design and Test Conference, he received the best paper award. In 1998, he was a co-recipient of the honorable mentioned award in the IEEE International Test Conference. He received the best panel award in 2004 IEEE VLSI Test Symposium. In 2011, he was a co-recipient of the best paper award in IEEE International Symposium on Quality Electronics Design. In 2015, he was a co-recipient of the best poster award in IEEE Custom Integrated Circuits Conference.

Professor Sachdev is an IEEE Fellow, Fellow of Engineering Institute of Canada, Fellow of Canadian Academy of Engineering; and has served on several conference committees. In 1999, he was the Technical Program Co-Chair for IEEE Mixed-signal Test Workshop. He also served as the Technical Program Chair from IEEE IDDQ Test Workshop in 1999, and 2000. In 2007-08, he was an Associate Editor for IEEE Transactions on Vehicular Technology. In 2008 and 2009, he was the Program Chair for Microsystems and Nanoelectronics Research Conference, Ottawa, Canada. He serves on the editorial board of the Journal of Electronic Testing: Theory and Applications. He was a member of technical program committee of IEEE Custom Integrated Circuits Conference from 2008 till 2014, and since 2016 he is a program committee member of IEEE Design and Test in Europe (DATE) conference.