University of Toronto, Department of Electrical and Computer Engineering

ECE 1387F - CAD for Digital Circuit Synthesis and Layout Handout #1

September 1999 J. Rose

Course Information - ANOTHER NEW ROOM (GB120)

Instructor: Jonathan Rose
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Pre-requisites: ECE 1388 (VLSI Design Methodology), or
ECE 451 (VLSI Systems), or
CSC 2410 (Algorithms in Graph Theory), or Permission of instructor.
Basic Programming Skills in C, including data structures.

Lecture: Wednesdays 10am-12 noon, **GB 120 - NEW ROOM!**.

Reference Texts: **Combinatorial Algorithms for Integrated Circuit Layout**, Thomas Lengauer, Wiley.
Logic Synthesis, S, Devadas, A. Ghosh. K. Keutzer, McGraw-Hill.

Evaluation:				
	Assignments	50% (3)	Paper	20%
	Exercises	15% (3)	Class Part	15%

Assignments Programming implementations of CAD problems such as placement, routing, logic optimization, technology mapping using optimization strategies such as simulated annealing dynamic programming, and branch and bound, and illustrated using computer graphics.

Exercises Hands-on experience with CAD tools such as VPR (Auto Place & Route), SIS (Logic synthesis), and BC (Behavioral Compiler).

The Paper Is a critical assessment of work in a subset of the field (chosen in consultation with the instructor) based on 3 to 4 papers.

Class Participation Is the expectation that you will contribute at least one good question or idea per class to the general discussion. Hopefully much more!

Tentative Lecture and Assignment Schedule

#	Date Lecture	Lecture Topic	Assignment/Exercise **Out**	Assignment/ Exercise **In**
1	Sept 15	Introduction, Overview of Synthesis	Paper	-
2	Sept 22	Detailed Routing	Assignment 1 - Maze Router on FPGA	-
3	Sept 29	Timing-Driven Routing	-	
4	Oct 6	Placement	-	Assignment 1
5	Oct 13	Placement (Simulated Annealing)	Exercise 1 - Placement	-
6	Oct 20	Partitioning (Branch & Bound)	Assignment 2 Partitioning Using B&B	Exercise 1
7	Oct 27	Technology-Independent Logic Optimization	-	-
8	Nov 3	Technology-Independent Logic Optimization	Exercise 2 Using Logic Synthesis	Assignment 2
No Lecture, November 10				
9	Nov 16	Technology Mapping (Dynamic Programming)	Assignment 3 Technology Mapping using Dyn Prog	Exercise 2
10	Nov 24	High Level Synthesis		-
11	Dec 1	High-Level Synthesis	Exercise 3 Synopsys Behavioural Compiler	Assignment 3
12		Scheduling and Allocation.	-	Paper & Exercise 3