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First Name:............................ Last Name:............................

Student Number:..

University of Toronto
Faculty of Applied Science and Engineering

Midterm Examination – November 1994

ECE241F – Digital Systems

Examiner – Paul Chow

1. There are 6 questions and **10** pages. Do **all** questions. The total number of marks is 100.
2. **ALL WORK IS TO BE DONE ON THESE SHEETS!** Use the back of the pages if you need more space. Be sure to indicate clearly if your work continues elsewhere.
3. Please put your final solution in the box if one is provided.
4. **No calculators allowed.**
5. **Paper Type D** – Examiner specified aids. You are permitted to use personal textbooks, the LogicWorks manual, and any of your personal notes. Unauthorized photocopies of copyrighted material are not permitted.

1 [15]	
2 [10]	
3 [15]	
4 [15]	
5 [25]	
6 [20]	
Total [100]	

[15 marks] 1. For the function

$$F(A,B,C,D) = \Sigma(3,4,5,11)$$

with don't cares

$$\overline{A}BC + ABD$$

(a) Draw the minimal NAND/NAND circuit.

F

AB \ CD	00	01	11	10
00				
01				
11				
10				

(b) Draw the minimal NOR/NOR circuit.

F

AB \ CD	00	01	11	10
00				
01				
11				
10				

(c) Which is the lowest cost solution based on # gates + # inputs? Why?

[10 marks] 2. A four-input function, G(A,B,C,D), outputs a one if the binary equivalent of the input is divisible by 3 or 7. Zero is not considered to be divisible by any numbers in this case. Draw the truth table for this function and give the lowest cost expression for G, where cost is measured in terms of # gates + # inputs.

[15 marks] 3. You have four positive edge triggered JK flip flops with the following characteristics:

Setup time T_S = 2ns
Hold time T_H = 3ns
Clock to Q delay T_D = 8ns (flip flop delay)

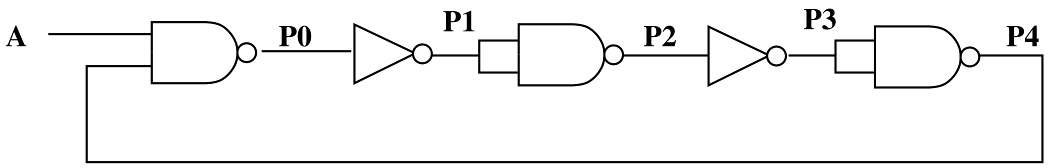
and gates that have a delay of 4ns.

(a) Show how to connect the four flip flops as a serial 4-bit shift register using a minimal number of extra gates. There should also be an input line called *serial in* and an output called *serial out*.

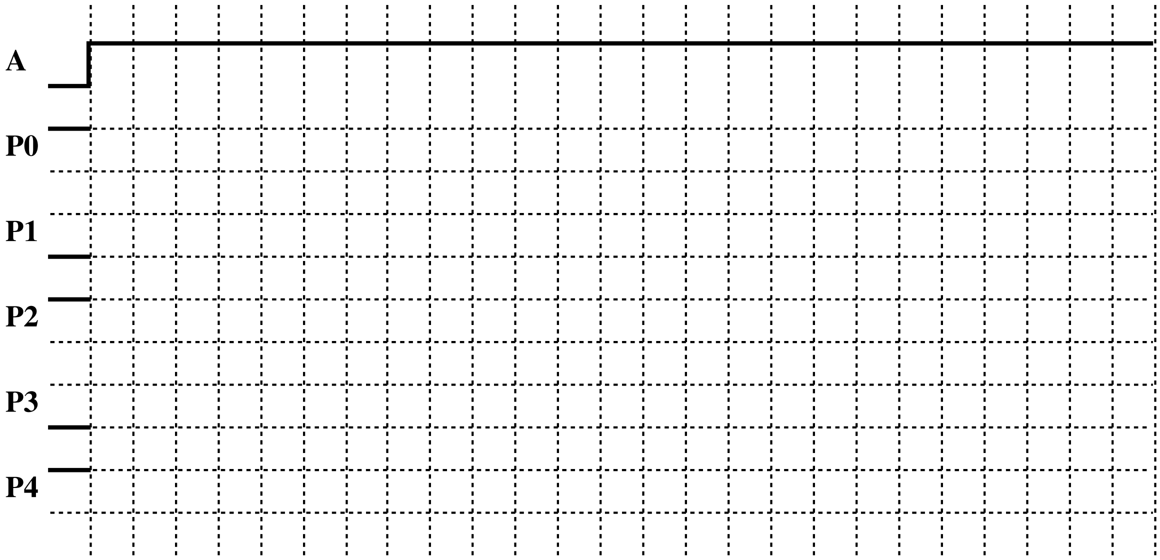
(b) What is the maximum clock frequency that you can use for this shift register? Show how you get your answer.

(c) If T_H = 10ns, would this shift register function properly? Explain your answer.

[15 marks] 4. Consider the circuit below. Assume that the NAND gates have twice the delay of an inverter.

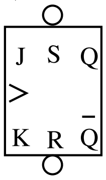


(a) Complete the timing diagram below. Assume that each division corresponds to one inverter delay.



(b) If it is determined that in a $10\mu s$ period there were 125 pulses at **P4**, what is the delay of an inverter?

[25 marks] 5. Using the positive-edge triggered JK flip flops with asynchronous set and clear inputs as shown in the symbol below, you are to implement a counter that counts in the sequence 000, 001, 011, 010, 110, 111, 101, 100, and repeats.



(a) What type of counter is this?

(b) Give the state transition table with the remapped next-state functions.

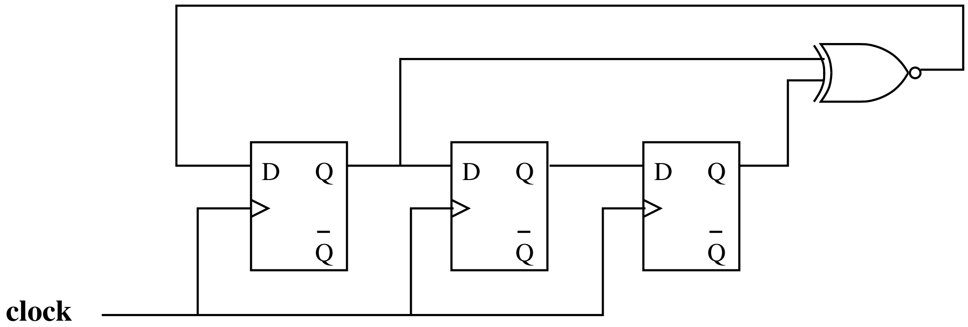
Question 5 continued...

(c) Derive the minimal expressions for the next-state functions.

Question 5 continued...

(d) Draw the complete schematic for your circuit. Include a way to initialize the counter to 010.

[20 marks] 6. Assume that the counter below is initialized to 000.



(a) Give the state transition diagram for the circuit.

(b) Is the counter self starting? Explain.

Question 6 continued...

(c) Explain how you would use LogicWorks to verify your solution by describing the features of LogicWorks that you would use. You may use diagrams if that will help.