University of Toronto, Faculty of Applied Science and Engineering
Department of Electrical and Computer Engineering

ECE 241F - Digital Systems

September 1996 P. Chow, J. Rose

Lecture, Lab Schedule and Contents - Revised Schedule - Readings are wrong

Date	Lecture	Reading	Lab/Tutorial/Assignment
Sept 5.	• Motivation & course outline • Handouts • expectations, lab schedule, • tutorial sign up	1.0, 1.2 - 1.2.1	
Sept 6.	• logic primitives - AND, OR, NOT & NAND, NOR, XOR, XNOR • how to build gates with simple transistors	1.2.2, 1.2.3	
Sept 10.	• logic representation & simple boolean algebra - sum of products from truth table, product of sums • representations - binary numbers	1.3.2, 1.3.3 App A.	Tutorial #1 • AND, OR NOT • Venn diagram • full adder impl.
Sept 12.	• design of full adder • demo Logic Works • handout logic works exercise, due in tutorial next week	1.3.4, 2.1, 2.2	
Sept 13.	• time response in networks • simple performance calculations (3.5.2) • circuits with feedback • inverter chain, timing diagram		Problem Set #1 • A.1 to A.5, A.7, 1.2, 1.4, 1.7, Venn diags, 2.1
Sept 17.	• RS latch • set-up and hold times • latches and flip-flops • triggering - positive edge and negative edge	3.3, 6.1	Tutorial #2: • take up questions on PS#1 • questions on logicworks • collect logic works exercise

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Sept 19.	• JK , D, Master/Slave Flip-flops • timing methodologies	6.1, 6.2, 6.3, 6.4	Problem Set #2 • 2.3, 2.7, 2.9, 2.12, 2.13, 2.15 • handout
Sept 20.	• registers, shift registers and counters, analysis of counter (FSM analysis) 7.1 • ripple vs. synchronous counters (7.5)	6.1, 6.2 6.3	
Sept 24.	• two-level optimization • Technology Metrics (2.5.1) • boolean algebra • DeMorgan's theorem (proof)	7.1, 7.5	• Lab #1 • using the test equip & protoboards • how to wire up circuits • use circuits from LogicWorks Exercise 1 • RS latch analysis
Sept 26.	• Karnaugh Maps (2.3) • don't cares	2.3 (omit 2.3.2)	Problem Set 3: 3.13, 3.14, 6.1, 6.7, 6.10, 6.11, 6.17
Sept 27.	• design examples using Karnaugh maps		
Oct 1.	• Multiplexors (4.2.2) • Decoders, demultplexors (4.2.3) • multi-level logic (3.1)	3.1 4.3 7.2 7.3	Lab #2 • measuring gate delay
Oct 3.	• combinational logic word problems (4.3)		Problem Set 4: 7.1, 7.4, 2.17, 2.19, 2.20, 2.26, 2.28
Oct 4.	• synchronous counter design (7.2) • self-starting counters (7.3) • talk about Lab #2		
Oct 8.	• counter designs (7.4) • excitation tables for R/S, J/K		Tutorial #3 • optimization and flip-flops • discuss problem sets 3 and 4.

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Oct 10.	• design process (1.1) • refinement of representations, specifications and constraints, top-down vs bottom-up, design rules, debugging • 1.2-1.3 digital hardware systems and representations		Problem Set 5: 3.4, 3.5(a-f), 4.22
Oct 11.	• fan-in and fan-out as design rules • timing diagrams, waveform representations • propagation delay, describing behaviours • what is rapid prototyping, Lab 3 discuss		
Oct 15.	• Data Sheets (3.5.1) • Inputs and Outputs - switches and LEDs (3.5.3) • Schematic conventions	7.4, 7.5, 7.6, 4.2.2, 4.2.3, 4.2.4	Lab #3 • 2-bit ALU -- large design
Oct 17.	• Programmable Logic - PALs, PLAs, ROMS (4.1, 4.2.5)		Problem Set 6: 7.10, 7.14, 7.16
Oct 19.	• Designing PALs with ABEL - PAL manual and 10.1.4		
Oct 22.	• Finite State Machine Analysis - Mano 6-4 and 8.1 FSM concepts	4.1, 4.2.5 PAL man intro, 8.1	Lab #4 • PAL Tutorial/Intro + Lab assignment
Oct 24.	• FSM design approach -- synthesis (8.2)		Problem Set 7: 7.18 to 7.22 inclusive
Oct 25.	• Other representations (8.3)		
Oct 29.	• Moore and Mealy designs (8.4) • Hand out project proposal forms	8.2, 8.3, 8.4	Tutorial #4 • prep for midterm, problems sets 5, 6 and 7
Oct 31.	• FSM Synthesis examples - word problems: serial adder, D and JK synthesis		Problem Set 8: 4.1, 4.8, 4.10, 4.15, 4.23

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Nov 1.	• More FSM synthesis word problems		
Nov 5.	• State Minimization 9.1, 9.2	8.5,9.1, 9.2	Lab #5 • 4-bit ALU using PALs and edge-triggered Ds • lab assignment
Nov 7.	• State assignment in general, do briefly- dense, one-hot (9.3)		Midterm this week on November 6th.
Nov 9.	• Flip-flop choices (9.4) • FSM partitioning (9.5)		Project Proposals due in the lab - must be approved and signed by TA or instructor
Nov 12.	• FSM design with ROMS and PALs (10.1)	9.3 (not 9.3.4), 9.4, 9.5 10.1	Project Week #1 • discuss proposals with TA **disagree - need to have it agreed on by the time project starts**
Nov 14.	• Field-Programmable Gate Arrays (10.3)		Problem Set 9: 8.7, 8.10, 8.13, 8.17, 8.21 (draw state diagram), 9.3 (user row matching)
Nov 15.	• RAMs (7.6)		
Nov 19.	• Tri-state and open collection (4.2.4)	10.3 5.1	Project Week #2
Nov 21.	• slack		
Nov 22.	• Number Systems (5.1), overflow, underflow		
Nov 26.	• Fast adders/subtractors (5.2)	5.2	Project Week #3
Nov 28.	• combinational multiplier (5.5)		
Nov 29.	• slack		
Dec 3.	• Asynchronous Circuits/Hazards? (3.4)		