University of Toronto, Department of Electrical and Computer Engineering

ECE241F - Digital Systems - Lab 3

More Complex Logic Design Using 7-Segment Displays

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1.0 Purpose

The purpose of this lab is to build several more complex logic circuits and to gain increased familiarity with the Altera maxplus2 design software.

2.0 Background

A seven-segment display is often used on computers, watches, VCRs and many electronic devices to display numbers and some characters. It consists of seven independent lights in an "8" configuration as shown below in Figure 1 on page 3. By turning on different segments, you can display different numbers and some letters.

3.0 Preparation

You are to create two of logic circuits to drive one of the seven-segment displays on the Altera UP-1 board. Please see Section 5.0 for details of how to use and hook up to these boards. (In particular, note that to turn a segment on, you must drive the corresponding pin to a logical "0").

Your preparation, to be marked, should consist of the VHDL code and the simulator output for all circuits. Print out the simulation results and VHDL code for marking. Use the timing simulator for the 7128 device if you're using the student version of maxplus2.

1. Design a circuit that takes a four bit (X_3, X_2, X_1, X_0) input from the digital switch board (like you did in Lab #2) and drives digit #1 on the Altera board as described in the table below. Note that for the letters, some are capitalized and some are not. (The reason is that a capital B, for example, would come out the same as an 8 on a 7-segment display, so we will display a lower case b instead).

X_3 X_2 X_1X_0	**Display (note the capitalization)**
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	b
1100	C
1101	d
1110	E
1111	F

Determine the equations for the 7-segment display segments, and minimize them using the Karnaugh-map method described in class. Write VHDL code to represent the logic function for each segment as a boolean equation (with AND, NOT, OR etc.). Simulate and test your equations using the maxplus2 functional or timing simulation on the MAX 7128S device.

2. Design a similar circuit to the one given in part 1, except that you should use the four input switches to generate the letters of your last name. For example, if your last name is Suvanthingham, you could use code 0000 to display an S, 0001 to display a U, 0010 to display a V (or something as close to a V as you can get). Note that you can choose any code you wish for each letter. Notice also that you don't need to create two codes for a letter that appears twice in your name. For example, the letter A appears twice in Suvanthingham, but you only need to produce one code for the letter A - the intent is that you will be able to spell out your last name on the 7-segment display by entering the codes for the letters one at a time.

   Fairness alert: if your last name is longer than 8 *unique* letters, you need only do 8 unique characters of it. If your last name is shorter than 8 characters, you must add more letters of your first name until you have coded at least 8 unique characters.

   Since you will only need to do 8 codes, you can leverage the don't cares that will be available in the truth tables.

4.0 In the Lab

1. First, to check and make sure that the 7-segment display and Altera board are working, by copying the file ~jayar/ece241/lab3/flash.pof (on the ECE ugsparc system or the ECF sparks system) and place it into a separate directory.

   Then, open the **Programmer** module and use **File | Select Programming File**, and select the file flash.pof. Click OK in the prompt that asks if it's OK to change the project to "flash". Once the file is downloaded it will count using the 7-segment displays.

   The VHDL source code for this program is in two files, in the directory ~jayar/ece241/lab3. The file flash.vhd uses four counters and two 7-segment decoders. The file seg7.vhd has the 7-segment decoder description. Look at this code to get an idea of what you will learn later in the course. Note that it will not be easy to understand the code that is written in the files. **DO NOT** use this code in your lab here, it is just meant as a test programming file for the board. (In this lab you must create direct equations for all of the logic).

2. Download and test your circuits from the preparation. Show each working circuit to the TA.

5.0 Connections Between MAX 7128 and The Seven-Segment Decoder

The Altera UP-1 board has two seven segment displays attached directly to the pins of the chip. The figure below shows the naming of each segment. The subsequent table gives the connections between segments and the MAX 7128 pins. **NOTE: to turn a segment on, you must drive the associated pin with a "0." (not a 1).**

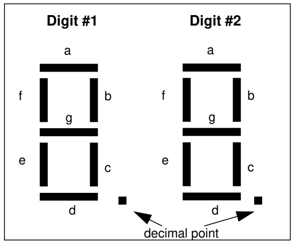

Figure 1 - *Seven Segment Display*

Display Segment	7128 Pin for Digit 1	7128 Pin for Digit 2
a	58	69
b	60	70
c	61	73
d	63	74
e	64	76
f	65	75
g	67	77
Decimal point	68	79