University of Toronto, Department of Electrical and Computer Engineering

ECE241F - Digital Systems - Lab 5

Adders and Registers

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1.0 Purpose

The purpose of this lab is to introduce the logic needed to create an adder, and use it in combination with registers. The lab also provides practice in coding VHDL and schematic entry.

2.0 Background

Read Section 5.1 and 5.2 of the text to learn about binary number representation, and how to build a **ripple-carry adder**.

Using the 3-bit register (with reset) that you built in lab 4, and the seven-segment decoder you built in Lab 3 you will build an adder unit, as shown in Figure 1, whose inputs are: a single three-bit binary number ($X_2X_1X_0$) the clock, and the Reset signal. The four-bit output of the adder is connected to the 7-segment display so that it can be viewed. In the preparation below, you are required to figure out how to use this circuit to add two three-bit numbers. This is actually a simple version of the arithmetic and logic unit found inside all computers.

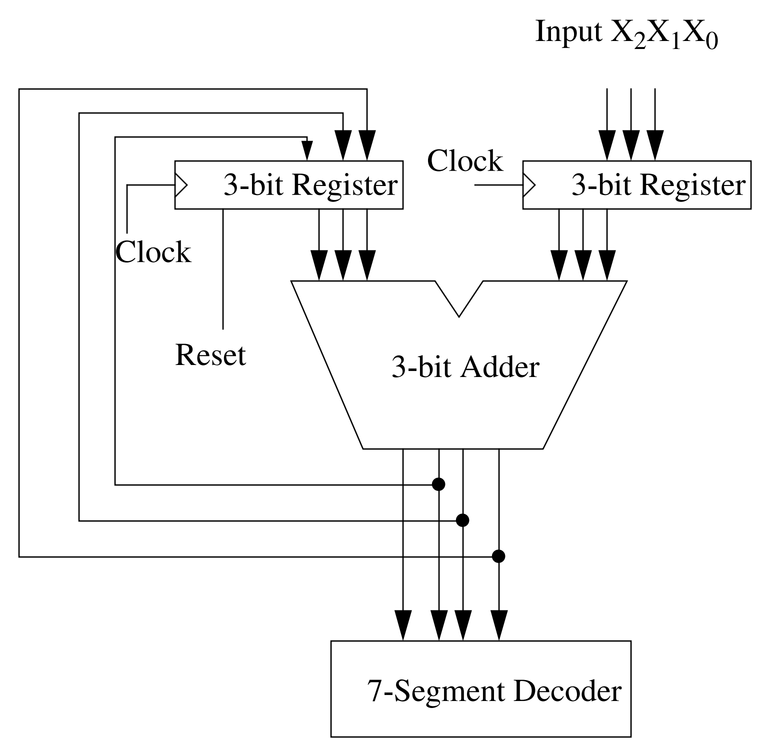

Figure 1 - *Adder Unit Schematic*

3.0 Preparation

1. Determine the sequence of control signals and data inputs that you would need to be able to add **two** 3-bit numbers using the circuit of Figure 1. You will need to know this in order to properly simulate the circuit that you will be designing. The sequence is essentially a timing diagram (giving the sequence of the input values $X_2X_1X_0$, Reset and clock) such as you would create using the waveform editor of maxplus2 to test the circuit.

2. Design, using VHDL, a 3-bit ripple-carry adder. You should design the adder as a basic logic function - do not use the built-in addition capability of VHDL. Simulate the adder using maxplus2 timing simulation to be sure that it works. Note that a 3-bit adder has two 3-bit inputs and one four-bit output. For use in the parts below, convert your adder into a symbol that can be imported into the graphic editor.

3. Using the adder, two 3-bit D-type registers with reset, and your seven-segment decoder circuit from Lab 3, build the circuit of Figure 1 using the graphic editor. Simulate your circuit to ensure that it works.

4. Design and simulate the same circuit using VHDL only (i.e. don't use the graphic editor). You will need to read the VHDL reference manual closely in order to do this.

4.0 In The Lab

1. Build and test the adder circuit from part 2 of the preparation.

2. Build and test the register/adder/display unit from part 3 of the preparation.

3. Build and test the register/adder/display unit from part 4 of the preparation.