University of Toronto, Faculty of Applied Science and Engineering
Department of Electrical and Computer Engineering

ELE 241F - Computer Organization **November 6, 1996**

Mid-Term Examination

1. Answer all questions.
2. **ALL WORK IS TO BE DONE ON THESE SHEETS!** Use the back of the pages if you need more space. Be sure to indicate clearly if your work continues elsewhere.
3. Each question has a different assigned value, as indicated. Total marks available are 60.
4. Verify that your exam has all 10 pages.
5. Aids allowed: Contemporary Logic Design textbook, LogicWorks manual, PAL manual and personal notes.
6. Unauthorized photocopies of copyrighted material are not permitted.

PRINT:

Name: ______________________

Student Number: ______________________

Question 1:	/10
Question 2:	/7
Question 3:	/10
Question 4:	/15
Question 5:	/8
Question 6:	/10
TOTAL:	/60

1. **[10 marks]**

   This question deals with the function $F(a,b,c,d) = \Sigma\,(0,1,6,8,13,14)$.

1a. Determine the minimized two-level sum-of-products boolean expression for this function using the Karnaugh map below. The minimal expression is one that has the fewest gates + gate inputs.

F

ab \ cd	00	01	11	10
00				
01				
11				
10				

Boolean Expression:

1b. Give the logic gate design for the circuit using AND and OR gates. You may use gates with "bubbles" on the inputs to indicate inversion.

1c. Given that the input combinations abcd = 0010, 0101, 0111, 1001, and 1010 and will never occur, give a new minimized two-level sum of products expression for the function, using the same minimization criterion as in question 1a.

Use the following Karnaugh Map:

F

ab \ cd	00	01	11	10
00				
01				
11				
10				

Boolean Expression:

2. **[7 marks]** Consider the following two-level boolean expression:

$$\mathbf{f} = a\,b\,c + a\,\bar{b}\,\bar{c}\,\bar{d} + \bar{a}\,\bar{c}\,d + \bar{a}\,b\,\bar{c}$$

2a. Determine a multi-level boolean expression (using only the Boolean operators AND, OR and NOT) for the function **f** that uses the fewest literals. How many literals were saved compared to the two-level expression?

Expression:

Number of Literals Saved:

2b. Give the logic gate design that corresponds to this multi-level expression, **under the following restriction:** the fanin (i.e. the maximum number of inputs) to the AND and OR gates is limited to two inputs. You may use “bubbles” on the inputs of gates to indicate inversion.

Circuit

3. **[10 marks]** Recall that a binary-coded decimal (BCD) is a four bit number that is used to represent a single base 10 digit - the numbers from 0 to 9.

   Design and optimize a two-level combinational circuit that determines if a BCD digit is **greater than 8** or **less than 3.** Be sure to make maximum use of don't cares. Answer the questions below to do this.

3a. Identify the inputs and outputs.

Inputs:

Outputs:

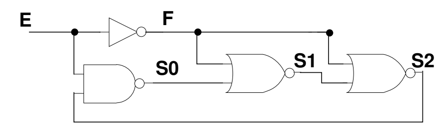
3b. Create the truth table and Karnaugh map representation of the function:

0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

	00	01	11	10
00				
01				
11				
10				

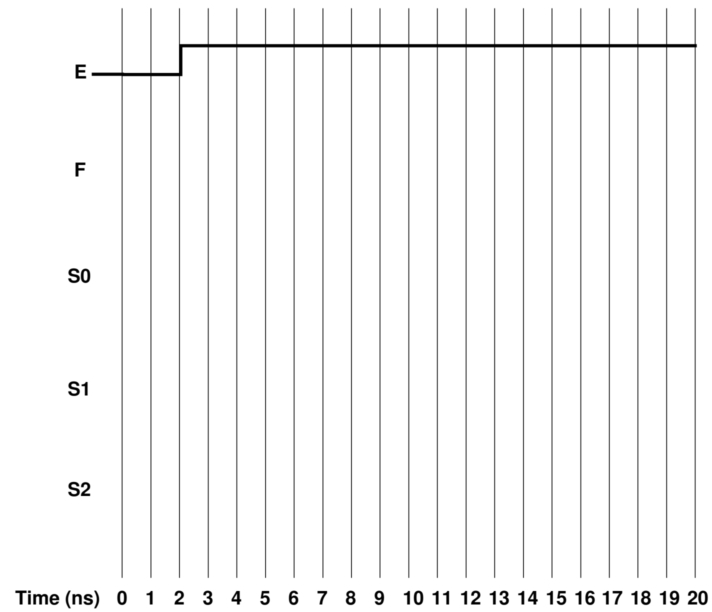
3c. Give the minimum cost two-level sum of products boolean expression for the function, where cost is defined as the number of gates + number of gate inputs.

4. **[15 marks]** Consider the following circuit:



Assume that each type of gate has the following propagation delay:
NOT: 1ns, NAND: 2ns, NOR: 2ns.

4a. Complete the following timing diagram. For each transition (edge), indicate by means of an arrow, which previous transition caused it.



4b. What is the *period* of oscillation of the signal S2?

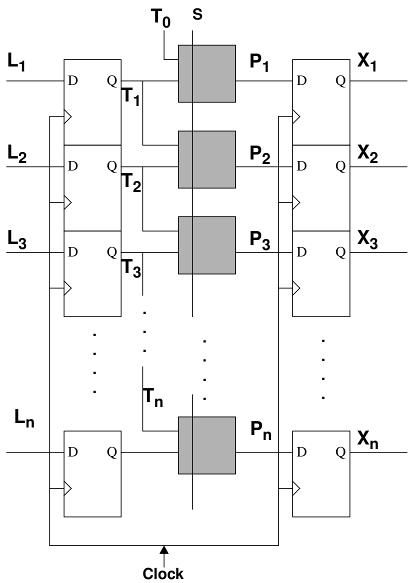
Period of Oscillation:

4c. Suppose that the above circuit has **N** NOR gates in a row (rather than two as illustrated in the picture) in addition to the one NAND. For each of the following values of **N**, indicate if the circuit will oscillate or not, and if so give the *period* of the oscillation.

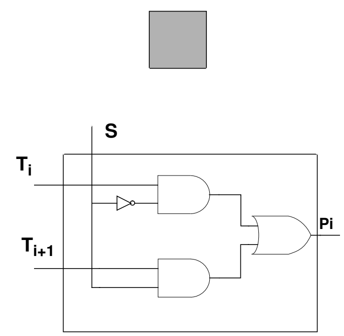
N	4	9	10	25
Oscillates? (Yes or No)				
Period of Oscillation				

5. **[8 marks]** Give the *complete* (i.e. should be able to compile) ABEL-HDL program for the circuit of question 4, using the P18CV8 PAL. Include one test vector for the input E = 0.

6. **[10 marks]** Consider the following sequential circuit:



The shaded sub-circuit contains:



6a. State, in words, what happens to the values of $\mathbf{X_i}$ (i = 1...n), as a function of the $\mathbf{T_i}$ (i= 0...n) after a positive edge on the clock signal arrives, under the following two circumstances:

i. S = 0

ii. S = 1

6b. Given the timing values in the table below, determine the minimum *period* that the clock can have for which the system will still operate correctly. Assume that the signals S and T_0 arrive (i.e. are stable) 1.5ns after the positive clock edge. Show the work that you used to determine the minimum period.

Gate/Attribute	Delay
AND Gate Delay (T_{and})	3ns
OR Gate Delay (T_{or})	4ns
NOT Gate Delay (T_{not})	1ns
Set-up Time (T_s) of D Flip-Flop	2ns
Hold Time (T_h) of D Flip-Flop	1ns
Clock-to-Q Time (T_{cq}) of D Flip-Flop	2.5ns