University of Toronto, Faculty of Applied Science and Engineering
Department of Electrical and Computer Engineering

ECE 241F - Digital Systems

September - December 1997 S. Brown, J. Rose

Lecture, Lab Schedule and Contents

#	Date	Lecture	Chapter	Lab
1	Sept 4.	• Motivation & course outline • handouts: tutorial, expectations, lab schedule, lab, project • light switches as logic functions, • basic AND/OR Gates	1	• No lab
2	Sept 5.	• Variables & Functions, inversion • simple boolean expressions • truth tables; gates	2	
3	Sept 9.	• Boolean Axioms, laws; venn diagram • minterms; synthesis from truth tables - sum of products • minterms; product of sums	2	• No lab
4	Sept 22.	• simple algebraic minimization; example	2	
5	Sept 12	• Lab 1 Discussion • Voltage, • Transistor switch • 7400 series • NMOS gate	3	

#	Date	Lecture	Chapter	Lab
6	Sept 16.	• NMOS &CMOS gates	3	• Lab 1 • TTL/Protoboard • comb logic; show that two circuits have same function • circuit debug
7	Sept 18.	• transistor operation • real propagation delay • waveform • prop delay through network	3	
8	Sept 19.	• Lab 2 Discussion • PALS & CPLDs • Intro to CAD • Intro to VHDL	3	
9	Sept 23.	• Optimization 1 • K maps	4	• Lab 2 • Altera Tutorial • comb logic needed only
10	Sept 25.	• Optimization 2 • don't cares	4	
11	Sept 26.	• Optimization 3	4	
12	Sept. 30.	• Optimization 4 • multi-level logic, factoring	4	• Lab 3 • more complex logic function design - 7 seg?
13	Oct 2	• Flip Flops 1	6	
14	Oct 3	• Flip Flops 2	6	
15	Oct 7.	• Flip Flops 3	6	Week of MIDTERM
16	Oct 9.	• MIDTERM!	6	
17	Oct 10.	• Shift Register Example of FF's • Counters	6	
18	Oct 14.	• Set-up/Hold Time, Clock to Q • State Machine 1	8	• Lab 4 • Sequential Logic - RS Latch, Master-Slave D FF •
19	Oct 16.	• State Machine 2	8	
20	Oct 17.	• State Machine 3	8	

#	Date	Lecture	Chapter	Lab
21	Oct 21.	• State Machine 4	8	• Lab 5 • Small State Machine
22	Oct 23.	• Numbers/Arithmetic Representation • Adder - using basic logic	7	
23	Oct 24.	• Full Adder • Project Description, handout proposal forms	7	
24	Oct 28.	• Critical Path Delay • Carry Lookahead Adder	7	• Lab 6 • Big State machine - ALU controlled by switches
25	Oct 30.	• Gate Delay; critical path? • fanout dependency	3	
26	Oct 31.	• Power Dissipation	3	
27	Nov 4.	• I/O Devices		• Lab 7 • Electrical Issues: • gate delay measure, fanout dependency • Power Dissipation • I/O Devices
28	Nov 6.	• Glitches and Hazards		
29	Nov 7.	• Ring Oscillator		
30	Nov 11.	• Tristate Gate, Open Collector • Transmission Gates • Multiplexors		• Project Week 1
31	Nov 13.	• Multiplexors as Logic		
32	Nov 14.	• Demultiplexors, Decoders		
33	Nov 18.	• 2's complement notation		• Project Week 2
34	Nov 20.	• Multipliers		
35	Nov 21.	• Bit Serial Addition		
36	Nov 25.	•		• Project Week 3
37	Nov 27.	• slack		
38	Nov 28.	• FPGAs		
39	Dec 2	• Course Summary		• no lab; • Project Report Due