University of Toronto, Faculty of Applied Science and Engineering
Department of Electrical and Computer Engineering

ECE 241F - Digital Systems

September - December 1998 S. Brown, J. Rose

Lecture, Lab Schedule and Contents

#	Date	Lecture	Chapter	Lab
1	Sept 10	• Motivation & course outline • handouts: tutorial, expectations, lab schedule, lab, project	1	• No lab
2	Sept 11	• light switches as logic functions, • truth tables; gates • basic AND/OR Gates	2	
3	Sept 15	• Variables & Functions, inversion • simple boolean expressions • simple synthesis of logic -sum of products representation,, minterms • minterms; synthesis from truth tables - sum of products	2	• No lab
4	Sept 17	• Boolean Algebgra, axioms,laws; • simple algebraic minimization; example	2	
5	Sept 18	• Lab 1 Discussion • Voltage, • Transistor switch • 7400 series • NMOS gate	3	

#	Date	Lecture	Chapter	Lab
6	Sept 22	• NMOS &CMOS gates - build using transistors	3	• Lab 1 • TTL/Protoboard • comb logic; show that two circuits have same function • circuit debug
7	Sept 24	• Lab 2 Discussion • PALS & CPLDs • Intro to CAD • Intro to VHDL • maxplus2 demo	3	
8	Sept 25	• Optimization 1 • K maps, 2 & 3 variable	4	
9	Sept 29.	• Optimization 2 • 3 & 4 variable K maps	4	• Lab 2 • Altera Tutorial • comb logic needed only
10	Oct 1	• Optimization 3 • don’t cares & 7 segment example	4	
11	Oct 2	• Optimization 4 • multi-level logic, factoring	4	
12	Oct 6	• Numbers/Arithmetic Representation • Adder - using basic logic, Full Adder, ripple carry adder	5	• Lab 3 • Combintational logic for 7 segment decoder
13	Oct 8	• Sequential Logic; defn of comb. vs seq • cross-coupled NOR latch • Transparency, RS Latch, D Latch, • timing diagram; desire for edge trip	7	
14	Oct 9	• Flip Flops 2 • master-slave D-type flip flop • timing diagram, set up & hold, clock to Q	7	
15	Oct 13	• Serial Transmission of Data - shift registers, parallel to serial conv.	7	• week of midterm
16	Oct 15	• MIDTERM!		
17	Oct 16	• slop	6	

#	Date	Lecture	Chapter	Lab
18	Oct 20.	• Registers/Counters • Ripple Counters • Synchronous Counter	7	• Lab 4 • Sequential Logic - RS Latch, Master-Slave D FF + hierarchical design • • • • • Project Headsup
19	Oct 22	• State Machine 1 • intro • steps • simple recognizer	8	
20	Oct 23	• State Machine 2 • circuit • VHDL of FSM	8	
21	Oct 27	• State Machine 3 • Moore • pop machine example	8	• Lab 5 • Adders and Registers
22	Oct 29	• State Machine Minimization - Brown method • Mealy	8	
23	Oct 30	• Example State Machine design for transmission system • Lab 6 Discussion	8	
24	Nov 3.	• Signed Number Representation • Project Description, handout proposal forms	5	• Lab 6 • Small finite state machine - sequence recognizer
25	Nov 5.	• 2's complement addition and Subtraction	5	
26	Nov 6	• Lab 7 discussion - takes a whole lecture, concerns LPMS, handshaking big FSMs, FSM review	8	

#	Date	Lecture	Chapter	Lab
27	Nov 10	• transistor operation at process level • real propagation delay • waveform • prop delay through network (Critical Path Delay) • Carry Lookahead Adder	3 5	• Lab 7 • big finite statemachine, modules and handshaking
28	Nov 12	• Gate Delay; critical path • Demo Altera Timing Analyzer • fanout dependency	 3	
29	Nov 13	• Hierarchical Cary Lookahead • Bit Serial Adder • Ring Oscillator	5 8	
30	Nov 17	• FPGAs, LUT Mapping • Multiplexors	3, 4 6	• Project Week 1
31	Nov 19	• Multiplexors, Multiplexors as Logic	6	
32	Nov 20.	• Demultiplexors, Decoders	6	
33	Nov 24	• Tristate Gate, Open Collector • Transmission Gates	3 3	• Project Week 2
34	Nov 26	• debouncing switches	10	
35	Nov 27	• VHDL	A	
36	Dec 1	• Mulipliers	5	• Project Week 3
37	Dec 3	• SRAM	10	project report due
38	Dec 4	• Course Summary		