University of Toronto, Department of Electrical and Computer Engineering

ECE241F - Digital Systems - Lab Schedule and Information

Fall 1999 A. Carusone, P. Lehn, J. Rose

The real learning in this course goes on in the laboratory where you design, build and debug real circuits. There are seven labs of three hours each (you have one 3-hour lab every week) plus one 3 week (9 hour) project at the end of the term. **You will work in groups of two.**

There are two parts to the lab experience: preparation, which you do outside of the lab hours, and the actual implementation of circuits in the lab.

Preparation

Each lab usually requires you to do significant amount of preparation work, and is where you must do much of the work to understand the concepts. Preparation **must** be complete before the lab begins. Preparation will usualy require design using the Altera software. Each partner in the group of 2 must submit a separate preparation. It be graded by the TAs at the beginning of the lab, on the following basis:

Judgement of TA	Grade
Unable to explain any part of preparation	0*
Made a legitimate attempt	1
Some merit to work	2
Reasonable job, may be some missing things	3-4
Correct and Done well, demonstrated clear knowledge of subject.	5

In-Lab Work

In each lab you will have to typically build a working circuit. Once this is done, for each such circuit, show it to your TA for grading, out of 3:

Judgement of TA	Grade
Did not attend or try	0
Tried, but failed to get much working	1
Most, but not all working	2
Everything worked	3

Note: Although the lab portion of the course is worth only 10%, both the midterm and the

final exam will contain questions directly related to skills learned in the lab. (*) Also, please be aware that severe penalties will be imposed for copying of labs, as evidenced by an inability to explain work presented as preparation.

Lab Workstation Number and Maintenance

Each digital workstation has a number. Please use the same station each week. If a piece of equipment is not working, please tell a TA to tag the board with the problem and notify someone to have it repaired. Otherwise it will be broken the next time you need to use it!

Lab Section, Day Time and Location

Section	Day	Time	Place
1	Thursday	9am-12noon	GB 144/150 & SF 2201
2	Monday	9am-12noon	GB 144/150 & SF 2201

Lab and Project Schedule

Monday/Thursday	Lab
Sept 20/23	Lab1 - Introduction to Combinational Logic and TTL **GO TO LAB IN ROOM SF 2201 THIS FIRST DAY; YOU'LL BE ASSIGNED TO A ROOM FROM THERE**
Sept 27/30	Lab 2 - Altera Software Intro and Tutorial
Oct 4/7	Lab 3 - 7-Segment Combinational Logic Design
Oct 11/14	Week of MIDTERM, no lab
Oct 18/21	Lab 4 - Sequential Logic and Hierarchical Design
Oct 25/28	Lab 5 - Adders and Registers
Nov 1/4	Lab 6 - Finite State Machines
Nov 8/11	Lab 7 - Complex Finite State Machine Modules and Handshaking Project Proposal Due this week, in lab day.
Nov 15/18	Project Week 1
Nov 22/25	Project Week 2
Nov 29/Dec 2	Project Week 3; additional lab periods in evening will be available.
	Project Report Due December 3