University of Toronto

Department of Electrical and Computer Engineering

ECE241- Digital Systems

Midterm Examination

October 1998

Last Name: ____________________

First Name: ____________________

Student Number: ____________________

Signature: ____________________

Duration: **1 Hour**

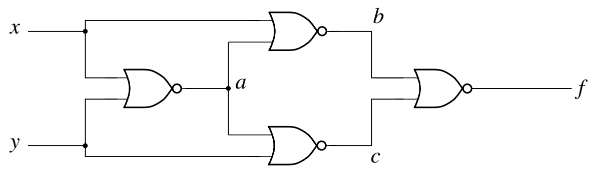
Answer ALL questions on this test paper. There is extra space at the end if you need it.

EXAMINER's REPORT

1	______	/15
2	______	/10
3	______	/12
4	______	/13
TOTAL:	______	/50

Question 1 — **[15 marks]**

a. The circuit shown below has the output f and the inputs x, and y. You are to derive the logic expressions for the intermediate nodes a, b, c and the output f, and then on the next page, minimize the expression for f.



a = ______________________________

b = ______________________________

c = ______________________________

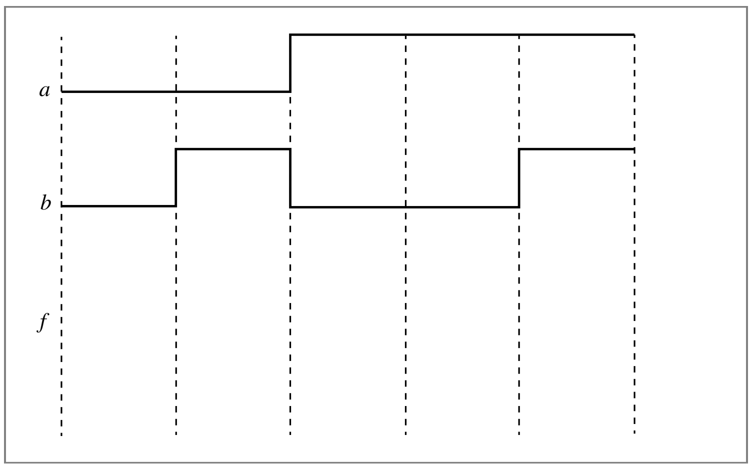
f = ______________________________

Use **algebraic manipulation** to find the minimal sum-of-products expression for the function f derived above. You must show all of the steps.

b. **Circle all** the *legal* VHDL statements below which correctly represent the function $f = \bar{x}y + x\bar{y}$. A legal statement has the correct syntax and semantics.

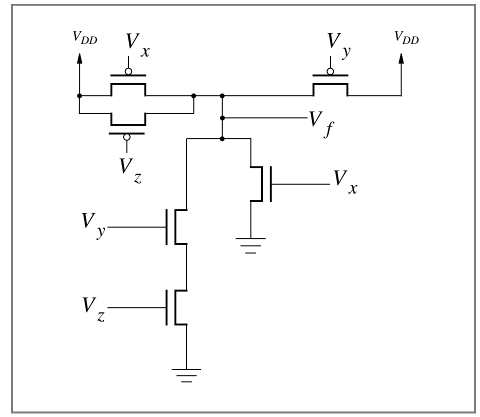
- f <= (x **AND NOT** y) **OR** (**NOT** x **AND** y) ;
- f <= (**NOT** x **AND NOT** y) **OR** x ;
- f <= **NOT** x **AND** y **OR** x **AND NOT** y ;
- f <= (**NOT** x **OR** y) **AND NOT** y ;
- f <= (**NOT** x **AND** y) **OR** (x **AND** NOT y) ;

c. Draw the **output waveform** for the function $f = \bar{a}b + a\bar{b}$ on the timing diagram below.



Question 2 — [10 marks]

a. The CMOS circuit below contains an error in the pull-up network (the "P-part"). Draw the corrected PUN (P-part) in the space given below (you do not have to draw the PDN (N-part)).



ANSWER:

b. Draw a CMOS complex gate that implements the function below. Use as few transistors as you can in your solution (Hint: consider $\bar{f}$).

$$f = xy + xz$$

ANSWER:

Question 3 — **[12 marks]**

a Consider a truth table in which there are a total of k entries that are marked as d, for don't care. The other entries are set as either 1 or 0. How many different logic functions are represented by this truth table?

ANSWER: ____________________

b Consider the logic function

$$f = \sum m(0, 2, 3, 4, 6, 7, 8, 10, 11, 12)$$

What are the prime implicants of this function (there is extra space for rough work at the end of this test paper)?

ANSWER: ____

____

What are the essential prime implicants:

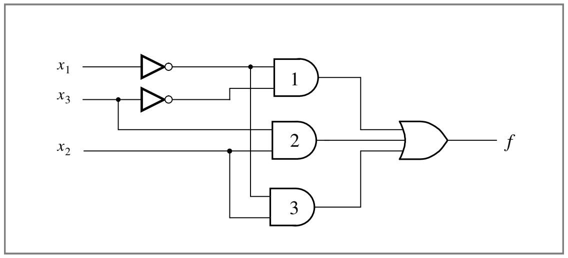
ANSWER: ____

Give a minimal cover in sum-of-products form:

ANSWER: ____

c The circuit below shows a 3-input logic function, f. Can any of the AND gates in this circuit be removed from the circuit without changing the logic function? If so, which gate(s) is it (1,2, or 3)?

ANSWER: ____



Question 4 — **[13 marks]**

The K-maps for two 4-variable logic functions, f and g, are shown below. Indicate on the K-maps how the two functions should be implemented such that the resulting 2-output circuit has minimal cost. Use a sum-of-products realization for both functions. Show your expressions for f and g in the spaces provided below and give the cost of the 2-output circuit. In your cost calculation, you should count the NOT gates needed to invert the inputs.

K-map for f:

x_1x_2 / x_3x_4

0	0	0	0
1	1	1	0
1	1	d	0
0	1	0	0

K-map for g:

x_1x_2 / x_3x_4

0	d	0	0
1	0	1	1
1	0	1	1
0	1	d	0

Expression for f: ____

Expression for g: ____

Total cost: ________________

EXTRA SPACE — USE ONLY IF NEEDED

EXTRA SPACE — USE ONLY IF NEEDED

EXTRA SPACE — USE ONLY IF NEEDED