University of Toronto, Faculty of Applied Science and Engineering
Department of Electrical and Computer Engineering

ECE 241F - Digital Systems

September - December 1999 A. Carusone, P. Lehn, J. Rose

Lecture, Lab Schedule and Contents

#	Date (accurate section3)	Lecture	Chapter	Lab
1	Sept 10	• Motivation & course outline • handouts: tutorial, expectations, lab schedule, lab, project	1	• No lab
2	Sept 14	• light switches as logic functions, • truth tables; gates • basic AND/OR Gates	2	• No lab
3	Sept 15	• Variables & Functions, inversion • simple boolean expressions • simple synthesis of logic - from truth tables	2	
4	Sept 17	• Lab 1 Discussion • Voltage, • Transistor switch • 7400 series • NMOS gate	2	
5	Sept 21	• NMOS &CMOS gates - build using transistors	3	• Lab 1 • TTL/Protoboard • comb logic; show that two circuits have same function • circuit debug
6	Sept 22	• finish NMOS & CMOS • PALS & CPLDs	3	
7	Sept 24	• Lab 2 Discussion • Intro to CAD • Intro to VHDL • maxplus2 demo	3	

#	Date (accurate section3)	Lecture	Chapter	Lab
8	Sept 28	• sum of products representation, minterms • Boolean Algebgra, axioms,laws; • simple algebraic minimization; example	4	• Lab 2 • Altera Tutorial • comb logic needed only
9	Sept 29.	• Optimization 1 • K maps, 2 & 3 variable	4	
10	Oct 1	• Optimization 2 • 3 & 4 variable K maps	4	
11	Oct 5	• Optimization 3 • don’t cares & 7 segment example	4	• Lab 3 • Combintational logic for 7 segment decoder
12	Oct 6	• Optimization 4 • multi-level logic, factoring	5	
13	Oct 8	• Numbers/Arithmetic Representation • Adder - using basic logic, Full Adder, ripple carry adder	7	
14	Oct 12	• Sequential Logic; defn of comb. vs seq • cross-coupled NOR latch • Transparency, RS Latch, D Latch, • timing diagram; desire for edge trip	7	• **MIDTERM!** • no lab; • this is the missing thanksgiving monday!!!
15	Oct 13	• Flip Flops 2 • master-slave D-type flip flop • timing diagram, • set up & hold time of FF; clock-to-Q	7	
16	Oct 15	• Serial Transmission of Data - shift registers, parallel to serial conv.		

#	Date (accurate section3)	Lecture	Chapter	Lab
17	Oct 19	• slop	6	• Lab 4 • Sequential Logic - RS Latch, Master-Slave D FF + hierarchical design • • • • • Project Headsup
18	Oct 20.	• Registers/Counters • Ripple Counters • Synchronous Counter	7	
19	Oct 22	• State Machine 1 • intro; simple recognizer • steps - state diagram • method #1 - 1 one encoding direct method	8	
20	Oct 26	• State Machine 2 • method #2 - full encoding, State Trans Table, K-map etc.	8	• Lab 5 • Adders and Registers
21	Oct 27	• State Machine 3 • VHDL of FSM • Lab 6 discussion - handshaking!	8	
22	Oct 29	• General form of Moore Machine [Mealy machine not taught!] • Example State Machine design for transmission system	8	
23	Nov 2 .	• State Machine Minimization - Brown method • Project Headsup, handout approval form	8	• Lab 6 • Small finite state machine - sequence recognizer • handshaking state machine at high speed
24	Nov 3.	• Lab 7 discussion - takes a whole lecture, concerns LPMS, handshaking big FSMs, FSM reviev • Demo Altera Timing Analyzer	5	
25	Nov 5.	• Signed Number Representation	5	

#	Date (accurate section3)	Lecture	Chapter	Lab
26	Nov 9	• 2's complement addition and Subtraction	8	• Lab 7 • big finite statemachine, modules and handshaking
27	Nov 10	• transistor operation at process level • real propagation delay • waveform • fanout dependency	3 5	
28	Nov 12	• Debouncing switches • four methods	3	
29	Nov 16	• RAM - SRAM • LPMs for SRAM • Altera 10K RAM • How to use RAM	5 8	• Project Week 1
30	Nov 17	• Internal working of SRAM • bit, row, column • deocder (for address bus) • tristate gate (for data bus)	3, 4 6	
31	Nov 19	• Gate Delay; critical path • maximum clock frequency • hold time violations • Flip flop timing - setup and hold, clock to Q	6	
32	Nov 23.	• Reading delays for data sheets • Ring Oscillator	6	• Project Week 2
33	Nov 24	• Cary Lookahead Adders	3	
34	Nov 26	• Hierarchical Carry Lookahead • Bit Serial Adder	10	

#	Date (accurate section3)	Lecture	Chapter	Lab
35	Nov 30	• FPGAs, LUT Mapping • Multiplexors	A	• Project Week 3 project report due
36	Dec 1	• Multiplexors, Multiplexors as Logic • Demultiplexors, Decoders	5	
37	Dec 3	• Course Summary, Exam Discussion, slop	10	